Design and Simulation of Multi Channel UART for Serial Communication

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ABSTRACT
UART (Universal Asynchronous Receiver Transmitter) is used for serial communication. It is used for long distance and low cost process for transfer of data between pc and its devices. In general a UART operated with specific baud rate. To meet the complex communication demands it is not sufficient. To overcome this difficulty a multi channel UART is proposed in this paper. And the whole design is simulated with modelsim and synthesized with Xilinx software

Keywords
UART, Baud rate generator, First in First Out, Simulation.

1. INTRODUCTION
To meet the modern operation microcontroller and digital signal processor we need desired system performance. But in actual process, it is very difficult to attain desired result, since it depends on various factors. Communication is vital factor which affect the performance of system.

UART is a kind of serial communication circuit most widely used. In parallel communication process we need more address and data lines. So it is limited to short distance. When compared with parallel communication, serial communication has more advantage [1]. It need less transmission lines, low distortion, high reliable and very much useful for long distance transmissions.

A UART is a integrated circuit which plays the most important vital role in serial communication. This serial communication process is much suited for long distance data transmission because of less transmission lines [2]. But to meet the modern complex communication need with different baud rates, a single channel UART is not sufficient. Since this single channel UART operated with specific baud rate. The data loss may happen in the communication process due to difference in speeds which may leads to bit error. To overcome the above difficulty a multi channel UART is proposed in the paper. A multi channel UART internally consists of 4 single channel UART which were operated with different baud rate. This multi channel UART facilitates the user to select UART form the multiple UART based on the requirement. This process reduced delay because of in built buffer i.e. FIFOs also introduced in this multi channel UART. And one more advantage in this 4 UART can operate parallel i.e. more devices can able to communicate with the pc randomly

2. DESIGN OF MULTI CHANNEL UART
To meet the modern communication need a multi channel UART is proposed in this paper. This multi channel UART consists of 4 UARTs which will operate at different baud rates. The simple block diagram of multi channel UART is shown in Fig.1

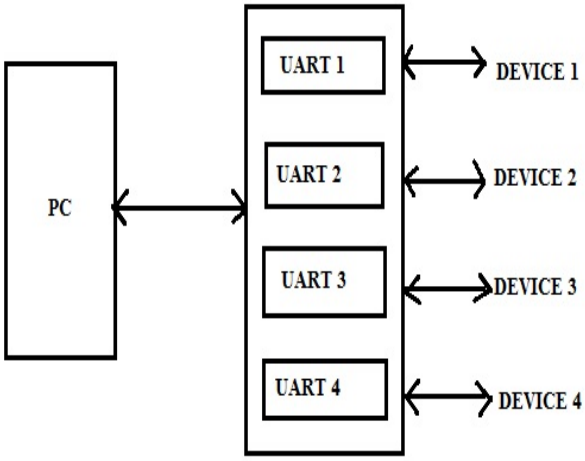

Fig 1. Simple Block diagram of multi channel UART

In the figure 1, the 1st device communicates with pc through UART 1 with baud rate 9600. The 2nd device communicates with pc through UART 2 with baud rate 19200. The 3rd device communicates with pc through UART 3 with baud rate 38400. The 4th device communicates with pc through UART 4 with baud rate 4800. For designing the multi channel UART, we need to design UARTs with buffer i.e. FIFO at receiver and transmitting ends. UART is internally divided into five sub-modules. They are baud rate generator, transmitter logic, receiver logic, transmitter FIFO and receiver FIFO. The basic block diagram of UART is shown in Fig.2

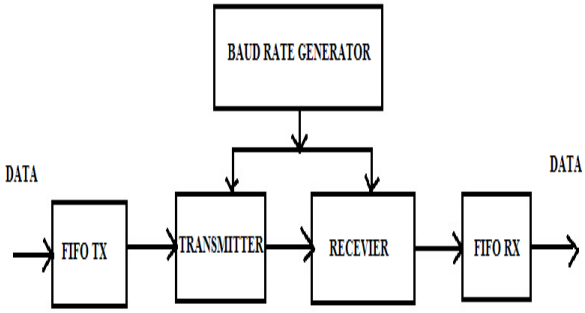

Fig 2. Block diagram of UART with FIFO

UART transmitter logic receive parallel signal and converted into serial data, the UART receiver logic receive serial signal and converted into parallel signal and FIFO are used to avoid the loss of data.

2.1. Design of Transmitter logic

The main function of transmitter logic is to read data from the transmitter FIFO, covert parallel data into serial data and send to peripherals. The finite state machine design of transmitter logic shown in below Fig. 3.

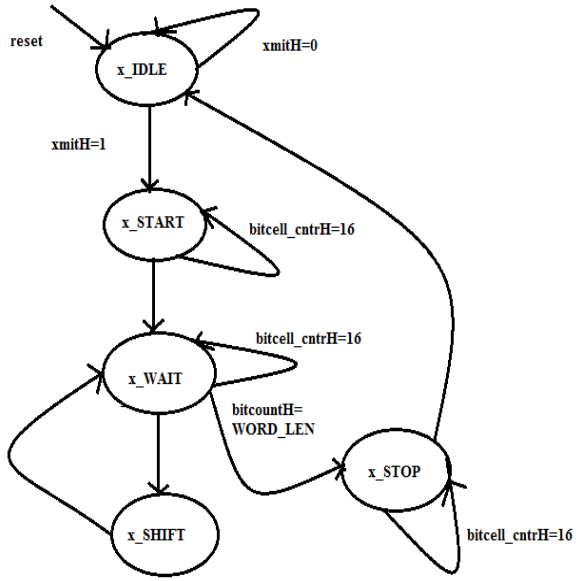

Fig 3. UART transmitter state machine

The state machine of transmitter controller contains 5 states. They are x_IDLE, x_START, x_WAIT, x_SHIFT, x_STOP. When reset is applied, the state machine defaults to x_IDLE state. In this state, the state machine idles for as long as no transmit command is given . But when xmitH become active high, then the serializer is loaded and the state machine transitions to x_START state. In x_START state, the uart_ xmitH mux is set to 1, and 1 baud tick is waited before transitioning to x_WAIT state. In x_WAIT state, the uart_ xmitH mux is set to point to the shift register, and 1 baud tick is waited. After the wait complete, if all bits (WORD_LEN) have been transmitted then the state machine transitions to x_STOP, otherwise it goes to the x_SHIFT state. In the x_SHIFT state, the shift-register is shifted by 1 bit, and transitions to x_WAIT state. In x_STOP state, the uart_xmitH mux is set to 1, 1baud tick is waited and then transitions to x_IDLE state. Then the state machine waits in the same state until the next bunch of data is received for conversion.

2.2 Design of receiver logic

The main function of receiver logic is to convert the serial data into parallel data and forwarded to peripherals through FIFO. The finite state machine design of receiver logic is shown in below Fig. 4

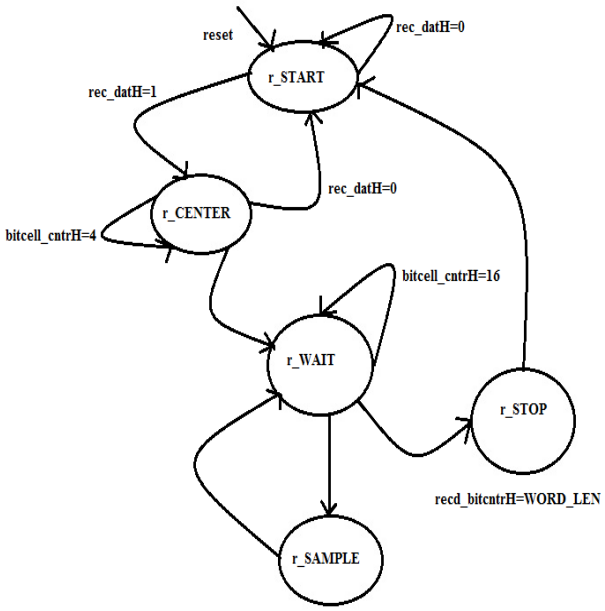

Fig 4. UART receiver state machine

The state machine of receiver controller contains 5 states. They are r_START, r_CENTER, r_WAIT, r_SAMPLE, r_STOP. When reset is applied the state machine defaults to r_START state. The state machine lies in that condition until the condition is detected. Once the start bit is detected, it transitions to r_CENTER state. In r_CENTER state, the state machine waits for ½ bit cell in order to find the bit cell center. A bit cell is baud "tick" and corresponds to 16 uart_clk ticks. So ½ bit cell corresponds to 8 uart_ticks. The bit cell counter is used to generate the delay. The reason for waiting for 4 uart_ticks is that the synchronizer uncertainly adds up to 2 uart_ticks. Once bit cell counter is found, if the state of the rec_dataH is still low, then this is not a valid start bit, so the state machine transition back to r_START state. The r_WAIT state simply waits for 1 baud tick. Once 1 baud ticked, the incoming date can be sampled into the de-serializer. If all WORD_LEN bits have been sampled, then the state machine transitions to r_STOP state. In r_STOP state, the state of rec_dataH is sensed. The state machine transition to r_START. And waits for next data.

2.3 Baud Rate Generator

Baud rate generator is a programmable bit timing device that is used to synchronize the bit duration for both the transmitter and receiver sections of serial communication. This baud rate generator produced pulse, which determines the baud rate of UART transmission. The baud rate frequency factor is calculated according to a system clock. Let assume that the system clock is 32MHz, baud rate is 4800 bit per second, and then output clock frequency of baud rate generator should be 16*4800Hz. Therefore the frequency coefficient (M) of baud rate generator is measured as

$$M = 32MHz/16*4800Hz=416$$

In the baud rate generator design, the receiver clock frequency is designed to be 16 times the baud rate, therefore each data width received by UART is 16 times the receive clock cycle.

2.4 Asynchronous FIFO

Since read and write clock of the data bus and UART's clock may not be the same. So loss of data may happen and bit error may occur. To avoid the difficulties a buffer i.e. FIFO is proposed in this paper. The main function of FIFO buffer is to send and receive data, and reduce the interaction time between the serial port and the CPU [4]. And also, it can improve the transmission efficiency between CPU and UART. This asynchronous FIFO is used to transmit data from one clock domain to another clock domain. This asynchronous FIFO consist of four parts they are read pointer, write pointer, empty flag and full flag

3. VERIFICATION OF RESULT

The whole design of multi channel UART is simulated with modelsim software and synthesized with Xilinx software

3.1 Transmitters Simulation Results

During the transmitters simulation process the baud rate generator frequency of UART1, UART2, UART3, and UART4 are maintained at 153600Hz, 307200Hz, 614400Hz and 76800Hz respectively. The Fig 5 shows the simulation results of multiple transmitters.

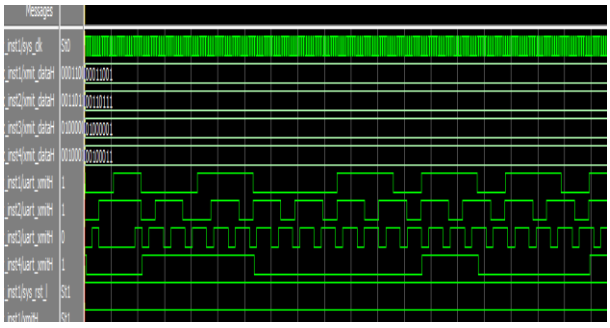

Fig 5 Simulation results of multiple Transmitters

3.2 Receivers Simulation Results

During the receiver's simulation process, the system clock frequency is set to 32MHz, and the baud rate of UARTs maintained at 9600bps, 19200bps, 38400bps and 4800bps respectively. The Fig 6 shows the simulation results of multiple receivers with different baud rates.

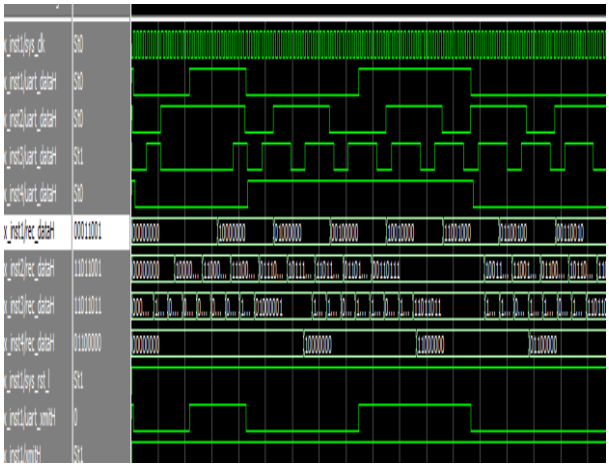

Fig 6 Simulation results of multiple Receivers

3.3. Simulation Results of FIFO at Transmitters and Receivers

The simulation results of FIFOs are obtained by using the modelsim software. The Fig 7 show the simulation result of FIFOs which are place at the receiving and transmitting ends

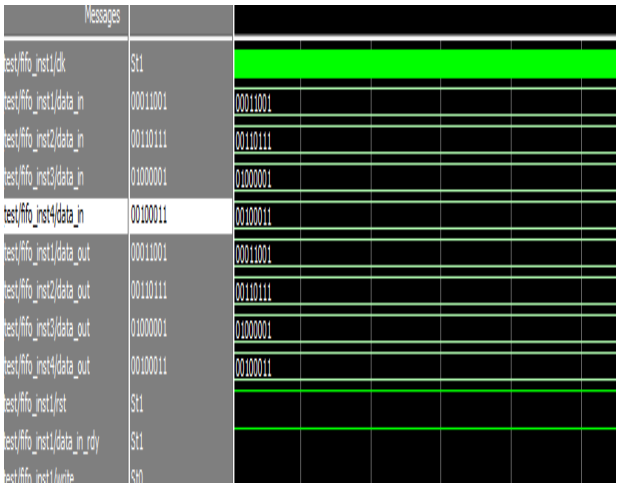

Fig 7 simulation results of FIFOs

3.4 Simulation Result of Baud rate Generators

The simulation results of Baud rate generators are obtained by using the modelsim software. The fig 8 show the simulation results

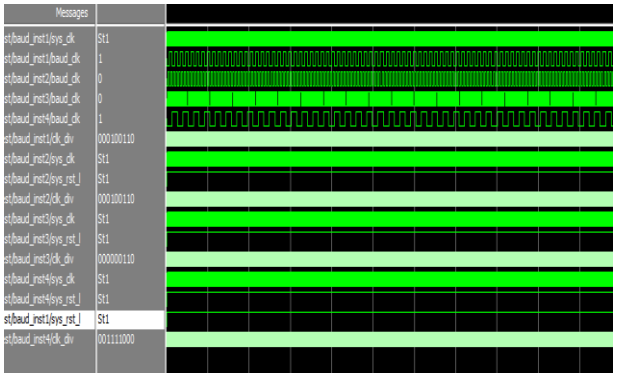

Fig 8 Simulation results of baud rate generators

3.5 RTL of Multi channel UART

The RTL of multi channel UART is obtained by synthesizing the whole multi channel UART design with the Xilinx software. The Fig 9 shows the RTL of multi channel UART. The RTL of multi channel UART includes the baud rate generators, transmitters and receivers

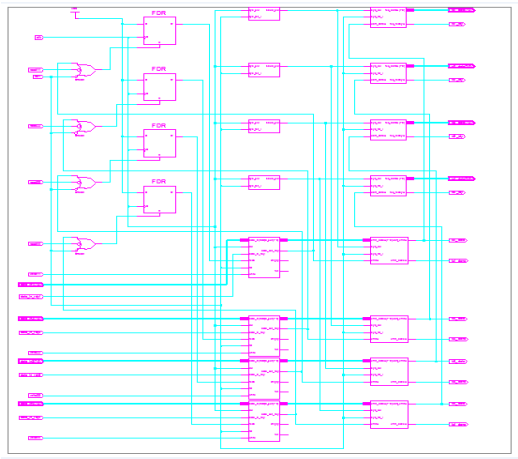

Fig 9 RTL of Multi channel UART

4. ACKNOWLEDGMENTS

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5. CONCLUSION

In this paper, we proposed a design of multi channel UART. It internally consists of baud rate generators, Asynchronous FIFO along with transmitters and receivers. The design is successfully simulated using modelsim software and synthesized using Xilinx software. The results are stable and reliable which shows the correct functionality. Hope this multi channel design meet the modern communication needs. The design has great flexibility, high integration. Because of using FIFO data loss is avoid. In future BIST technology is added to avoid the errors

6. REFERENCES

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