

Design and Optimization of Reversible Multiplier Circuit

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ABSTRACT

The development of conventional computing technologies faces many challenges for the last couple of decades. Power dissipation in today's computer chips becomes dominant. Reversible computing is a promising alternative to these technologies, with applications in ultra-low power, nano computing, quantum computing, low power CMOS design, optical information processing, bioinformatics etc. In reversible logic the power dissipation can be minimized or even eliminated. In this paper, the 4x4 reversible multiplier circuit is proposed with the design of new reversible gate called RAM gate. The proposed multiplier circuit is efficient compared to the existing designs in terms of gate counts, garbage outputs, constant inputs and quantum cost. The design can be generalized to construct nxn reversible multiplier circuit.

KEYWORDS

Reversible logic, Constant/Garbage input, Garbage output, Quantum cost, Reversible multiplier.

1. INTRODUCTION

Power dissipation is an important factor in VLSI design as modern logic circuits offer a great deal of computing power in a small footprint. The combinational logic circuits dissipate heat of $kT \ln 2$ joules [1] for every bit of information erased during computation, where $k = 1.3806505 \times 10^{-23} \text{ J/K}$ is Boltzmann constant and T is the operating temperature in degrees at which the computation is carried out. Also, as Moore predicted that the number of transistors approximately doubles in every eighteen months and if this trend continues to hold, in the near future more and more energy will be lost due to the loss of information. Charles Bennett [2] showed that energy loss could be avoided or even eliminated if the computations are carried out in reversible logic and also proved that circuit built from reversible gates have zero power dissipation. Thus reversible logic appears to be promising in future low power design applications.

Reversible circuits are similar to conventional logic circuits except that they are built from reversible logic gates. In reversible gates, there is unique i.e., one-to-one mapping between the inputs and outputs, which is not the case in conventional logic. Reversible gates are used in quantum computing system as quantum operations are reversible in nature. The reversible circuit/gate has the following characteristics: (i) has equal number of inputs and outputs (ii) the gate output, which is not used as primary output in the circuit is called garbage output (iii) the input which is used as control input to the gates is called constant/garbage input (iv) the fan-out of each gate is equal to one. A copying circuit is

used if two copies of a signal are required and (v) the resulting circuit is acyclic.

An efficient design in reversible logic should have the following features [3]: (a) use minimum number of reversible logic gates (b) should have less number of garbage outputs (c) less number of constant inputs and (d) minimization of quantum cost. Addition and multiplication operations are widely used arithmetic operations in many computations. High speed multiplier circuits are of particular interest in processor design.

Contribution: In this paper, we presented a reversible 4x4 multiplier with the design of new reversible gate called RAM. The proposed multiplier circuit is efficient compared to the existing designs in terms of gate counts, garbage outputs, constant inputs and quantum cost, and this design can be generalized to construct reversible nxn multiplier.

Organization: The paper is organized into the following sections. Section 2 is an overview of basic reversible gates. The background work is described in section 3. Section 4 is about new reversible gate and the proposed multiplier design, results and discussions of the proposed design is presented in section 5 and conclusions are contained in section 6.

2. BASIC REVERSIBLE GATES

The simplest reversible gate is NOT gate and is a 1*1 gate. Controlled NOT (CNOT) gate is an example for a 2*2 gate. There are many 3*3 reversible gates such as Fredkin (F), Toffoli (TG), Peres (PG) and TR gate. The quantum cost of 1*1 reversible gates is zero, and quantum cost of 2*2 reversible gates is one. Any reversible gate can be realized by using 1*1 NOT and 2*2 CNOT reversible gates, such as V, V^+ (V is square root of NOT gate and V^+ is its hermitian) and Feynman gate which is also known as CNOT gate. The V and V^+ quantum gates have the property given in the Equations 1, 2 and 3.

$$V * V = \text{NOT} \dots\dots\dots (1)$$

$$V * V^+ = V^+ * V = I \dots\dots\dots (2)$$

$$V^+ * V^+ = \text{NOT} \dots\dots\dots (3)$$

The quantum cost of a design using reversible logic is calculated by counting the number of V, V^+ and CNOT gates.

2.1 NOT Gate



Figure 1. NOT gate

The reversible 1*1 gate is NOT gate with zero quantum cost is as shown in the figure 1.

2.2 Feynman / CNOT Gate

The reversible 2*2 gate with quantum cost of one having mapping input (A, B) to output ($P = A$, $Q = A \oplus B$) is as shown in the figure 2.

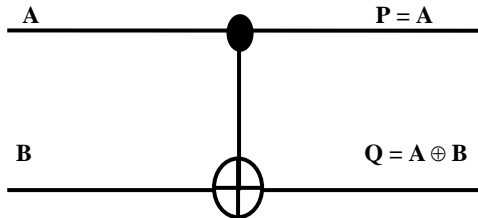


Figure 2. Feynman/CNOT gate [4]

2.3 Toffoli Gate

The 3*3 reversible gate with three inputs and three outputs. The inputs (A, B, C) mapped to the outputs ($P = A$, $Q = B$, $R = A.B \oplus C$) is as shown in the figure 3.

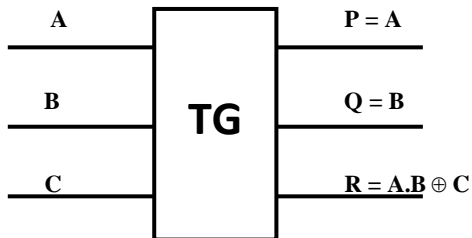


Figure 3. Toffoli gate

Toffoli gate [5] is one of the most popular reversible gates and has quantum cost of five. It requires two V, one V^+ and two CNOT gates. Its quantum implementation is as shown in figure 4.

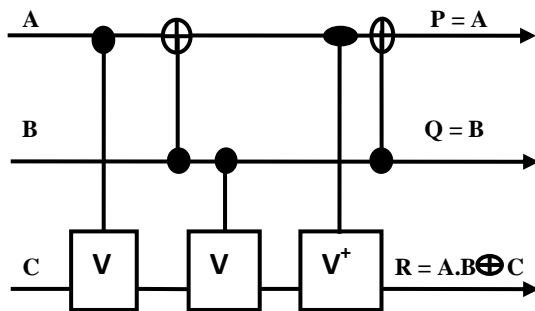


Figure 4. Quantum implementation of Toffoli gate

2.4 Fredkin Gate

Reversible 3*3 gate maps inputs (A, B, C) to outputs ($P = A$, $Q = A^1B + AC$, $R = AB + A^1C$) having quantum cost of five and it requires two dotted rectangles, is equivalent to a 2*2 Feynman gate with quantum cost of each dotted rectangle is one, one V and two CNOT gates.

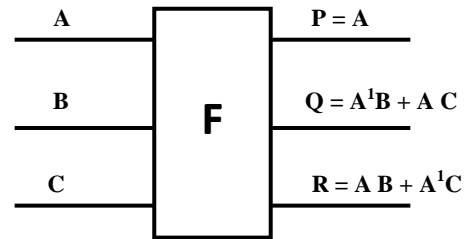


Figure 5. Fredkin gate

Fredkin gate [6] and its quantum implementations are shown in figure 5 and 6 respectively.

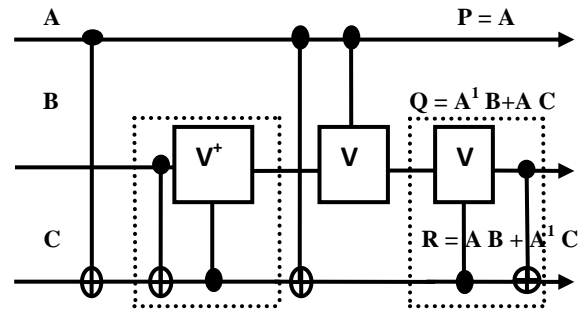


Figure 6. Quantum implementation of Fredkin gate

2.5 Peres Gate

The three inputs and three outputs i.e., 3*3 Reversible gate having inputs (A, B, C) mapping to outputs ($P = A$, $Q = A \oplus B$, $R = (A.B) \oplus C$). Since it requires two V^+ , one V and one CNOT gate, it has the quantum cost of four. The Peres gate [7] and its quantum implementation are as shown in the figure 7 and 8 respectively.

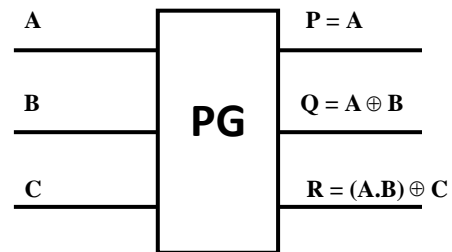


Figure 7. Peres gate

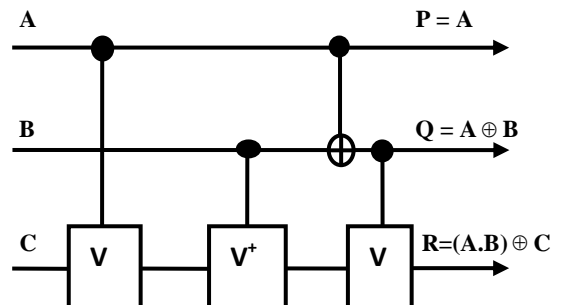


Figure 8. Quantum implementation of Peres gate

2.6 Double Peres Gate

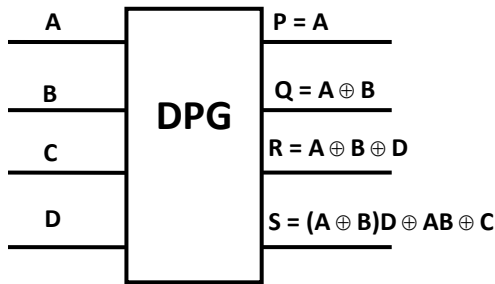


Figure 9. Double Peres gate

The 4x4 reversible gate with four inputs and four outputs. The inputs (A, B, C, D) mapped to ($P = A$, $Q = A \oplus B$, $R = A \oplus B \oplus D$, $S = (A \oplus B)D \oplus AB \oplus C$) is as shown in figure 9.

The DPG has a quantum cost of six as it requires three V, one V^+ and two CNOT gates and its implementation is as shown in figure 10.

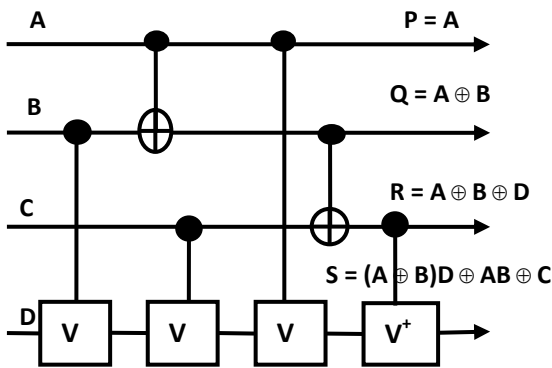


Figure 10. Quantum implementation double Peres gate

The Double Peres Gate (DPG) [8] alone can be used as reversible full adder. The full adder function is realized by using input C as control input i.e., logical low and D input as C_{in} input of the full adder. With inputs (A, B, 0, C_{in}) mapped to the outputs ($P = A$, $Q = A \oplus B$, $R = A \oplus B \oplus C_{in}$, $S = (A \oplus B)C_{in} \oplus AB$) is as shown in figure 11. Here outputs P, Q are garbage outputs and R, S are sum and carry outputs of the full adder respectively.

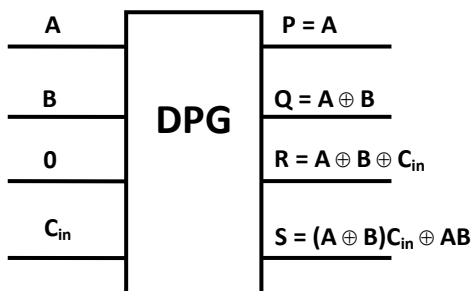


Figure 11. DPG as full adder

2.7 TR Gate

The gate has three inputs and three outputs having inputs (A, B, C) mapped to the outputs ($P = A$, $Q = A \oplus B$, $R = (A \cdot B^1) \oplus C$). TR gate is shown in figure 12.

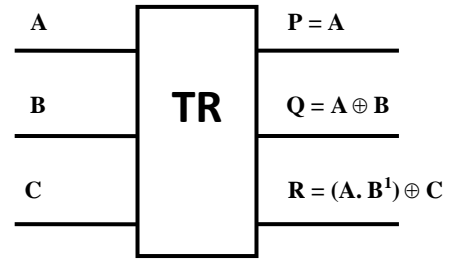


Figure 12 TR gate

The quantum cost of TR gate [9] can be estimated by realizing from two controlled V gates, one CNOT gate, and one controlled V^+ gates resulting quantum cost of four and the quantum implementation is shown in figure 13.

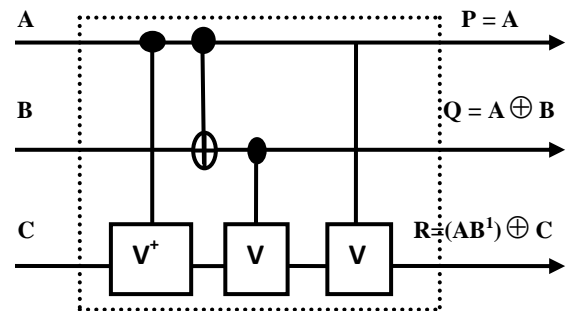


Figure 13. Quantum implementation of TR gate

3. BACKGROUND WORK

Himanshu Thapliyal and Srinivas [13] proposed an $N \times N$ reversible multiplier using TSG gate. In this the partial products are generated using Fredkin gates and addition using reversible parallel adder designed from TSG gates and demonstrated that the multiplier architecture using TSG gate is optimized. Majid Haghparsat et al., [14] presented two new 4x4 bit reversible multiplier designs which have low hardware complexity, less garbage input/output bits and less quantum cost and implementation of reversible HNG is also presented. Noor Muhammed Nayeem et al., [15] explained the use of reversible logic for designing the Arithmetic Logic Unit of a crypto processor. A reversible carry save adder using modified TSG gates and architecture of Montgomery multipliers are also discussed. Maryam Ehsanpour et al., [16] explored the reversible 4-bit binary multiplier circuit using new reversible device called modified full adder with low hardware complexity, fewer garbage outputs and constant inputs.

Sebastian Offermann et al., [17] presented synthesis of multiplier circuits in reversible logic and three methods are discussed to address the drawback of the previous approaches. Fateme Naderpour and Abbas Vafaei [18] proposed the reversible multiplier with decreasing the depth of the circuit by reducing quantum cost and garbage outputs. Anindita Benerjee and Anirban Pathak [19] presented the reversible multiplier design which has two components, reversible partial product generation circuit and reversible parallel adder circuit to minimize number of garbage output bits, gate count and quantum cost. Nidhi Syal and Sinha [20] presented a 4x4 universal reversible parity preserving reversible logic gate which matches the input parity with the output parity. It can be used to synthesis any given Boolean function and offers

less hardware complexity and improved parameter efficiency.

Himanshu Thapliyal and Nagarjan Ranganathan [21] proposed a design of reversible BCD adder which is primarily optimized for the number of input bits and number of garbage outputs, results in the reduction of quantum cost and the delay. Himanshu Thapliyal and Nagarjan Ranganathan [22] presented the design of the reversible half and full subtractor based on the quantum gate implementation of the reversible TR gate. The reversible half and full subtractor shown better in terms of the quantum cost, delay and minimum number of garbage outputs. Michael Nachtigal et al., [23] presented the reversible floating-point adder that follows the IEEE 754 specification for binary floating-point arithmetic. Majid Haghparsat et al., [24] proposed 4x4 bit reversible multiplier circuit, is faster and has lower hardware complexity. The use of reversible gate to construct multiplier is presented.

4. PROPOSED MULTIPLIER DESIGN

4.1 The Proposed 4x4 Reversible RAM gate

The proposed 4X4 reversible gate called RAM gate is shown in figure 14. The inputs (A, B, C, D) mapped to outputs (P = A, Q = A ⊕ B, R = A ⊕ B ⊕ C, S = A ⊕ B ⊕ C ⊕ D). The RAM gate is mainly useful in copying the signal as reversible logic has a fan-out of one.

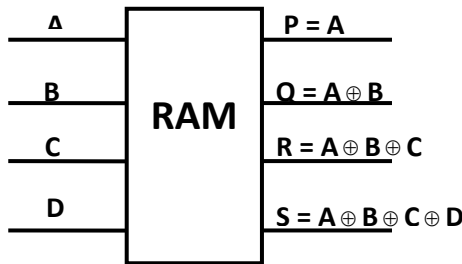


Figure 14. RAM gate

4.2 Reversible Multiplier Design

A reversible 4x4 multiplier circuit has two parts: Partial Product Generation (PPG) circuit and Multi-Operand Addition (MOA) circuit. The details of these two parts are discussed in the following sections:

The RAM gate quantum implementation is shown in figure 15. It has a quantum cost of three as it requires three CNOT gates and by making B, C and D inputs as logical *low* i.e., control input, then the input signal A is copied at all the four outputs as shown in figure 16.

Hence it is useful in partial product generation circuit of reversible multiplier circuit.

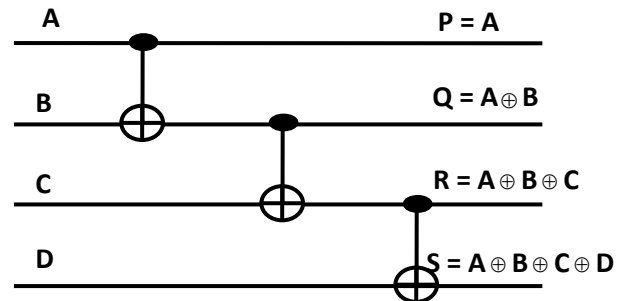


Figure 15. Quantum implementation of RAM gate

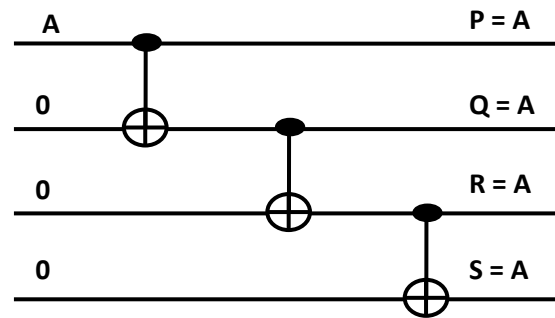


Figure 16. RAM gate as copying circuit

4.2.1 Partial Product Generation

The basic operation of 4x4 parallel multiplier is depicted in figure 17. It consists of sixteen partial products of the form $X_i \cdot Y_j$, where i vary between 0 and 3.

				X3 Y3	X2 Y2	X1 Y1	X0 Y0
				X3.Y0	X2.Y0	X1.Y0	X0.Y0
				X3.Y1	X2.Y1	X1.Y1	X0.Y1
				X3.Y2	X2.Y2	X1.Y2	X0.Y2
				X3.Y3	X2.Y3	X1.Y3	X0.Y3
Z7	Z6	Z5	Z4	Z3	Z2	Z1	Z0

Figure 17. The basic operation of 4x4 parallel multiplier

The PPG circuit using Peres and RAM gates is as shown in figure 18. Here sixteen PG gates are used to generate sixteen partial products as shown in figure 17. The RAM gate is used

as a copying gate, for each X_i input four copies are generated and totally sixteen input signals are copied using four RAM gates as shown in figure 18.

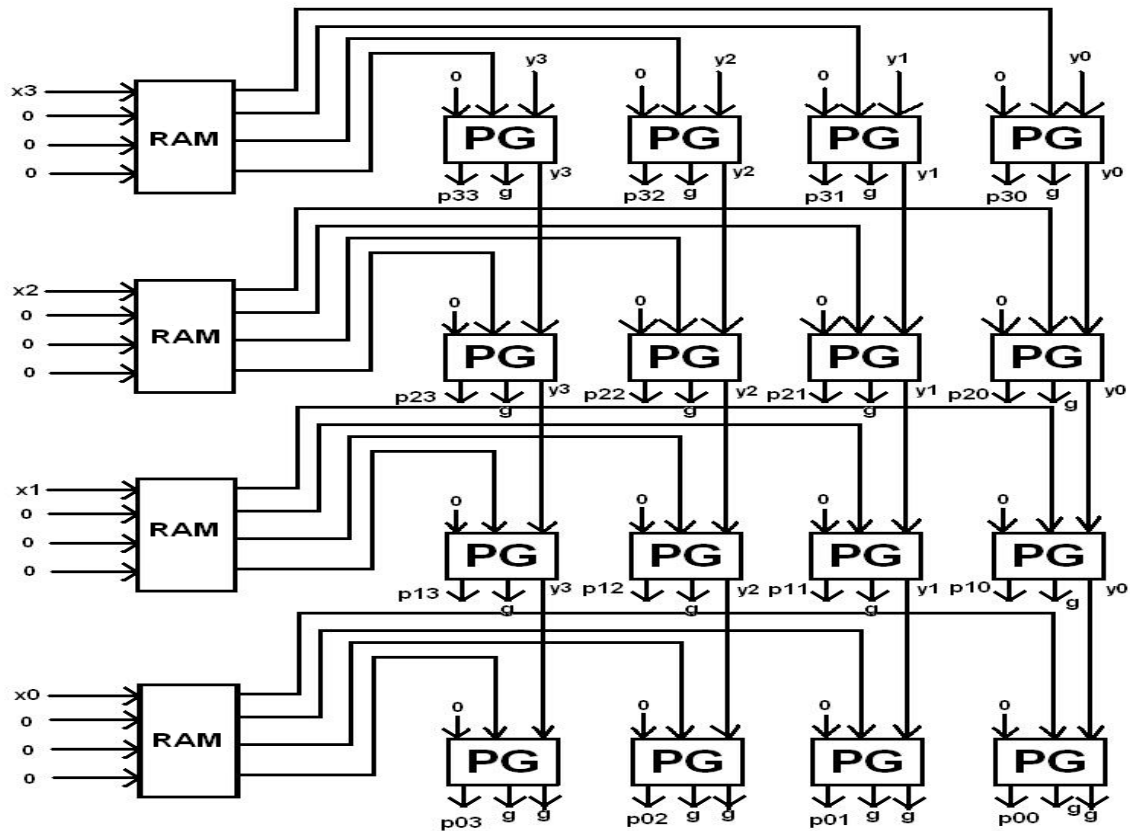


Figure 18. Proposed reversible partial products generation circuit using Peres and RAM gates

4.2.2 Multi-Operand Addition

The addition of the partial products using DPG and PG gates is as shown in figure 19. The basic cells for such a multiplier is full adder using DPG with three inputs and one constant

input, two garbage outputs and half adder using PG with two inputs and one constant input, one garbage output.

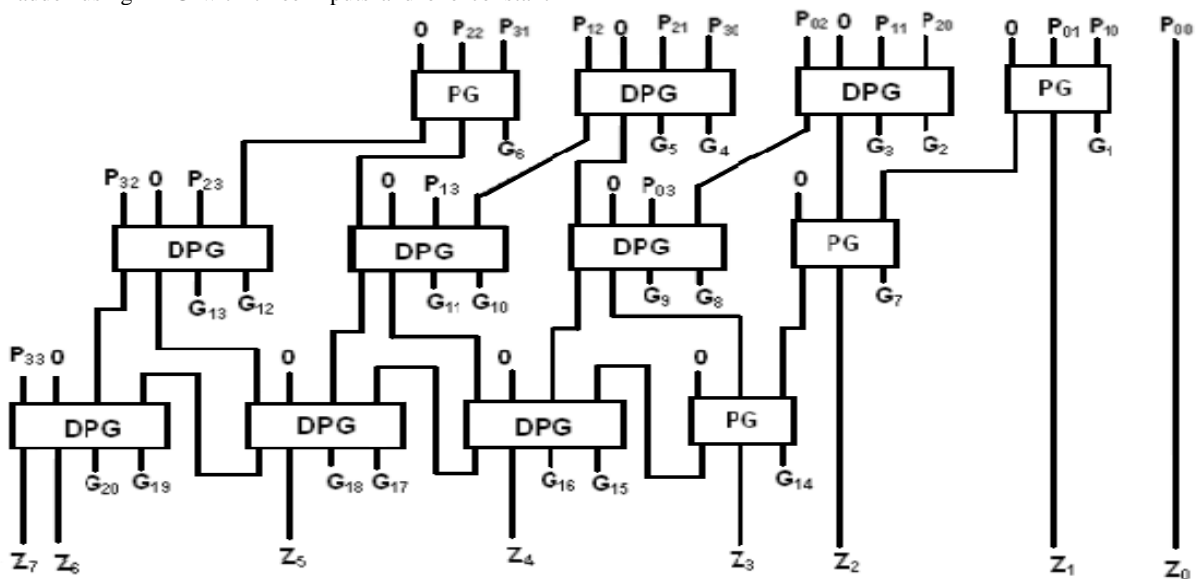


Figure 19. Reversible multi-operand addition circuit

The proposed reversible multiplier circuit uses eight DPG gates, four PG gates, sixteen PG gates for partial product generation and four RAM gates for fan-out creation. It is possible use FG gate as copying circuit, but it requires twelve FGs instead of four RAM gates and by using RAM gate the hardware complexity and garbage outputs are reduced.

5. RESULTS AND DISCUSSIONS

Gate Count/Hardware Complexity: one of the major factors of a circuit is measured in terms of number of gates. It can be proved that the proposed circuit is better than the existing approaches in terms of hardware complexity. In [10], the total number of reversible gates required is 40, [11] requires 42 and in [12] total number of gates required is 44. The proposed reversible multiplier design requires 32 gates. Therefore, the hardware complexity of the proposed design is less compared to the existing approaches.

Quantum Cost: The detailed cost of a reversible gate depends on the realization of quantum logic. Several reversible gates have been realized in quantum technology, among which are FG, PG and DPG. The reversible 4X4 RAM gate is proposed and used as copying gate for fan-out creation in partial product generation circuit, which reduces quantum cost of the design. The quantum cost of the design is 140. The existing design [10], [11] and [12] has the total quantum cost of 152, 136 and 160 respectively. Therefore the proposed design has better in terms of quantum cost compared to the existing designs [10] and [12].

Garbage Inputs: Number of constant inputs is one of the main factors in designing a reversible logic circuit. The input used as a control input by connecting to logical low or logical high to get the required function at the output is called garbage/constant input. The proposed reversible multiplier circuit requires 40 constant inputs, but the design in [10], [11] and [12] requires 52, 42 and 44 respectively. So, it is clear that our design approach is better than existing designs in terms of constant inputs.

Garbage Outputs: the output of the reversible gate that is not used as a primary input or as input to the other gates is referred as garbage output. Optimizing garbage outputs is one of the other main constraints in designing reversible logic circuit. The proposed reversible multiplier circuit produces 40 garbage outputs, but the design [10], [11] and [12] produces 52, 49 and 52 garbage outputs respectively. Therefore, it is clear that design is better than the existing counterparts in terms of number of garbage outputs.

From the above discussion, it is evident that the proposed reversible multiplier circuit is better than the existing designs in terms of gate counts, quantum cost, garbage inputs and garbage outputs.

Evaluation of the proposed reversible multiplier circuit:

The proposed reversible multiplier circuit is more efficient compared to the existing circuits presented by [10], [11] and [12]. This can be comprehended easily with the help of the comparison results shown in table 1.

Table1. Comparison of existing and proposed reversible multiplier designs

	Number of gates	Garbage inputs	Garbage outputs	Quantum cost
[10]	40	52	52	152
[11]	42	42	49	136
[12]	44	44	52	160
Proposed	32	40	40	140

The difference between proposed and existing design is mainly in the partial product generation block. In our design, a new RAM gate is used to create fan-out instead of Feynman gate in the existing designs. By using RAM gate the quantum cost and garbage outputs are reduced. It is clear from figure 20 that the proposed reversible multiplier circuit is better than the existing designs in terms of number of gates, quantum cost, garbage inputs and garbage outputs.

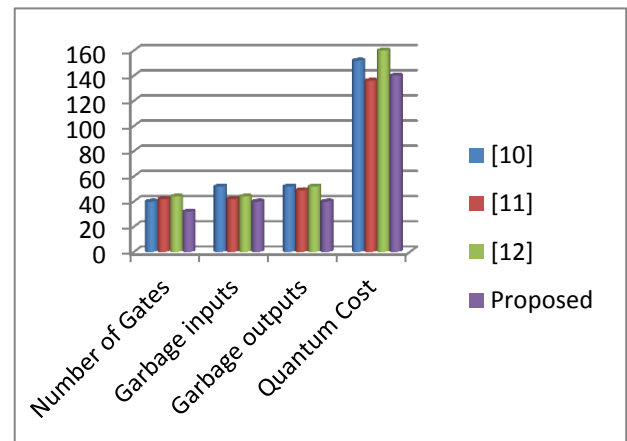


Figure 20. Comparison of proposed and existing reversible multiplier designs

6. CONCLUSIONS

In this paper, design of the 4x4 reversible multiplier circuit with new reversible RAM gate is presented. The design is based on the useful properties of PG, DPG and RAM gate suitable for multiplier operation. The RAM gate is useful in PPG circuit as copying circuit, reduces the number of gates and garbage outputs. The number of gates, garbage inputs, garbage outputs and quantum cost are analyzed. It is seen that number of gates, garbage inputs, garbage outputs and quantum cost values are less in the proposed design compared to the existing approaches. The design can be extended to construct nxn reversible multiplier circuit.

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