The Performance and Analysis of an Efficient Model of DC to DC Converter for on Chip Circuitry using a Less Number of Power Devices

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ABSTRACT

This paper presents an efficient DC to DC converter for on chip circuitry which gives high-energy conversion quality using CMOS Driver-Receiver Pair for Low-Swing Signaling. The efficiency has increased due to the use of power FETs, which are able to switch at high frequency more efficiently than power bipolar transistors, which incur more switching losses and require a more complicated drive circuit. The proposed schemes perform better than the other schemes in terms of power consumption, delay, and energy delay product. Moreover, the proposed scheme requires no reference voltages, and multiple threshold voltage processes. In addition the other key advantages of the proposed signaling schemes is that they require only one power supply and threshold voltage, hence significantly reducing the design complexity. This proposed work also takes care of the relative reliability benefits of the proposed signaling techniques through a signal-to-noise ratio (SNR) analysis.

Keywords

Complementary metal oxide semiconductor (CMOS), Signal to noise ratio (SNR), Threshold voltage, Buck converter.

1. INTRODUCTION

In Electrical Engineering, power conversion has a more specific meaning, namely converting electric power from one form to another. Power conversion systems often incorporate redundancy and voltage regulation. DC to DC converters are important in portable electronic devices such as cellular phones and laptop computers, which are supplied with power from batteries primarily. Buck converters are commonly used as efficient voltage regulators in most miniature portable consumer electronics like mobile phones, PDAs, and multimedia players. There is an increasing trend to use digital controllers over analog ones to control the buck converter in those applications. Because of the ever-decreasing sizes of those devices, it is very desirable to integrate the buck converter controllers with the digital system that is being regulated [1]. The digital controllers make this possible and easier. A typical product development cycle for consumer electronics devices is about six months shorter than the IC suppliers' cycle to deliver the underlying circuitry for these products . Therefore, the reprogram ability of the digital controllers can shorten the development time by programming the digital controllers according to the specification for different products. Several digital current-mode controllers (DCMCs) for buck converters have been successfully demonstrated in recent re- search. In a FPGA-based peak-current-mode digital controller is demonstrated to control a no isolated point-of-load (POL) converter with 20 A loading current. Similarly, shows a FPGA-based average-current-mode digital controller for con- trolling a 10 A synchronous buck converter. These two DCMCs are designed for high-current applications with off-chip power MOSFETs. In contrast, another paper aims to demonstrate a peak-current-mode digital controller for a 500 mA low-power buck converter used in battery-powered products.

2. LITERATURE SURVEY

The research is mainly based on Adaptive processor, energy efficient, low power and variable voltage. In this study we have also seen variety of microprocessor systems which are portable electronic devices. When we vary the supply voltage and clock frequency for the microprocessor system then how these systems works? This also we have discussed in given study. Key design objectives for the processor systems in these applications are given that the maximum possible peak performance for the compute-intensive code like handwriting recognition or image decompression during maximizing the battery life for the lasting low performance time. One more important factor of this paper is DVS means dynamic voltage scaling which can be defined as the strategy that achieves the uppermost promising energy efficiency for time-changing computational loads. At the end of this study the prototype processor system explains that DVS may get better the energy efficiency of battery-powered processor systems with the help of the factor of 10x without losing peak throughput [1].

This research is mainly based on concept f multilevel converter which is firstly invented in 1975. Then after that multilevel power converter has been a projected solution to increase output voltage level in the last recent years. The problems faced to use of multilevel power converter are majorly discussed in this paper.

The major problems of these types of devices as high power applications are also measured. Thus this project is desirable to present low cost converters appropriate for high power applications. One other point is also covered in this study which is Reactive power. Furthermore a procedure for calculating the necessary ratings for the active switches, clamping diodes, and dc link capacitors with a design example has been discussed in our study. It should be prominently underlined that this paper could not cover all the multilevel power converter associated applications, however the essential principles of dissimilar multilevel converters have been demonstrated systematically. The main intention of this research is to make available a universal concept to readers who are concerned in multilevel power converters and its applications [2].

In this study we are mainly concentrating on digital pulse-width modulator i.e. DPWM and digital pulse-frequency modulator i.e. DPFM. Here all the processes we have implemented in CMOS. We have seen in this study that how Digital control of low-power switching converters permits

several settlement including the capacity to use digital design tools, stiffness in moving to various implementation technology and low sensitivity on external influences as well? In this research we initiate a fresh technology that is DPWM/DPFM controller which can be used in low-power "Switched mode power supply" and effortlessly moved from a implementation technology to some another. This scheme also assembles the necessities of very high frequency of operation in DPWM mode as well as very low power consumption in the DPFM which is needed for low-power portable and handheld devices. One experiment has also covered in this paper which explains operations at a very high steady switching frequency of 6.2 MHz, and helpful voltage regulation in DPFM operation as well [3].

Today frequency control technique is very challenging and developed in global scale. We will discuss about the digital three phase full bridge dc\ac power inverter which tells about the frequency control technique. There were so many challenging efforts in the field of communication speed in past few days, so an efficient technique is discovered i.e frequency control technique which helps in managing the communication speed between components. To achieve high speed, simple control system configuration, and low cost, a new on-chip all digital three-phase dc/ac power inverter using feed forward and frequency control techniques is proposed. The digital three-phase full-bridge dc/ac power inverter is an instrument that is implemented by a six series-resonant parallel-loaded configuration with a model of motor, a controller, and a buffer chain. The proposed power inverter, called the shift register, consists of six-stage D-latch flip-flops and developed with MOSFET technology with a goal of achieving low-power consumption and area efficiency. By applying the MOSFET technology containing shift register, use variable frequency for controlling the clock and data signal. To ensure stability, the frequency of CK must be six times higher than that of D. The operation frequency of the proposed power inverter ranges from 10 Hz to 2 MHz, and the maximum output loading current is 0.8 A. From the simulated and experimental results, the proposed power inverter has yielded excellent functionality in terms of wide operation frequency range, simple operation, all-digital control, and system-on-chip because of its ability to convert the dc supply voltage into the three-phase ac power sources [4].

Today Multiphase machine drives have unbiased significant interest among researchers in recent years because of its inherent features. We will discuss about the presents certain sequential switching hybrid modulation strategies, and compared for the multiphase multilevel inverters. Hybrid modulation represents the combination of fundamental frequency, and multilevel sinusoidal modulations which is designed for performance of the alternative phase opposition disposition, phase shifted carrier, carrier-based space vector modulation and single-carrier sinusoidal modulations. The main characteristic of these modulations are the reduction of switching losses with good harmonic presentation. A hybrid modulation contains simple sequential switching and base pulse-width modulation (PWM) techniques to achieve balanced power dissipation. Hybrid modulation device is the series of connected cells with equal load sharing and balanced DC-link capacitor voltages. Many new modulation techniques have been developed to cater the growing number of MLI topologies. They are aimed at generating a stepped switched waveform with adjustable amplitude, frequency and phase fundamental component that is sinusoid at steady state. The multilevel sinusoidal PWM and its base modulation design are implemented on a TMS320F2407 digital signal processor (DSP).The feasibility of these modulations are theoretically analyzed for five level and then generalized for N-level, validated by simulation and confirmed practically for a five-level inverter. The algorithm which is used for the Combinational logic-based HPWM control and HPWM circulation are compact and easily realized with CPLD. It can be easily applied to higher level through the generalization process and implementation [5].

This research is mainly based on some of these terms which are Electrostatic analysis, packaging, power-chip on-chip approach, power/drive interaction, press-pack implementation, and radiated field. At the same time we are concentrating on new generation of power modules and we have also tried to optimize the tradeoff between the thermal and electromagnetic interference managements. In this study we have also discussed the uniqueness and benefits of bus-bar-like power module. The configuration of the module is based on the PCoC conception that is used here in order to divide the link in between the electrical and thermal managements, which is trying to take benefit of the third dimension. After that we moved to the realization and the assembly of the structure which is nicely covered under this study. Additionally, the power module is likely to present a tremendously reduced switching cell inductance because a function of the assembly technology. Eventually, the 3-D assembly measured in this paper allows confining conducted general mode EMI in a simple manner. All the clarifications are validated d because of practical experiments [6].

Digital current-mode control is more favorable than voltage-mode control is a dual-loop control which potentially results in a better transient response. Many proposals have been made for the design and Implementation of Fully Integrated Digitally Controlled whose on-chip implementation is very challenging, especially for current-mode control. Among all the challenges one of the main challenge is to efficiently sample and quantize both the output voltage and inductor current of the buck converter for control purposes. BUCK converters have wide application in most miniature portable consumer electronics like mobile phones, PDAs, and multimedia players as efficient voltage regulators. Here the proposed converter uses a time-multiplex scheme (TMS) for the control-loop to demonstrate how the DCMC controls the buck converter by using a single TM-ADC for quantizing both the output voltage and the inductor current. A modified delay-lock-loop DPWM has been developed for minimizing the mismatch of the delay-cells. A low power and small chip area TM-ADC is designed for the TMS and integration purposes. This not only saves one ADC static power but also requires less chip area [7].

Ultra-low-power operation is very important in battery-powered medical devices for enabling advanced signal processing algorithms. Such operation requires innovation in all aspects of the design of integrated circuits including architecture, circuit design, and process selection. This paper presents an embedded processor platform chip using an ARM Cortex-M3 suitable for mapping medical applications requiring microwatt power consumption. It has been proposed that by using a novel system architecture with a 100-nJ FFT accelerator, a fully differential 0.5-V 6T SRAM, and a 90% efficient DC-DC converter, it shows the first sub-microwatt per channel electroencephalograph (EEG) seizure detection [8].

In this paper, a new power converter topology is presented. This novel multilevel competitive topology is very effective as it uses relatively less number of capacitors and

semiconductor devices compared to existing topologies, thereby avoids bulky installations. The novel topology can be seen as asymmetric flying capacitors or packed U cells. Each U cell consists of two power switches and one capacitor. It gives high-energy conversion quality using a comparatively less number of capacitors and power devices and consequently, has a very low production cost. The control approach has been designed to decrease the harmonic stuffing of the load voltage. With such converters, filters' rating is considerably reduced [9].

In the year of 2011, the study is mainly based on dc-dc converter. Now days the linear regulators can only output at lower voltages from the input. They are very inefficient when the voltage drop is large and the current is high as they dissipate heat equal to the product of the output current and the voltage drop; consequently they are not normally used for large-drop high-current applications. The digitally controlled current-mode buck converter is more favorable for portable consumer electronics if it is highly integrated as shown in Fig. 1. For example, the buck converter, including DCMC and power MOSFETs, should be fully integrated into a single silicon chip. However, all the aforementioned papers only verify their digitally controlled current-mode converters design through FPGAs/CPLD implementation. There are different design considerations between FPGAs and fully IC implementations. Therefore, this paper addresses the challenges and design considerations of implementing a fully integrated digitally controlled current-mode buck converter.

3. OPERATING PRINCIPLE OF TM-ADC

The schematic of the 4-bit TM-ADC with an on-demand clock is depicted in Fig.3. Although the TM-ADC is based on the same principle of successive approximation to do the analog-to-digital conversion, its implementation is different from basic ADC techniques. Some modifications have been made for the design of the controller in this paper. One is that two set of reference voltages are needed for two different phases of quantization. One (high, vow) is for output voltage quantization and the other (high, low) is for inductor current quantization. In this case, the successive approximation register (SAR) needs to switch the references according to the TMS mentioned in Fig. 3. Since the upper and lower bound reference voltages are used, the TM-ADC is actually a "window" ADC [1], which means the ADC is only linear within the "window." This kind of "window" ADC provides a fine resolution while maintaining low power consumption. Because of the bipolar supply used in [1] those SA-ADCs can obtain the digital code by comparing the sam- pled voltage to the virtual ground. However, bipolar supply is often unavailable in portable consumer electronics, which use batteries as the only source of power. This leads to another modification of those SA-ADCs. The TM-ADC shown in Fig. 5 is implemented using a single supply only. The generation of the digital code is then done by comparing a predefined DC voltage at the node as shown in Fig. 5. To ensure the high power efficiency of the buck converter, the power MOSFETs sizing design is important. As a general guideline, it is assumed that the switch resistances of power MOSFETs are 1% of the load resistance. Since the power MOSFETs are operating in the linear region for most of the time, we have the following linear equations for the MOSFETs to estimate the switch resistance of the p-type power MOSFET and the n-type power MOSFET

$$R_{PMOS} = \frac{1}{\mu_p C_{nx} \left(\frac{W}{L}\right)_p (V_{gS} - V_{tn})}$$

$$R_{NMOS} = \frac{1}{\mu_p C_{nx} \left(\frac{W}{L}\right)_n (V_{gS} - V_{tn})}$$

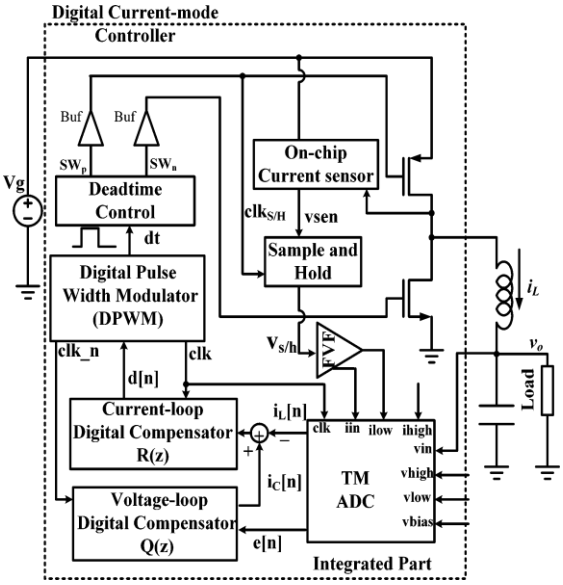

Fig.1. Block diagram of the digitally controlled current-mode buck converter with a single TM-ADC

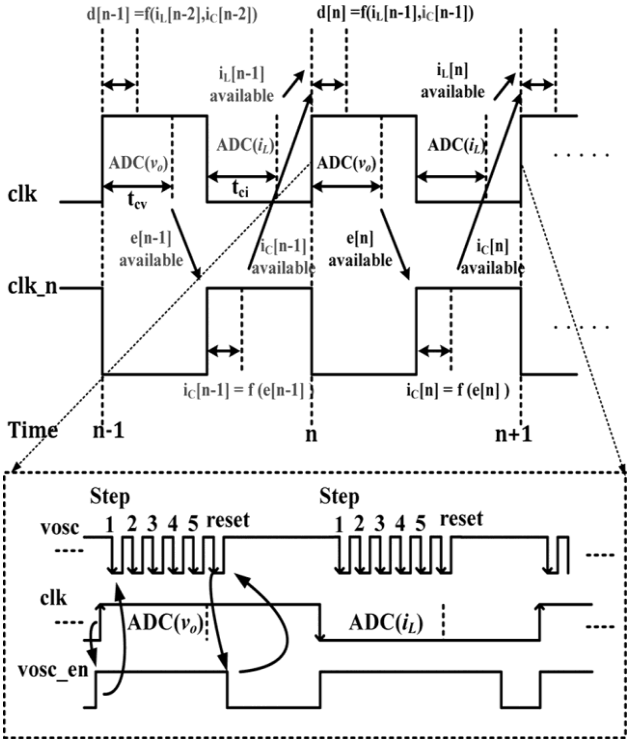

Fig. 2. Time-multiplex scheme for the DCMC

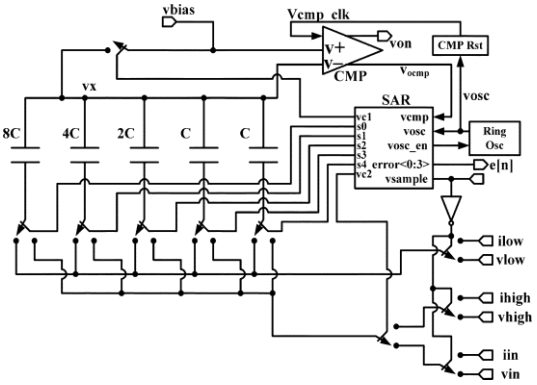

Fig. 3.Schematic of 4-bit time-multiplex ADC

By simulations, both the sizing of the n-type and p-type power MOSFETs are optimized for a heavy load condition, i.e., 500 mA loading current. After optimizing the switching resistance of the power MOSFETs, a dead time circuit, that to preclude any shoot-through current, is also important for ensuring high power efficiency. The dead time circuit makes sure that both n-type and p-type power MOSFETs are not turned on at the same time, i.e., there is a time that the both MOSFETs are off (dead time). Although some advanced dead time controls are available, a simple SR latch implementation has been chosen for the controller in this paper as shown in Fig.4.

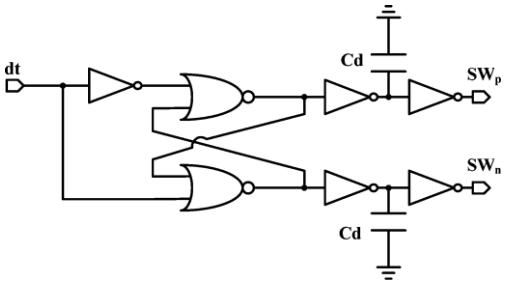

Fig. 4. Dead time circuit

4. COMMON LOW POWER PWM

Delay-line DPWM is commonly used in low-power digital PWM controller because of its low power and small chip area. For example shows one of the 8-bit delay-line DPWM implementations as shown in Fig.5. This DPWM has the advantage of not requiring an external clock and can be implemented on less than one-eighth of the area needed for the conventional ring implementation. The operating principle of the DPWM is to use two branches of delay-line to quantize time into a number of discrete time slots. One branch consists of fast-delay-cells and the other consists of slow-delay-cells. The slow-delay-cells quantize the time into coarse slots and then each coarse slot is further quantized by fast-delay-cells into a fine slot. Then a particular fine time slot is selected by the digital according to the digital word d[n] . The main disadvantage of this DPWM is that it is difficult to match two different types of delay cells, namely, those that are fast and those that are slow. That is, for the 8-bit DPWM in the delay time t_{fast} of one fast-delay-cell has to be exactly equal to 1/16 of the delay time of one slow-delay-cell (t_{slow}) t_{fast}, i.e., $16xt_{fast} = t_{slow}$. Matching all 16 fast-delay-cells to one slow-delay-cell is very difficult to achieve monolithically by simply adjusting biasing current because of process variation and the parasitic layout.

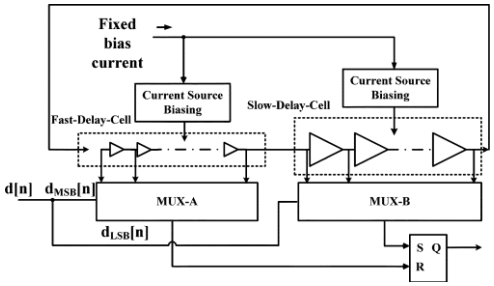

Fig. 5. Common Low Power DPWM.

5. PERFORMANCE CHARACTERISTICS OF DIGITALLY CONTROLLED CURRENT-MODE BUCK CONVERTER

The plot of the power efficiency with different input voltages is shown in Fig. 6. The power efficiency is measured with the output voltage regulated at 1.9 V. The plot of the power efficiency with different output voltages is shown in Fig. The power efficiency is measured with the fixed input voltage at 2.5 V.

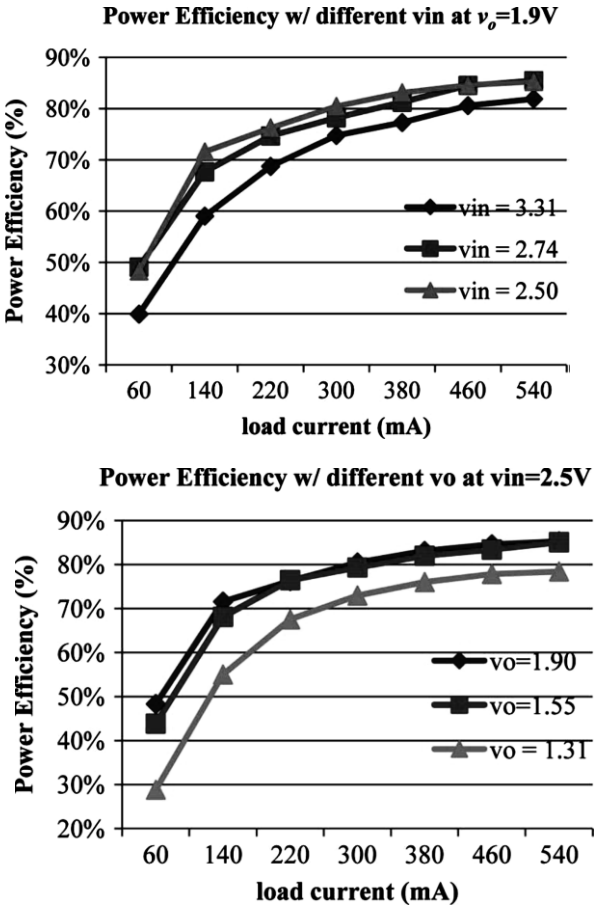

Fig.6.plot of the power efficiency with different input and output voltages.

The highest power efficiency is also close to 85%. However, the 0.35μp process is relatively old compared with others. The 0.35μp process has higher parasitic than the advanced process

like 40 nm or 0.13 µp. The buck converter is fabricated with a standard 0.35µ m CMOS process. It consists of the DLL DPWM, voltage-loop and current-loop digital compensators, the TM-ADC, the memory cells and the 500 mA power MOSFETs. All of them are integrated in a single die with a chip area of 1049µ m 1533µ m. The converter requires no external component except for the LC filter. Measurement results show that the buck converter is stable under different operation conditions. No limit-cycle occurs with the use of a single TM-ADC. The 20µs load transient response time is comparable with the other digitally controlled buck converters. All of these proved that it is possible to use a single TM-ADC for a stable and fast dual-loop digitally controlled converter.

6. DRAWBACK OF DIGITALLY CONTROLLED CURRENT MODE BUCK CONVERTER

One of the main challenges to implementing the converter in Fig. 1 is that two ADCs are required for quantizing the output voltage and the inductor current i_L . Compared to the digital voltage-mode control, the extra ADC requires more chip area and power to operate. Another design challenge is to design a timing scheme such that the single ADC knows when to sample and quantize the output voltage and the inductor current. The timing scheme also needs to make sure that the digitized signals can be sent to both the current-loop and the voltage-loop compensators with the least amount of delay to ensure the stability of the converter shown in Fig. 1.This digitally controlled current Mode Buck Converter have inefficiency wastes power and requires higher-rated and consequently more expensive and larger components. The heat dissipated by high-power supplies is a problem in itself and it must be removed from the circuitry to prevent unacceptable temperature rises. Switched capacitor converters rely on alternately connecting capacitors to the input and output in differing topologies. They are also used at extremely high voltages, as magnetic would break down at such voltages.

7. PROPOSED DC TO DC CONVERTER

To overcome the previous disadvantages we proposed an efficient DC to DC converter for on chip circuitry which gives high-energy conversion quality using CMOS Driver-Receiver Pair for Low-Swing Signaling. The efficiency has increased due to the use of power FETs, which are able to switch at high frequency more efficiently than power bipolar transistors, which incur more switching losses and require a more complicated drive circuit. The proposed schemes perform better than the other schemes in terms of power consumption, delay, and energy delay product. Moreover, the proposed scheme requires no reference voltages, and multiple threshold voltage processes. In addition the other key advantages of the proposed signaling schemes is that they require only one power supply and threshold voltage, hence significantly reducing the design complexity. This proposed work as shown in fig.7 also takes care of the relative reliability benefits of the proposed signaling techniques through a signal-to-noise ratio (SNR) analysis.

8. THE CMOS DRIVER CIRCUIT

The CMOS driver is a pin replacement of the existing bipolar circuit The CMOS driver is may fabricate in CMOS technology as shown in fig.8 and therefore has an inherent advantage over the bipolar line driver in terms of current consumption. Under worst case static conditions. In comparison with the line driver, a current consumption reduction to 500 µA max to 25 mA may be achieved. If we are using RS-232C specification states that the required driver output voltage is defined as being between +5V and +15V and is positive for a logic "0" (+5V to +15V) and negative for a logic "1" (−5V to −15V). These voltage levels are defined when driver is loaded 3000 ohm < RL < 7000ohm. The driver meets this voltage requirement by converting TTL/LSTTL levels into RS-232C levels through one stage of inversion.

The RS-232C specification further states that, during transitions, the driver output slew rate may not exceed 30V/µs. The inherent slew rate of the equivalent bipolar circuit DS1488/MC1488 is much too fast and requires the connection of one external capacitor (330–400 pF) to each driver output in order to limit the slew rate to the specified value. However the driver does not require any external components. This has a novel feature in that unique internal slew rate control circuitry has been incorporated which eliminates the need for external capacitors; to be precise, a saving of four capacitors per package. The driver minimizes RFI and transition noise spikes by typically setting the slew rate at 5V–6V/µs. This will enable optimum noise performance, but will restrict data rates to below 40k baud. The driver can also withstand an accidental short circuit from a conductor in the interconnecting cable to any one of four outputs in a package without sustaining damage to itself or its associated equipment.

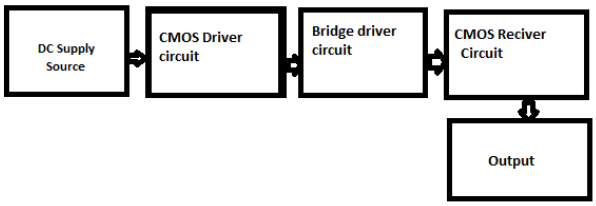

Fig.7. Example circuit structure for CMOS Driver Receiver

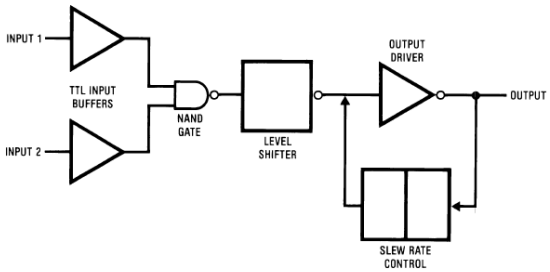

Fig.8.Model Driver Block Diagram

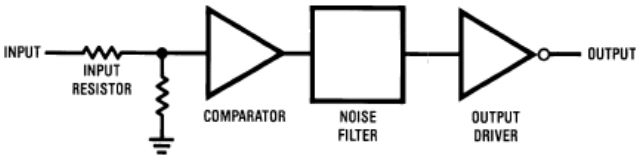

Fig .9. Model Receiver Block Diagram

System Parameters								
Technology	0.35µ	0.18µm	40nm	0.5µm	0.25µm	N/A	N/A	N/A
Voltage and Current mode	Current mode	voltage mode	voltage mode	voltage mode	voltage mode	Current mode	Current mode	Current mode
Controller: Integrated /FPGA	Integrated	Integrated	Integrated	Integrated	Integrated	FPGA	FPGA	FPGA
Dynamic Parameters								
LOAD STEP	0.05A→0.25A	0A→0.3A	0A→0.25	0A→1A	0.025→0.15	0.46→1.1A	0A→20A	0A→5A
Response Time	20µS	100µS	1ms	100µs	100µs	50µs	20µs	70µs
Static Parameters								
Max. efficiency	85%	94%	94%	N/A	92%	N/A	N/A	N/A
Nominal load	250mA	300mA	200mA	Max.1A	Max.400mA	500mA	Max.20A	10A
Output capacitor	4.7µF	22µF	10µF	22µF	47µF	36µF	5600µA	282µF
Inductor value	2.2µH	18.8µH	2.2µH	1µH	10µH	2.5µH	1.0µH	0.9µH
Switching frequency	2.5MHZ	500KHZ	3.125KHZ	1MHZ	1MHZ	1MHZ	100KHZ	200KHZ
Input voltage	3V	3.3V	3.3V	5V	3.2V	5V	12V	6V
Output voltage	1.5V	1.8V	1.5V	2.7V	1.1V	1.5V	2.5V	1.8V

9. CHALLENGES IN PROPOSED CONVERTER

To regulate the output voltage at all possible input voltage conditions, the device automatically switches from step down operation to boost operation and back as required. It always uses one active switch, one rectifying switch, one switch permanently on, and one switch permanently off. Therefore, it operates as a step down converter (buck) when the input voltage is higher than the output voltage and as a boost converter when the input voltage is lower than the output voltage. There is no mode of operation in which all 4 switches are permanently switching. Controlling the switches this way allows the converter to maintain high efficiency at the most important point of operation, when input voltage is close to the output voltage. The RMS current through the switches and the inductor is kept at a minimum, to minimize switching and conduction losses. The average inductor current is regulated by a fast current regulator loop which is controlled by a voltage control loop. The non-inverting input of the transconductance amplifier Gmv can be assumed to be constant. The output of Gmv defines the average inductor current. The current through resistor RS, which represents the actual inductor current, is compared to the desired value and the difference, or current error, is amplified and compared to the saw tooth ramp of either the Buck or the Boost. The Buck-Boost Overlap Control specifies that the classical buck-boost function, which would cause two switches to be on every half a cycle, is avoided. Because of this block, whenever all switches becomes active during one clock cycle, the two ramps are shifted away from each other. However, when there are no switching activities because there is a gap between the ramps, the ramps are moved closer together. As a result, the number of classical buck-boost cycles or no switching is reduced to a minimum and high efficiency values are achieved. Slope compensation is not required to avoid sub harmonic oscillation which are otherwise observed when working with peak current mode control with D>0.5. The amplified inductor current down slope at one input of the PWM comparator must not exceed the oscillator ramp slope at the other comparator input. This purpose is reached limiting the gain of the current amplifier. Comparison of various CMOS process technology shown TableI.

10. CONCLUSION

The switching power supplies, the layout are an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the converter could show stability problems as well as EMI (Electromagnetic interference) problems. Therefore, we use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC. The feedback divider should be placed as close as possible to the control ground pin of the IC. To lay out the control ground, short traces are recommended as well, separation from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current. The digitally controlled current Mode Buck Converter has inefficiency wastes power and requires higher-rated and consequently more expensive and larger components. The heat dissipated by high-power supplies is a problem in itself and it must be removed from the circuitry to prevent unacceptable temperature rises. To overcome above problem by implement of proposed converter. The challenges and design considerations of implementing a an efficient DC to DC converter for on chip circuitry which gives high-energy conversion quality using CMOS Driver-Receiver Pair for Low-Swing Signaling current-mode buck converter has been addressed and discussed.

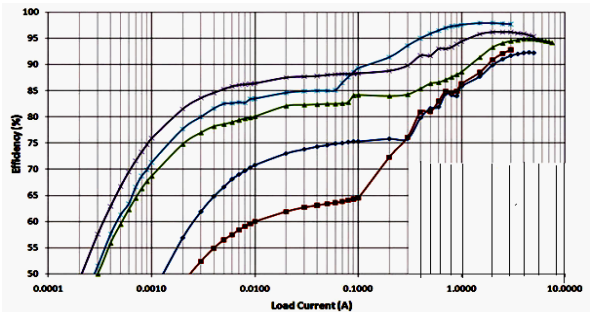

Fig.10.Expected result load current Vs Efficiency

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