Investigation of Fast Switched CMOS Inverter using 180nm VLSI Technology

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ABSTRACT
Inverter is truly the nucleus of electronics industry. It is the main building block of everyday appliances i.e. microwaves, power tools, battery chargers, air conditioners and computers etc. In this paper, CMOS technology has been chosen to study the transient and dc characteristics of an inverter. Feature size is the main parameter to study the voltage transfer characteristics of inverter, for which length and width of transistors is varied. Further, CMOS inverters can be paralleled for increased power to drive higher current loads. Simulations are run on cadence design tool and the schematic diagrams are drawn in virtuoso schematic editor using 180nm technology file.

Keywords
Subthreshold region, Complementary Metal Oxide Semiconductor (CMOS), Feature size, Design Rule Check (DRC), Layout Vs Schematic (LVS).

1. INTRODUCTION
Research efforts in digital electronics mainly have been directed toward increasing speed and complexity of single-chip-based digital systems [1-2]. These efforts have resulted in very-high-speed, sophisticated systems for graphics, video, speech recognition, and other applications. Complementary MOSFET (CMOS) technology is widely used today to form circuits in numerous and varied applications such as image sensors (CMOS sensor), data converters, and highly integrated transceivers for many types of communication. CMOS offers advantages like low power dissipation, relatively high speed, high noise margins in both states, and operates over a wide range of source and input voltages [3].
Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor-transistor logic (TTL) or NMOS logic. CMOS also allows a high density of logic functions on a chip. MOSFETs are continuously scaled to smaller dimensions to reduce the space complexity [4].

The inverter is the base building block of all digital designs. Once its operation and properties are clearly understood, designing more intricate structures such as NAND gates, adders, multipliers, and microprocessors is greatly simplified. The electrical behaviour of these complex circuits can be almost completely derived by extrapolating the results obtained for inverters. The analysis of inverters can be extended to explain the behaviour of more complex gates such as NAND, NOR, or XOR, which in turn form the building blocks for modules such as multipliers and processors [5].

A CMOS inverter is an ingenious circuit, built form a pair of nMOS and pMOS transistors operating as complementary switches. For an ideal symmetric transistor, (W/L) ratio of pMOS transistor is approximately 2.5 times (W/L) ratio of nMOS transistor to compensate the driving current loss in pMOS transistor due to lower hole mobility. The important CMOS properties are high and low output levels i.e. are V_{dd} and 0 respectively. CMOS inverter devices can be used to provide greater complementary current outputs [4].

2. CHARACTERISTICS OF nMOS AND pMOS TRANISTORS
The operation of a MOSFET can be separated into three different modes, depending on the voltages at the terminals. For an n-channel MOSFET, the three operational modes are [5]:
1. Cut-off, subthreshold, or weak-inversion mode, When $V_{GS} < V_{th}$
2. Triode mode or linear region, When $V_{GS} > V_{th}$ and $V_{DS} < (V_{GS} – V_{th})$
3. Saturation or active mode, When $V_{GS} > V_{th}$ and $V_{DS} > (V_{GS} – V_{th})$.
For p-channel MOSFET, the three operational modes are:
1. Cut-off, subthreshold, or weak-inversion mode, When $V_{GS} > V_{th}$
2. Triode mode or linear region, When $V_{GS} < V_{th}$ and $V_{DS} > (V_{GS} – V_{th})$
3. Saturation or active mode, When $V_{GS} < V_{th}$ and $V_{DS} < (V_{GS} – V_{th})$.

2.1 Conventional CMOS Inverter
The circuit diagram of a static CMOS inverter is shown in fig. 2. When V_{in} is high and equal to V_{DD}, the nMOS transistor is on, while the pMOS is off. A direct path exists between V_{out} and the ground node, resulting in a steady-state value of 0 V. On the other hand, when the input voltage is low (0 V), nMOS and pMOS transistors are off and on, respectively. A path exists between V_{DD} and V_{out}, yielding a high output voltage [6].
The main advantage of a CMOS inverter over many other solutions is that it is built exclusively from transistors, which operate as switches, without any other passive elements like resistors, inductors or capacitors.
From fig.1 and fig.2, it is noted that the pMOS (pull-up transistor) is connected between V_{DD} and the output, V_{out}, whereas the nMOS (pull-down transistor) is connected between the output, V_{out} and the ground terminal, GND [7].
The principle of operation is as follows

1. For small input voltages, V_{in}, nMOS transistor is switched off, whereas pMOS transistor is switched on and connects the output node to VDD.

2. For large input voltages, V_{in}, pMOS transistor is switched off and nMOS transistor is switched on and connects the output node to GND i.e. 0V.

A better understanding about the working of CMOS inverter can be obtained by analyzing its transfer and current characteristics [7].

2.2 Transfer Characteristics of transistor

It represents dynamic behaviour of transistor during switching the input signals from low-to-high or high-to-low voltages. It is a graph of output voltage, Vy and input voltage, Vx with respect to time. When input voltage decreases from V_{DD} to 0 Volts, output increases from 0 to V_{DD} Volts. Fig.1 and fig.2 explains this operation.

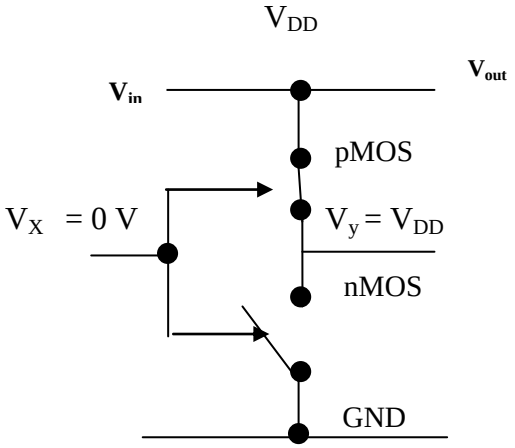

Fig 1: high output of inverter for low input [7]

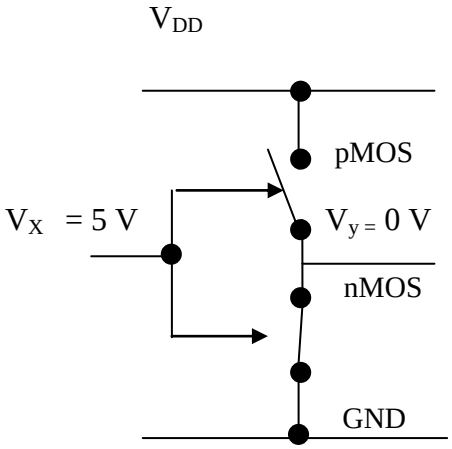

Figure 2: Low output of inverter for high input [7]

In order to build a symmetrical inverter, the midpoint of the transfer characteristic must be centrally located, that is, $V_{in} = 0.5\ V_{DD} = V_{out}$.

2.3 DC Characteristics

It presents output voltage with respect to input voltage of a gate. It also indicates the switching point for a gate. From such a graph, device parameters including noise tolerance, gain, and operating logic-levels can be obtained.

Ideally, the voltage transfer curve (VTC) appears as an inverted step-function - this would indicate precise switching between *on* and *off* - but in real devices, a gradual transition region exists. The VTC indicates that for low input voltage, the circuit outputs high voltage; for high input, the output tapers off towards 0 volts. The slope of this transition region is a measure of quality - steep (close to -Infinity) slopes yield precise switching [8].

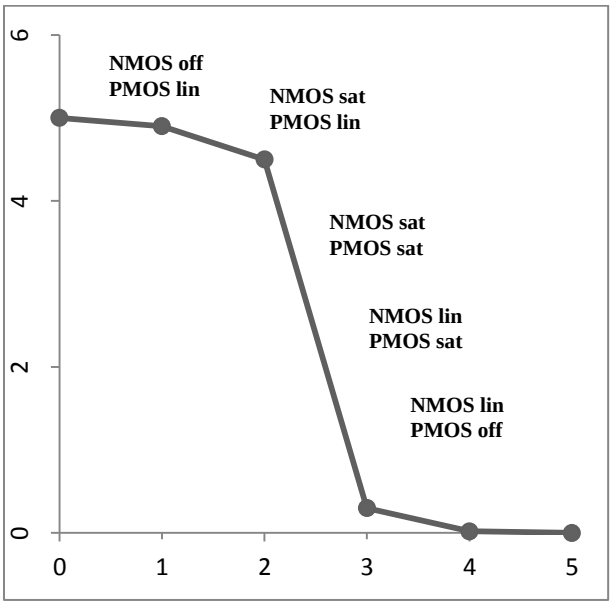

Figure 3: Voltage Transfer Characteristics of CMOS inverter, (where region I indicates nMOS is cut off and pMOS is in linear mode, region II indicates nMOS is in saturation region and pMOS is linear, region III indicates both nMOS and pMOS are saturated, region IV indicates nMOS is linear and pMOS is saturated, region V indicates nMOS is linear and pMOS is cut off [9].

2.3.1 Switching threshold

Switching threshold is defined as where input voltage is equal to output voltage on Voltage Transfer Characteristics (VTC). The switching threshold voltage is an important parameter to characterize the inverter DC performance. Its value can be obtained graphically from the intersection of the VTC with the line given by $V_{in} = V_{out}$. In this region, both PMOS and NMOS are always saturated, since $V_{DS} = V_{GS}$. [5]

3. DESIGN OF CMOS INVERTER

CMOS inverter has been implemented in 180nm technology using cadence design tool. Under this, VIRTUOSO DESIGN ENVIRONMENT is the main path for simulation. This design tool is compatible with RedHat LINUX. In order to create CMOS inverter schematic, nMOS and pMOS transistors with fixed length (180nm) and varying width are selected from the predefined library.

Also, the inverter symbol is created with specifications:

DC voltage source to V_{DD}, $V_{dc}=V_{DD}=1.8V$

Common input pulse to Gate, V_{pulse}, V_1 (low level) =0V, V_2 (high level) = 1.8V,

Period=20ns, Delay=1ns, Rise time,t_r = 10ns, Fall time,t_f = 10ns, Pulse width= 10ns.

Then, simulation is run in analog design environment (ADE L) with given parameters.

To find the transfer characteristics: stop time=200ns. For dc characteristics: sweep range = 0 to 1.8V.

After that, waveforms are plotted.

Similarly, vary the width of pMOS and nMOS transistors, such that (W/L)p is approximately 2 to 3 times of (W/L)n .

As $\beta = (\mu\varepsilon/t_{ox})(W/L)$, [11] (1)

For nMOS, $\beta n = (\mu_n\varepsilon/t_{ox})(W/L)n$, (2)

pMOS, $\beta_p = (\mu_p\varepsilon/t_{ox})(W/L)p$ (3)

In case of (W/L)p=(W/L)n and same oxide thickness and permittivity,

Dividing (2) and (3), we get

$\beta n/ \beta_p = (\mu_n / \mu_p)$

As electron mobility, μ_n is approximately 2 to 3 times mobility of hole, μ_p. Therefore, βn should be 2 to 3 times β_p. For length to be equal, it can be concluded that Wp should be 2 to 3 times Wn for switching threshold to be optimum.

Table 1: Comparison of switching threshold with variation in W/L of pMOS and nMOS transistors for length, L=180nm

Sr. No.	pMOS width, Wp (µm)	nMOS width, Wn (µm)	(W/L)p	(W/L)n	Switching Threshold
1.	4	10	22.2	55.5	0.65
2.	10	4	55.5	22.2	0.8
3.	12	4	66.6	22.2	0.825

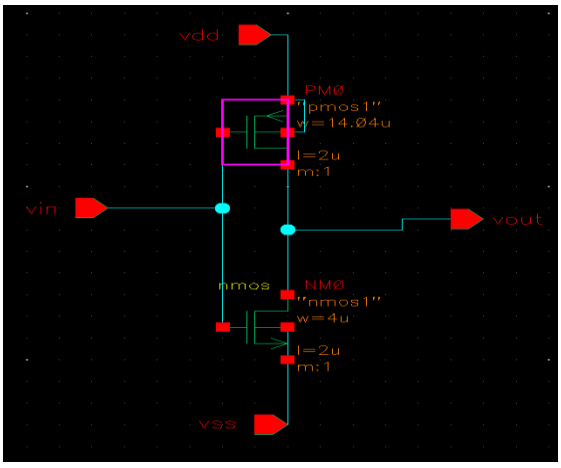

Fig 4: Schematic Diagram of CMOS Inverter

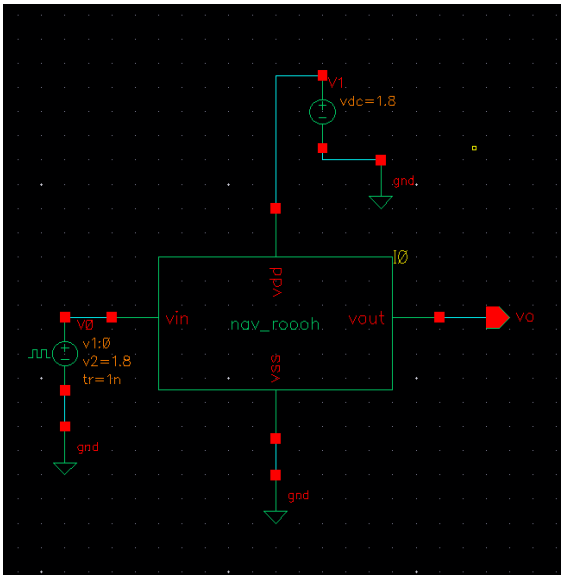

Fig 5: Symbol of CMOS Inverter

Complementary Metal-Oxide-Silicon circuits require an nMOS and pMOS transistor technology on the same substrate. To this end, an *n*-type well is provided in the *p*-type substrate. Alternatively one can use a *p*-well or both an *n*-type and *p*-type well in a low-doped substrate. The gate oxide, poly-silicon gate and source-drain contact metal are typically shared between the pMOS and nMOS technology, while the source-drain implants must be done separately [10]

Steps to draw layout are as follows: Layout for the inverter is generated from the inverter schematic, then connections are made between MOS terminals and power rails i.e. V_{dd} and Vss. Design Rule Check is run to verify whether all the rules for layout are satisfied or not .The schematic and layout of CMOS inverter is compared using 'LVS check'. Finally, RC extraction is done to see various resistance and capacitances present in Inverter layout. The layout diagram of CMOS Inverter is shown in fig. 6.

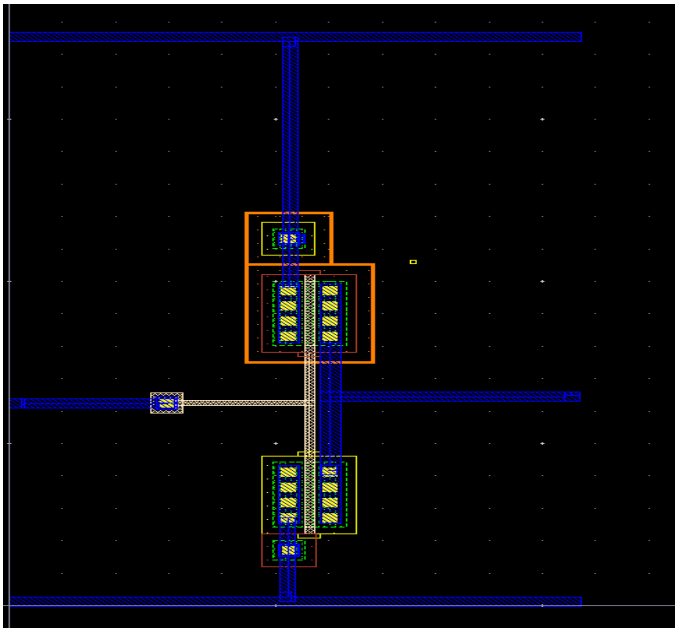

Fig 6: Layout of CMOS inverter

4. RESULTS AND DISCUSSIONS

Transient characteristics of CMOS inverter basically give a graph between input and output voltage (volts) w.r.t. time (ns). Top waveform shows the output, which is complementary to the input applied shown in the second quadrant of fig.7.

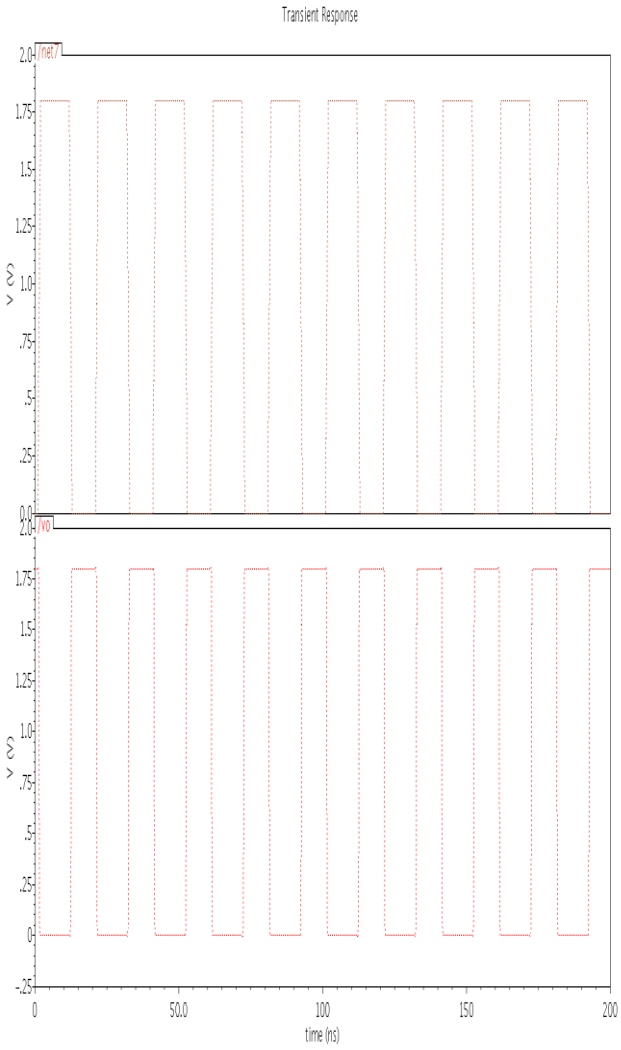

Fig 7: Transient Characteristics of CMOS Inverter

DC characteristics give output voltage (Vout) versus input voltage (Vin) of inverter. In fig. 8, DC response is shown for pMOS width=4µ and nMOS width=10µ i.e. Wp=0.4*Wn and $\beta n/ \beta_p$ =6.7 (approx). Therefore, corresponding curve shows strong pull down for switching threshold i.e. the point where Vin = Vout of 0.65, where it should be equal to Vdd/2=1.8/2=0.9 (approx).

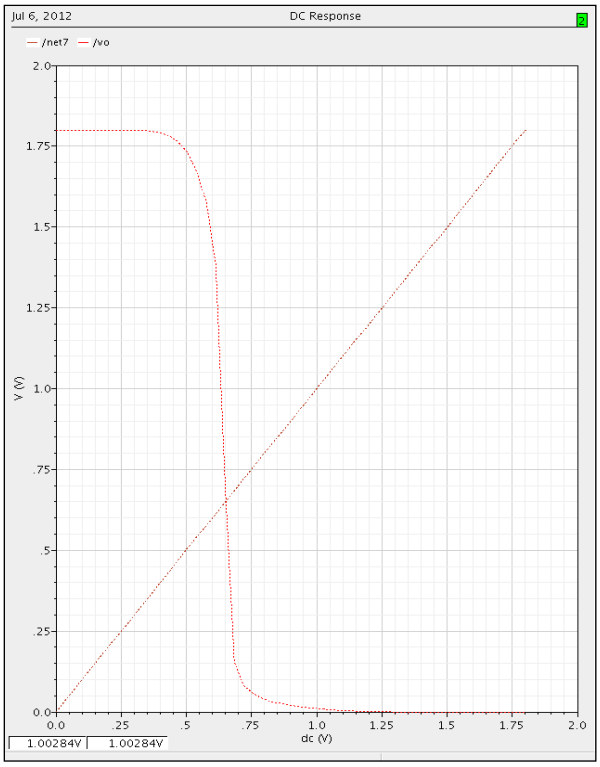

Fig 8: DC response of CMOS inverter for Wp/Wn=0.4.

In Fig.9 DC response for pMOS width=10µ and nMOS width=4µ. In this case, Wp=2.5*Wn. $\beta n/ \beta_p$ =0.98 (approx). Therefore, corresponding curve shows equal pull up-pull down and switching threshold comes out to be 0.8.

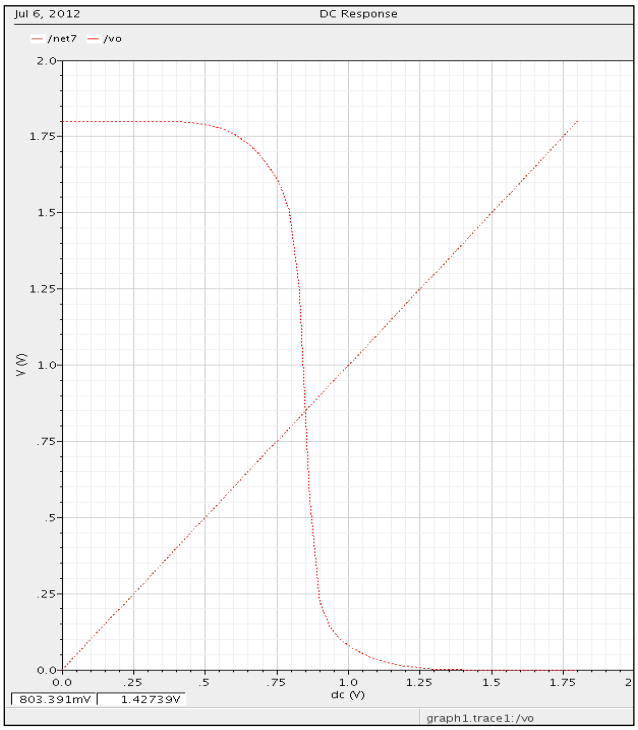

Fig 9: DC response of CMOS inverter for Wp/Wn=2.5

Fig.10 shows DC response for pMOS width=12µ and nMOS width=4µ. In this case, Wp=3*Wn. $\beta n/ \beta_p$ =0.83 (approx).

Therefore, corresponding curve shows strong pull up. Switching threshold i.e. the point where Vin = Vout is 0.825 and it is approx. equal to 0.9, which is required.

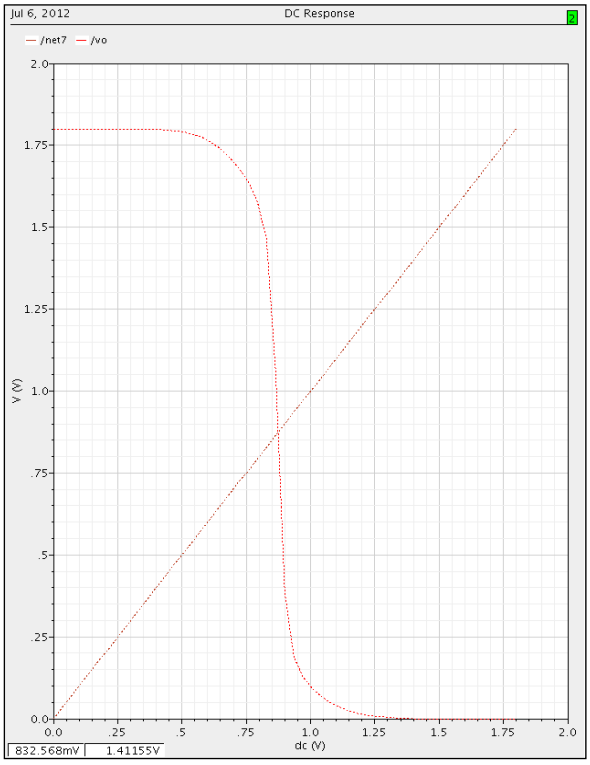

Fig 10: DC response of CMOS inverter for Wp/Wn=3

5. CONCLUSIONS

From the DC response of CMOS inverter, it is noted that for Wp/Wn=3, inverter is switching between logic 1 and logic 0 at exactly Vdd/2 value. This kind of characteristics is required for inverter applications. In other cases, switching occurs at 0.65 and 0.8, which deviates from the ideal value. Therefore, width of pMOS should be chosen such that it is approximately 2 to 3 times larger than that of nMOS transistor.

The effect of changing the Wp/Wn ratio is to shift the transient region of the VTC. Increasing the width of the PMOS or the NMOS moves V_M towards V_{DD} or GND respectively. This property can be very useful, as asymmetrical transfer characteristics are actually desirable in some designs.

6. FUTURE SCOPE

Other various parameters such as power, delay, power speed product can be calculated for CMOS inverter. Parameters like gate area, gate capacitance per unit area, gate capacitance, parasitic capacitance, channel resistance, gate delay, max operating freq, saturation current, power dissipation, current density are also of primary concern.

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