Architecture Design and FPGA Implementation of an FFT based Reactive Power Meter

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ABSTRACT
Reactive power measurement is increasingly paid attention by power industry. A novel architecture to measure the reactive power is proposed in this paper. Architecture is described in verilog and implemented using Xilinx ISE 13.1i. In this method voltage and current signals in time domain are converted to the frequency domain and power on each component is calculated to obtain the total reactive power.

Keywords
Xilinx, FFT, FPGA, DFF

1. INTRODUCTION
Novel methods of Reactive power measurement are drawing the attention of modern power system engineers due to the challenges in providing accuracy. In this modern era of electronic technology, power grids have been added to the large number of non-linear loads. This is resulting in a lot of harmonics into the power grids, causing serious distortion in power system voltage, current. Harmonic pollution will not only increase the wear and tear of the power components, but endanger the safe operation of power systems. Where sinusoidal variations of the power supply are not pure and multiple harmonics of fundamental frequency is present, electrical equipment like motors will not work properly and it leads to poor power factor, so that electrical equipment will not be utilized to their maximum capability. This also leads to wear and tear of transmission line. Therefore a system that measures the harmonic distortion plays an important role in the feedback system of the power grid in providing quality. By the architecture proposed in this paper, power is calculated through converting time domain voltage and current signals in to the frequency domain and summing the power on frequency component[6]. Low value for the relative error of the reactive power measured by FPGA is obtained, which is around 0.4%. Still this can be drastically minimized by using floating point multipliers inside the architecture implementation instead of fixed point multipliers. Architecture implementation is done using Xilinx ISE 13.1i and XC3S1200eFG320 device of Spartan3E family is targeted.

2. PROPOSED METHOD
The formula of reactive power for the sine wave can be shown as Equation 1.

$$P = I_{rms} * V_{rms} * \sin\theta \qquad \ldots\ldots (1)$$

The relationship between the maximum and the RMS value for a sine wave can be given by Equation (2)

$$V_{rms} = V_m/\sqrt{2},\ I_{rms} = I_m/\sqrt{2} \qquad \ldots\ldots (2)$$

Equation (2) is substituted into Equation1, then we can get the Equation (3).

$$P_k = 1/2 * I_{rms} * V_{rms} * \sin\theta \qquad \ldots\ldots (3)$$

In the formula (3) Im and Um are all maximums. For number k harmonic in the
non- sinusoidal condition, the formula of reactive power can be expressed as (4):

$$P_k = 1/2 * I_m(k) * V_m(k) * \sin\theta_K \qquad \ldots\ldots (4)$$

Then the total reactive power[7] is shown in Equation(5).

$$P_{total} = \sum_k 1/2 * I_m(k) * V_m(k) * \sin\theta_K \ldots\ldots (5)$$

For number k harmonic, we assume x1 and y1 representing voltage transform results. X1 and y1 are the results of FFT core. X1 is real part, y1 is imaginary part. In the same way, x2 and y2 are current transform results. X2 and y2 are results of FFT core. X2 is the real part, y2 is the imaginary part. The result of calculation through FFT cannot be used directly to compute the maximum value of voltages and currents and we need to scale the data. The scaling is done in the following manner, the outputs of FFT should be divided by 64 and then multiply with 2. Dividing by 2^6 is because of accumulation effect of fft and multiplying 2 is because the relationship of sine function and exponential function

$$\cos(x) = (e^{x} + e^{-jx})/2 \qquad \ldots\ldots (6)$$

The scaled values are

$$\left.\begin{aligned} X_1' &= 2 * X_1 / 2^6 \\ Y_1' &= 2 * X_1 / 2^6 \\ X_2' &= 2 * X_2 / 2^6 \\ Y_2' &= 2 * X_2 / 2^6 \end{aligned}\right\} \qquad \ldots\ldots (7)$$

The magnitude maximums can be expressed as

$$\left.\begin{aligned} V_m(k) &= \sqrt{X_1'^2 + Y_1'^2} \\ I_m(k) &= \sqrt{X_2'^2 + Y_2'^2} \end{aligned}\right\} \qquad \ldots\ldots (8)$$

For number k harmonic, θu is the voltage phase, θv is the current phase

$$\left.\begin{aligned} \sin\theta_u &= Y_1/\sqrt{X_1^2 + Y_1^2} \\ \cos\theta_u &= X_1/\sqrt{X_1^2 + Y_1^2} \\ \sin\theta_i &= Y_2/\sqrt{X_2^2 + Y_2^2} \\ \cos\theta_i &= X_2/\sqrt{X_2^2 + Y_2^2} \end{aligned}\right\} \qquad \ldots\ldots (9)$$

The formulae for phase seperation can be expressed as

$$\sin\theta_k = \sin(\theta_u - \theta_i)$$

$$= \sin\theta_u \cos\theta_i - \cos\theta_u \sin\theta_i \quad ...(10)$$

The power of a particular harmonic is given by:

$$P_K = (Y_1 * X_2 - X_1 * Y_2)/2^{11} \quad ....(11)$$

The total harmonic power is given by:

$$P = \sum_{K=1}^{N} P_K \quad ....(12)$$

3. FPGA IMPLEMENTATION

The proposed system module contains: Two FFT cores, Two multipliers subtraction module, Transposing module, Accumulator module to calculate the equation (12).

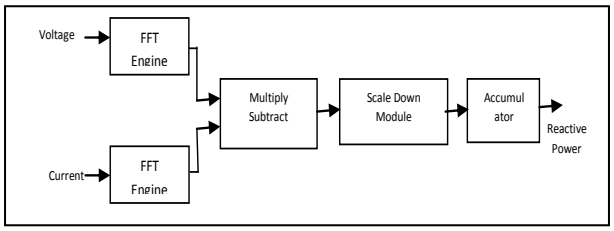
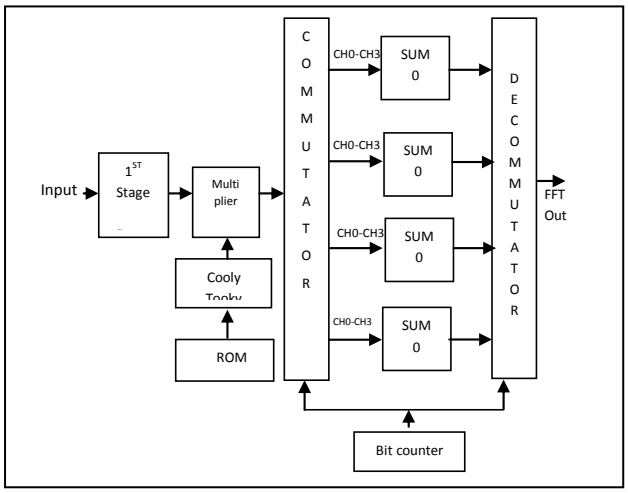


Fig 3.1 Block Diagram Of The Power Meter

3.1 FFT Engine

Two FFT cores are used to estimate the magnitudes and phases of each harmonic for voltage and current inputs.



3.2 FFT Engine Architecture

Initially FFT architecture consists of RST, CLK AND EN pins which are given as inputs to the FFT block. The reset pin performs initialization and termination operations. The clock signal will synchronize the entire operation.

3.2 Multiply Subtract unit

Multiply subtract unit calculates the numerator of the eq (11).,

3.3 Scale down module

Scale down unit performs the division in eq(11)This used minimize the bus width which holds the k^{th} power component.

3.4 Accumulator

This module is used to add the reactive power of all harmonics. This unit calculates the eq(12).

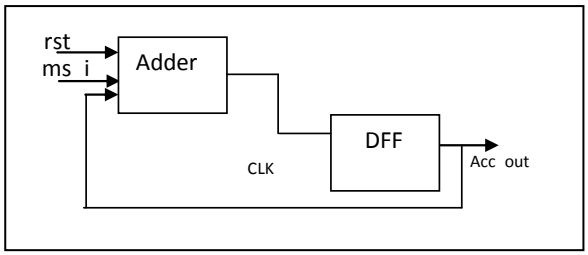


Fig 3.3 Accumulator

4. RESULTS

4.1 Simulation Results

4.1.1 Interface signals of FFT unit (voltage)

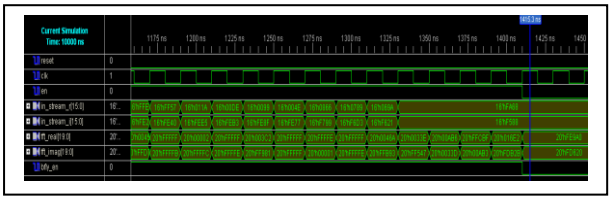


Fig 4.1 FFT Waveforms of Voltage

4.1.2 Interface signals of FFT unit (current)

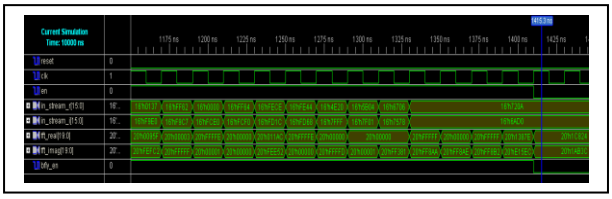


Fig 4.3 FFT Waveforms of Current

4.1.3 Interface signals of multiply subtract unit

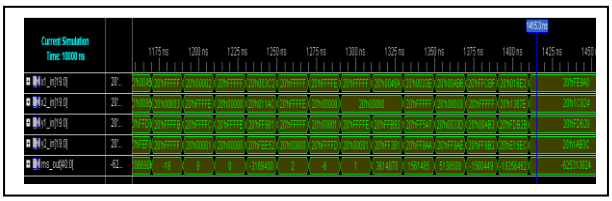


Fig 4.1 Multiply Subtract Unit- Waveforms

4.1.4 Interface signals of Accumulator unit

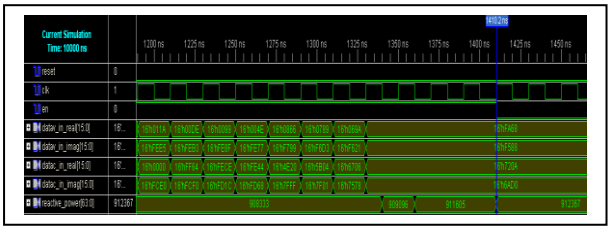


Fig 4.4 Reactive Power Result

4.2 Synthesis Results

4.2.1 RTL Schematic: In Out Pins

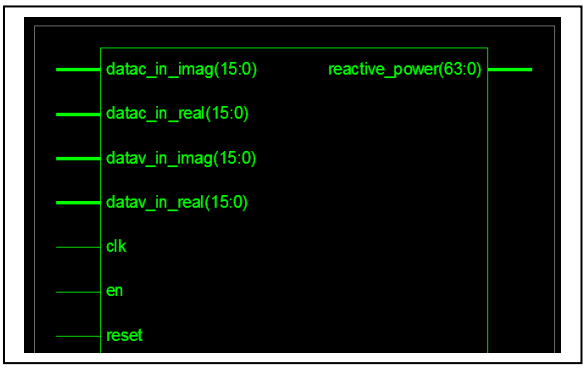


Fig 4.5 Top module's Port layout

4.2.2 RTL Schematic: Top Module

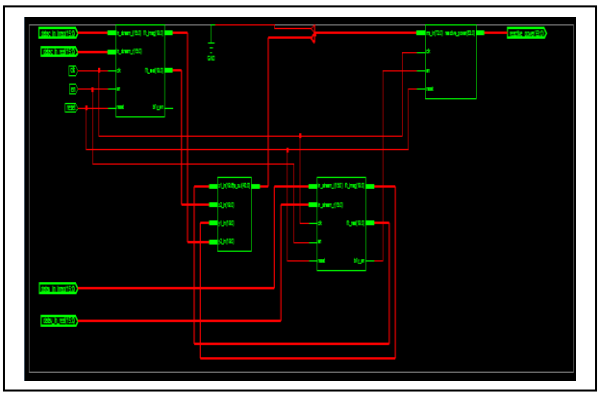


Fig 4.6 Top module

4.2.3 RTL Schematic: FFT Engine

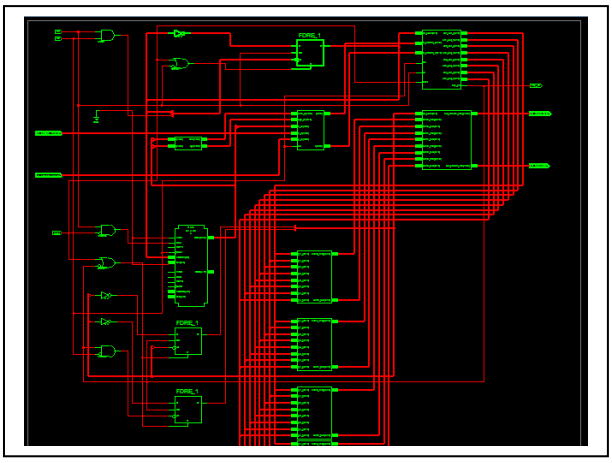


Fig 4.7 FFT Engine

4.3 Device Utilization Summery

FPGA synthesis by targeting Spartan 3e (XILINX) device results the requirement of FPGA components as seen in the Table.1.

Table 1. Device Utilization Summery

S. No.	FPGA Resource	Utilization
1	Slices	6487
2	Slice Flip Flops	548
3	4 input LUTs	1237
4	Ios	131
5	Bonded IOBs	131
6	BRAMs	2
7	GCLKs	10

5. PERFORMANCE

Reactive power using 'MATLAB' = 916310
Reactive power using 'FPGA' = 912367
The relative error of the simulation effect and data in theory is
= ((916310-912367)/916310)*100%
= 0.4303%

6. CONCLUSION

Architecture is implemented in Verilog and Xc3s1200e-4fg320 device of Spartan 3E family is targeted. FPGA simulation result obtained is very close to the theoretical result from Matlab. So it is preferable to develop an ASIC with this architecture to achieve highly accurate reactive power measurement.

7. REFERENCES

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