Comparative Study on Carrier Overlapping PWM Strategies for Three Phase Five Level Cascaded Inverter

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ABSTRACT
This paper presents the comparison of Carrier Overlapping Pulse Width Modulation (COPWM) techniques for the Cascaded Multi Level Inverter (CMLI). A CMLI is controlled in this paper with Sinusoidal PWM (SPWM) reference, Third Harmonic Injection PWM (THI PWM) reference, Sixty degree PWM reference and Stepped wave reference with Carrier Overlapping (CO) techniques. The variation of Total Harmonic Distortion (THD) in the inverter output voltage is observed when the chosen inverter is controlled by SPWM for various modulation indices. Simulation is performed using MATLAB-SIMULINK. It is observed that COPWM-C provides output with relatively low distortion for all strategies. It is also seen that COPWM-A is found to perform better for all strategies since it provides relatively higher fundamental RMS output voltage and in particular highest output is obtained for 60 degree PWM reference.

Keywords
THD, CMLI, Stepped, THIPWM, 60 degree PWM, COPWM.

1. INTRODUCTION
MultiLevel Inverter (MLI) offers a number of advantages when compared to the conventional two-level inverter counter part. The stepped approximation of the sinusoidal output waveform with higher levels reduces the harmonic distortion of the output waveform and the stresses across the semiconductor devices and also allows higher voltage/current and power ratings. The reduced switching frequency of each individual switch of the inverter also reduces the switching losses and improves the efficiency of the inverter. Donald Grahame Holmes and Mc Grath [1] proposed opportunities for harmonic cancellation with carrier-based PWM for two level and multilevel cascaded inverters. Loh et al [2] introduced synchronization of distributed PWM cascaded multilevel inverter with minimal harmonic distortion and common mode voltage. Mariethoz and Rufer [3] analysed resolution and efficiency improvements for three phase cascaded multilevel inverters. Xianglian et al [4] proposed phase-shift SPWM technique for cascaded multilevel inverter. Keith et al [5] introduced control of cascaded multilevel inverter. Deng et al [6] developed multilevel PWM methods based on control degrees of freedom combination and its theoretical analysis. Shanthi and Natarajan proposed carrier overlapping PWM methods for single phase cascaded five level inverter [7]. Roozbeh Naderi and Rahmati [8] described phase shifted carrier PWM technique for general cascaded inverters. Gierri Waltrich and Ivo Barbi [9] introduced three phase cascaded multilevel inverter using power cells. Gierri Waltrich and Ivo Barbi [10] also developed three phase cascaded multilevel inverter with commutation sub-cells. Jose Ignacio Leon et al [11] proposed multidimensional modulation technique for cascaded multilevel converters. Yerri Babu and Loveswara Rao [12] introduced a novel cascaded multilevel inverter with half bridge and full bridge cells in series. Batschauer et al [13] proposed three phase hybrid multilevel inverter based on half bridge modules. Yousefpoor et al [14] introduced THD minimization applied directly on the line to line voltage of multilevel inverters. Urmila and Subbarayudu [15] undertook comparative study of various pulse width modulation techniques. This work presents a novel approach for controlling the harmonics of output voltage of chosen MLI employing Sinusoidal, THI, 60 degree and Stepped wave PWM reference switching strategies since this literature survey reveals few papers only on chosen PWM techniques. Simulation is performed using MATLAB-SIMULINK. Harmonic analysis and evaluation of performance measures for various modulation indices have been carried out and presented.

2. MULTILEVEL INVERTER
Multilevel voltage source inverters have recently emerged as very important alternatives in high power, medium voltage applications. The function of a MLI is to synthesize a desired AC output voltage from several DC voltage sources with extremely low distortion. The MLIs provide high output voltages with low harmonics without the use of transformers or series connected synchronized switching devices. As the number of output voltage levels increases, the harmonic content of the output voltage decreases significantly. Increasing the number of voltage levels in the inverter output without requiring higher ratings on individual devices can increase the power rating of load. MLIs offer several advantages. These include higher DC bus utilization, improved harmonic performance and reduced stress on power devices. MLIs find applications in adjustable speed drives, electric utilities and renewable energy systems. Fig. 1 shows a configuration of the three phases five levels cascaded multilevel inverter. A cascaded multilevel inverter consists of a series of H-bridge inverter units. The general function of this inverter is to synthesize a desired voltage from several Separate DC Sources (SDCS). The load voltage is equal to the summation of the output voltage of the respective modules that are connected in series. The number of modules (M) which is equal to the number of DC sources required depends on the total number of positive, negative and zero levels (m) of the CMLI. It is usually assumed that m is odd as this would give an integer valued M. In this work, load voltage consists of five levels which include $+2V_{DC}$, $+V_{DC}$, 0, $-V_{DC}$ and $-2V_{DC}$ and the number of modules needed is 2. The following equation gives the relation between M and m,

$$M=\left(\frac{m-1}{2}\right)$$

The gate signals for chosen five level cascaded inverter are simulated using MATLAB-SIMULINK. The gate signal generator model developed is tested for various values of modulation index m_a and for various PWM strategies. Fig. 2 shows a sample SIMULINK model developed for COPWM-A method. The simulation results presented in this work in the form of the outputs of the chosen MLI are compared and evaluated.

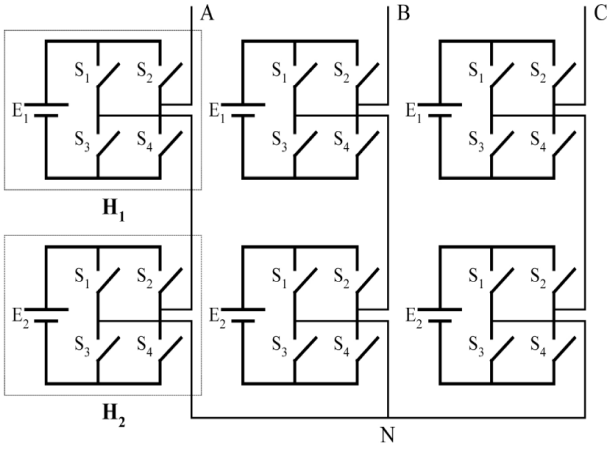

Fig 1: A three phase five level cascaded multilevel inverter

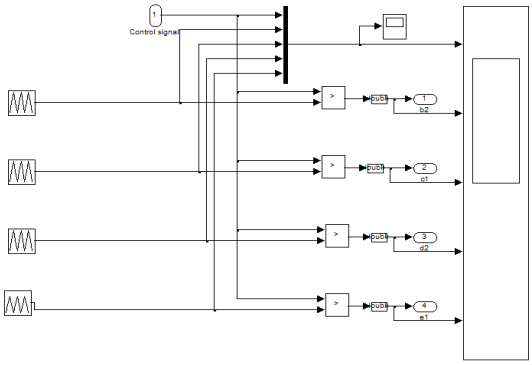

Fig 2: Sample PWM generation logic using SIMULINK model developed for COPWM-A technique

3. MODULATION STRATEGIES

The most popular method of controlling the output voltage is to incorporate PWM control within the inverters. In this method, a fixed DC input voltage is applied to the inverter and a controlled AC output voltage is obtained by adjusting the on and off periods of the inverter power semiconductor devices.. It is generally recognized that increasing the switching frequency of the PWM pattern reduces the lower frequency harmonics by moving the switching frequency carrier harmonics and associated sideband harmonics further away from the fundamental frequency component. The modulating/reference waves of multilevel carrier based PWM strategies employed in this work are sinusoidal, third harmonic injection, 60 degree PWM and stepped signal. As far as the particular reference wave is concerned, there is also multiple CFD including frequency, amplitude, phase angle of the reference wave. This paper focuses on three COPWM strategies that utilize the CFD of vertical offsets among triangular carriers. They are: COPWM-A, COPWM-B, COPWM-C. The above three strategies are simulated in this work.

The COPWM strategy utilizes the CFD of vertical offsets among carriers. The principle of COPWM strategy is to use several overlapping carriers with single modulating signal. For an m level inverter, m-1 carriers with the same frequency f_c and same peak-to-peak amplitude A_c are disposed such that the bands they occupy overlap each other. The overlapping vertical distance between each carrier is $A_c/2$ in this work. The reference wave has the amplitude A_m and frequency f_m and it is centered in the middle of the carrier signals [7]. The amplitude modulation index m_a and the frequency ratio m_f are defined in the carrier overlapping method as follows:

$$m_a = \frac{A_m}{\left(\frac{m}{4}\right)A_c}$$

$$m_f = \frac{f_c}{f_m}$$

3.1 COPWM-A Strategy

Without loss of generality, the vertical offset of carriers for an five level inverter using COPWM-A can be illustrated in Figs.3-6 wherein the normalized peak-to-peak amplitude of the single sinusoidal modulating wave equals to 4. There are four triangular carriers with same phase, same frequency of f_c and same amplitude of V [6].

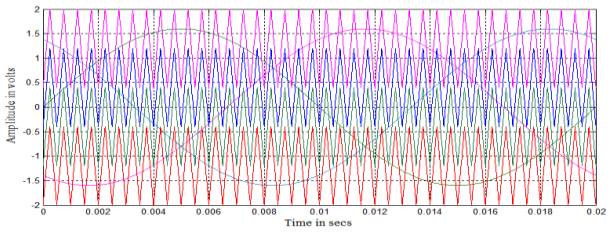

Fig 3: Carrier arrangement for COPWM-A strategy with sine reference (m_a=0.8 , m_f=40)

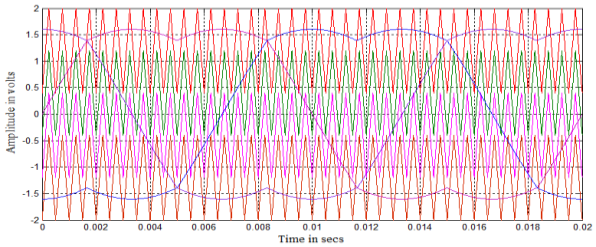

Fig 4: Carrier arrangement for COPWM-A strategy with THI reference (m_a=0.8 , m_f=40)

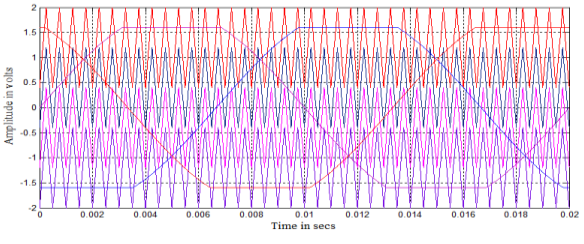

Fig 5: Carrier arrangement for COPWM-A strategy with 60 degree reference (m_a=0.8 , m_f=40)

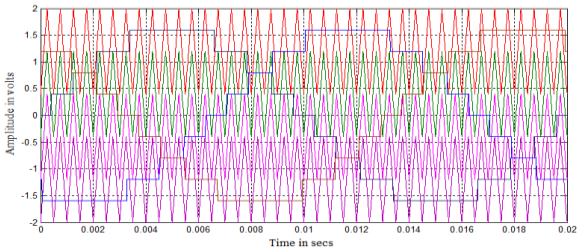

Fig 6: Carrier arrangement for COPWM-A strategy with stepped wave reference (m_a=0.8 , m_f=40)

3.2 COPWM-B Strategy

Carriers for 5-level COPWM-B are shown in Figs.7-10. It can be seen that they are divided equally into two groups according to the positive/negative average levels. This scheme tells no difference except the two groups are opposite in phase with each other while keeping in phase within the group [6].

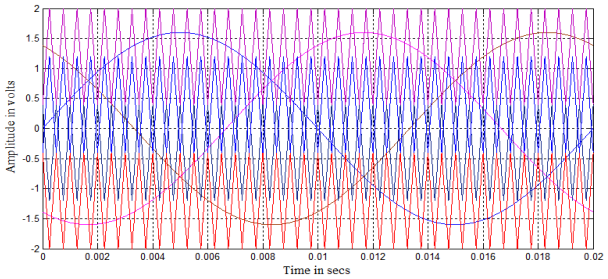

Fig 7: Carrier arrangement for COPWM-B strategy with sine reference (m_a=0.8 , m_f=40)

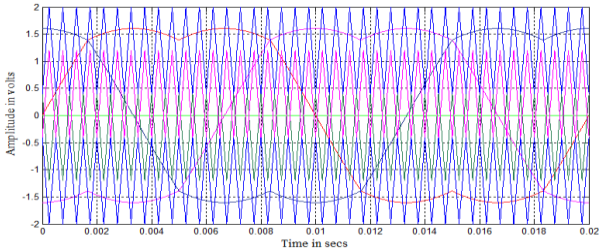

Fig 8: Carrier arrangement for COPWM-B strategy with THI reference (m_a=0.8 , m_f=40)

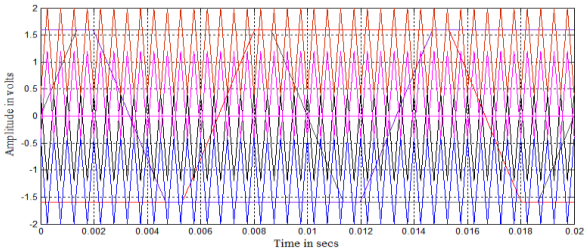

Fig 9: Carrier arrangement for COPWM-B strategy with 60 degree reference (m_a=0.8 , m_f=40)

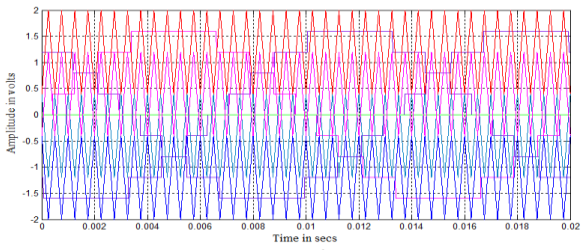

Fig 10: Carrier arrangement for COPWM-B strategy with stepped wave reference (m_a=0.8 , m_f=40)

3.3 COPWM-C Strategy

Carriers for 5-level COPWM-C are shown in Figs.11-14. In this pattern the carriers invert their phase in turns from the previous one. It may be identified as PWM with amplitude overlapped and neighboring phase interleaved carriers. Actually, pattern B and C can be looked on as a second control freedom change besides offsets in vertical: the carriers have horizontal phase shift from pattern A [7].

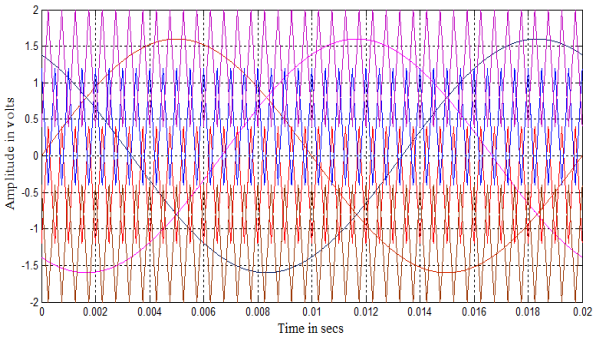

Fig 11: Carrier arrangement for COPWM-C strategy with sine reference (m_a=0.8 , m_f=40)

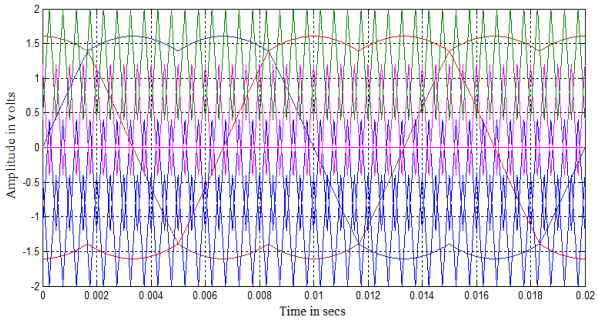

Fig 12: Carrier arrangement for COPWM-C strategy with THI reference (m_a=0.8 , m_f=40)

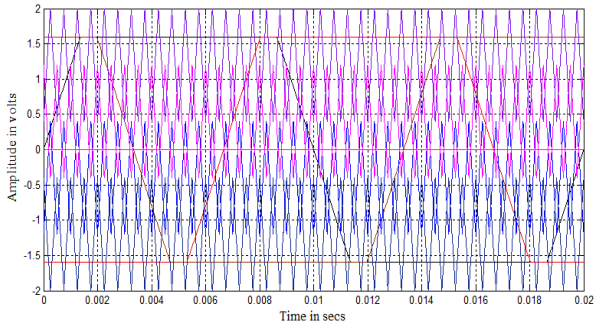

Fig 13: Carrier arrangement for COPWM-C strategy with 60 degree reference (m_a=0.8 , m_f=40)

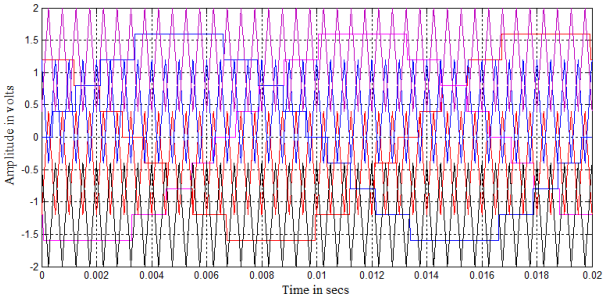

Fig 14: Carrier arrangement for COPWM-C strategy with stepped wave reference (m_a=0.8 , m_f=40)

4. THIRD HARMONIC INJECTION PWM

In this technique, a third harmonic component is superimposed on the fundamental. The addition of third harmonic makes it possible to increase the maximum amplitude of fundamental in the reference and in the output voltages . Third harmonic technique is preferred in three-phase applications since cancellation of third harmonic components and better utilization of DC supply can be achieved. Harmonic elimination techniques, which are suitable for fixed output voltage, increase the order of harmonics and reduce the size of output filter. But these advantages should be weighed against increase in switching losses of power devices and iron losses in transformer due to high harmonic frequencies. It is not always necessary to eliminate triplen harmonics which are not normally present in three phase connections. So, in three phase inverters, it is preferable to eliminate fifth, seventh and eleventh harmonics of output voltages, so that the lowest order harmonic will be thirteenth [15]. Firing pulses generation with third harmonic injection PWM method is using Figs. 4, 8 and 12.

5. 60 DEGREE PWM

This method is almost similar to sinusoidal PWM except that the modulating sine wave is flat topped for a period of 60 degrees in each half cycle. 60 degree PWM reference technique is as shown in Figs. 5, 9 and 13.

6. STEPPED MODULATION

The stepped wave is not a sampled approximation to the sine wave. It is divided into specified intervals, say 20^0 with each interval controlled individually to control magnitude of the fundamental component and to eliminate specific harmonics. This type of control gives low distortion but a higher fundamental amplitude compared with that of normal PWM control. Stepped wave PWM technique is as shown in Figs. 6, 10 and 14.

7. SIMULATION RESULTS

The cascaded five level inverter is modeled in SIMULINK using power system block set. Switching signals for CMLI are developed using bipolar PWM techniques discussed previously. Simulation are performed for different values of m_a ranging from 0.6 – 1. The corresponding %THD values are measured using FFT block and they are shown in Tables 1, 3 , 5 and 7. Tables 2, 4, 6 and 8 display the V_{RMS} of fundamental of inverter output for same modulation indices. Figs. 15-38 show the simulated output voltage of CMLI and corresponding FFT plots with above strategies but for only one sample value of m_a = 0.8 for all the chosen reference signal. Fig. 15 shows the five level output voltage generated by COPWM-A strategy and its FFT plot is shown in Fig. 16. From Fig. 16 it is observed that the COPWM-A strategy produces significant 3rd and 38th harmonic energy. Fig. 17 shows the five level output voltage generated by COPWM-B strategy and its FFT plot is shown in Fig. 18. From Fig. 18 it is observed that the COPWM-B produces significant 3rd, 35th, and 37th harmonic energy. Fig. 19 shows the five level output voltage generated by COPWM-C strategy and its FFT plot is shown in Fig. 20. From Fig. 20 it is observed that the COPWM-C strategy produces significant 3rd, 33rd, 35th and 37th harmonic energy.

Fig. 21 shows the five level output voltage generated by COPWM-A (THI) strategy and its FFT plot is shown in Fig. 22. From Fig. 22 it is observed that the COPWM-A (THI) strategy produces significant 3rd, 5th and 38th harmonic energy. Fig. 23 shows the five level output voltage generated by COPWM-B (THI) strategy and its FFT plot is shown in Fig. 24. From Fig. 24 it is observed that the COPWM-B (THI) strategy produces significant 3rd, 5th, 33rd, 35th and 37th harmonic energy. Fig. 25 shows the five level output voltage generated by COPWM-C (THI) strategy and its FFT plot is shown in Fig. 26. From Fig. 26 it is observed that the COPWM-C (THI) strategy produces significant 3rd, 5th, 29th, 31st and 33rd harmonic energy.

Fig. 27 shows the five level output voltage generated by COPWM-A (60 degree) strategy and its FFT plot is shown in Fig. 28. From Fig. 28 it is observed that the COPWM-A (60 degree) strategy produces significant 3rd, 5th and 7th harmonic energy. Fig. 29 shows the five level output voltage generated by COPWM-B (60 degree) strategy and its FFT plot is shown in Fig. 30. From Fig. 30 it is observed that the COPWM-B (60 degree) strategy produces significant 3rd, 5th, 7th, 31st, 33rd, 35th and 37th harmonic energy. Fig. 31 shows the five level output voltage generated by COPWM-C (60 degree) strategy and its FFT plot is shown in Fig. 32. From Fig. 32 it is observed that the COPWM-C (60 degree) strategy produces significant 3rd, 29th, 31st , 33rd and 35th harmonic energy.

Fig. 33 shows the five level output voltage generated by COPWM-A (stepped wave) strategy and its FFT plot is shown in Fig.34. From Fig. 34 it is observed that the COPWM-A (stepped wave) strategy produces significant 3rd, 23rd, 25th , 35th and 37th harmonic energy. Fig. 35 shows the five level output voltage generated by COPWM-B (stepped wave) strategy and its FFT plot is shown in Fig. 36. From Fig. 36 it is observed that the COPWM-B (stepped wave) strategy produces significant 3rd, 23rd, 25th and 38th harmonic energy. Fig. 37 shows the five level output voltage generated by COPWM-C (stepped wave) strategy and its FFT plot is shown in Fig. 38. From Fig. 38 it is observed that the COPWM-C (stepped wave) strategy produces significant 3rd, 13th, 17th, 21st, 23rd, 25th, 33rd, 35th and 37th harmonic energy. The following parameter values are used for simulation: V_{DC} =220V and R (load) = 100 ohms.

7.1 Simulation Results for Sinusoidal Reference

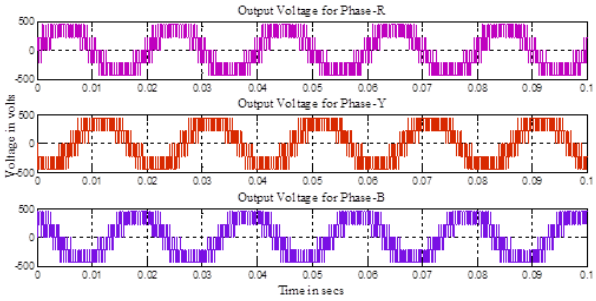

Fig 15: Output voltage generated by COPWM-A strategy

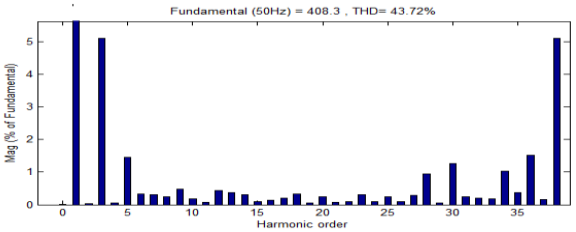

Fig 16: FFT plot for output voltage of COPWM-A strategy

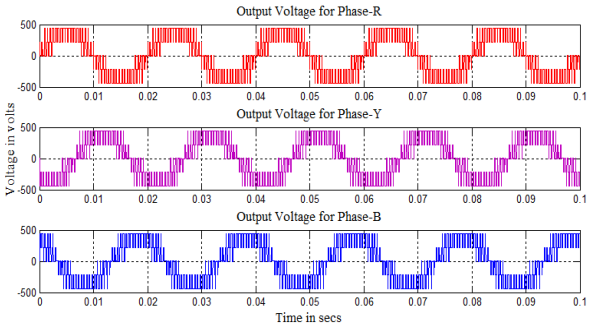

Fig 17: Output voltage generated by COPWM-B strategy

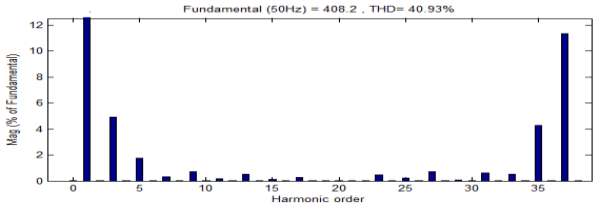

Fig 18: FFT plot for output voltage of COPWM-B strategy

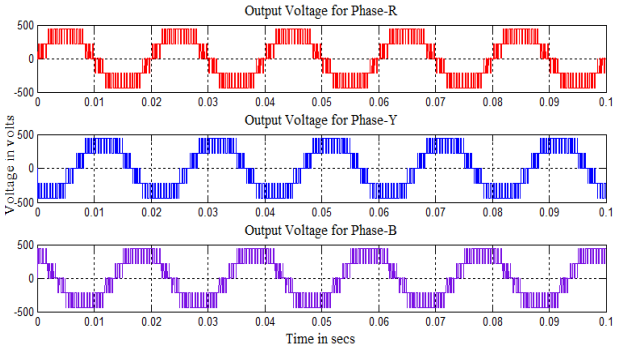

Fig 19: Output voltage generated by COPWM-C strategy

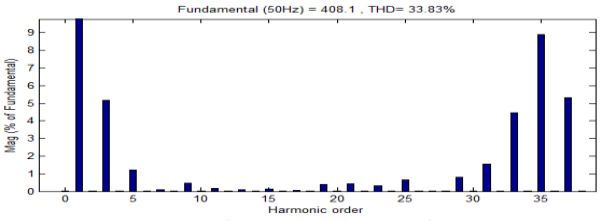

Fig 20: FFT plot for output voltage of COPWM-C strategy

7.2 Simulation Results for Third Harmonic Injection PWM Reference

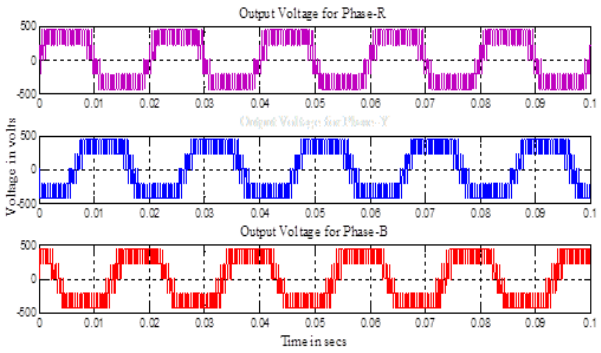

Fig 21: Output voltage generated by COPWM-A strategy

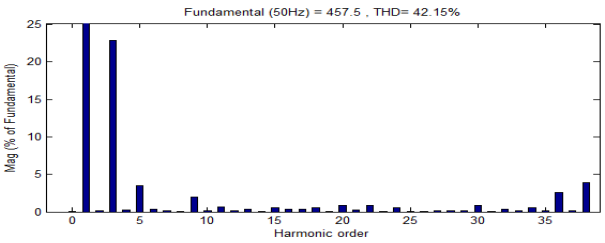

Fig 22: FFT plot for output voltage of COPWM-A strategy

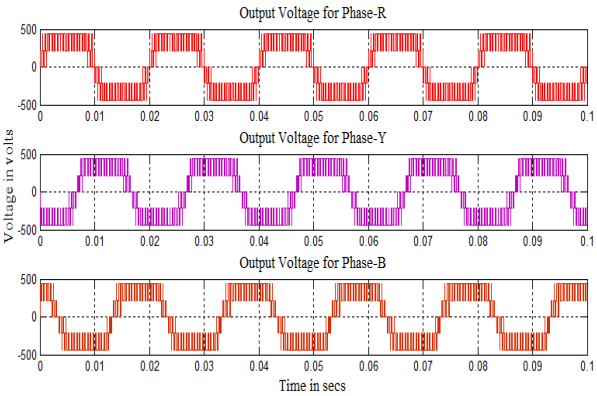

Fig 23: Output voltage generated by COPWM-B strategy

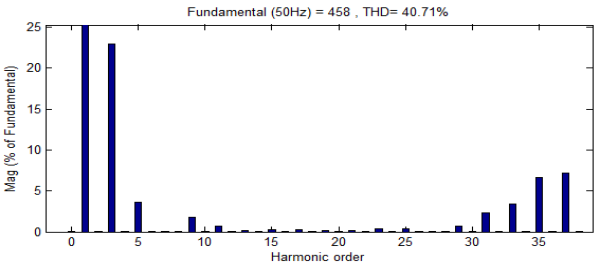

Fig 24: FFT plot for output voltage of COPWM-B strategy

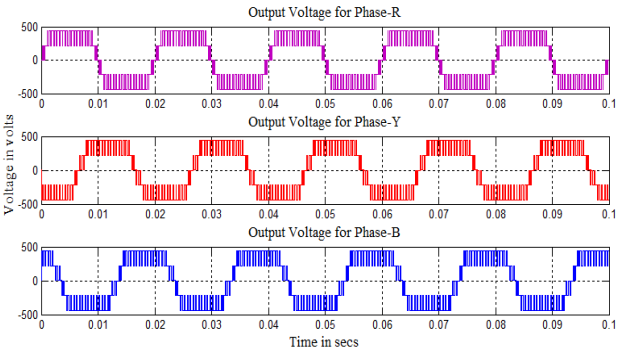

Fig 25: Output voltage generated by COPWM-C strategy

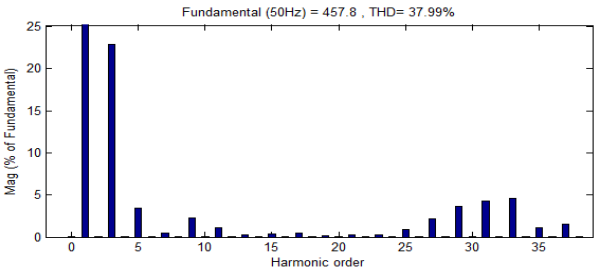

Fig 26: FFT plot for output voltage of COPWM-C strategy

7.3 Simulation Results for 60 Degree PWM Reference

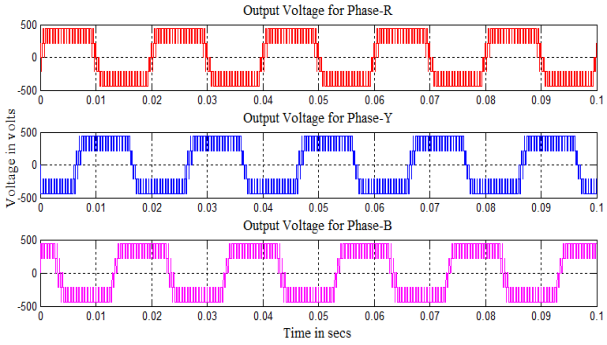

Fig 27: Output voltage generated by COPWM-A strategy

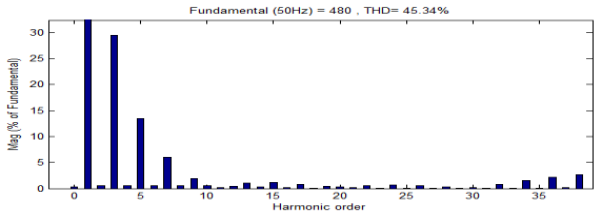

Fig 28: FFT plot for output voltage of COPWM-A strategy

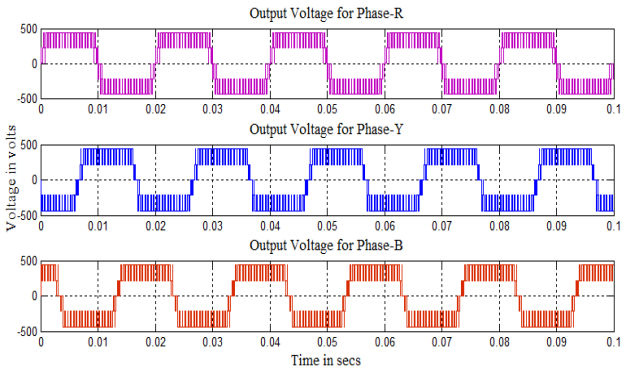

Fig 29: Output voltage generated by COPWM-B strategy

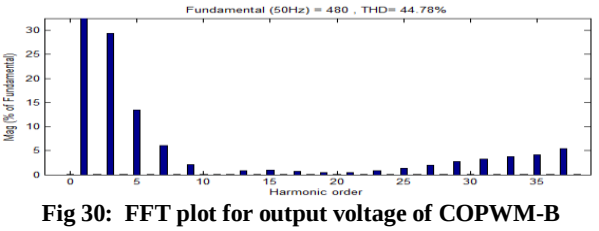

Fig 30: FFT plot for output voltage of COPWM-B strategy

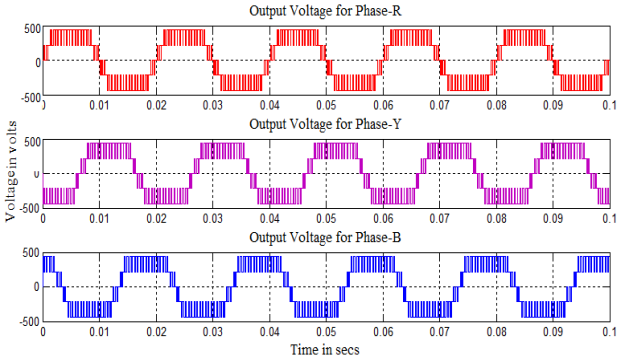

Fig 31: Output voltage generated by COPWM-C strategy

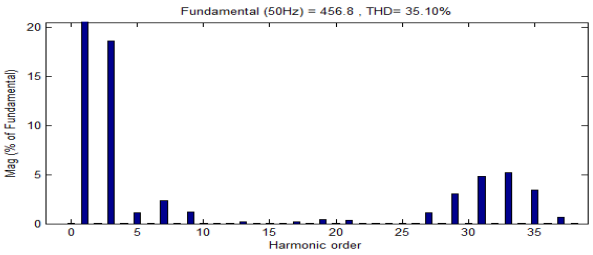

Fig 32: FFT plot for output voltage of COPWM-C strategy

7.4 Simulation Results for Stepped Wave Reference

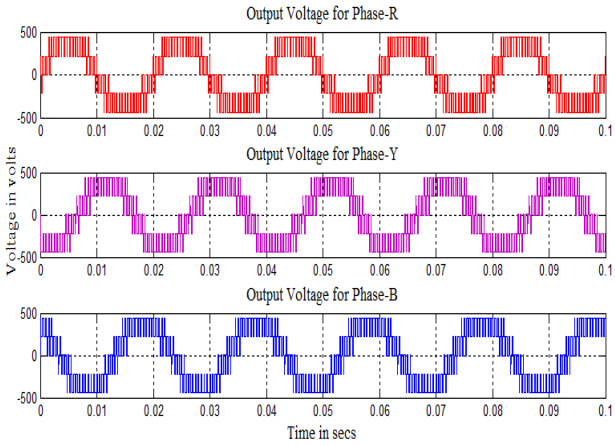

Fig 33: Output voltage generated by COPWM-A strategy

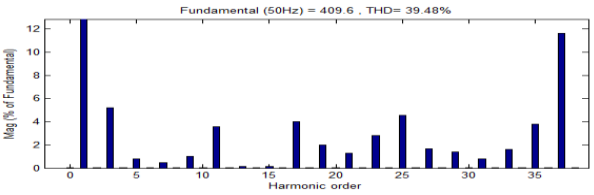

Fig 34: FFT plot for output voltage of COPWM-A strategy

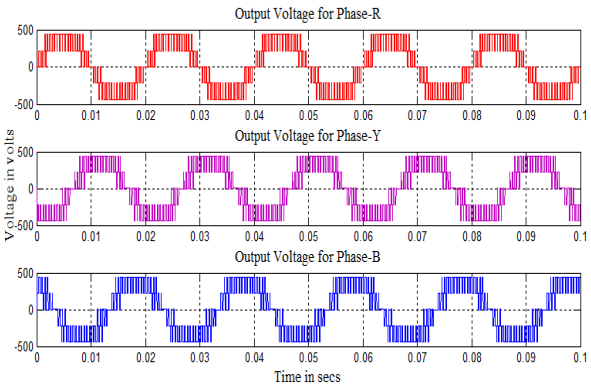

Fig 35: Output voltage generated by COPWM-B strategy

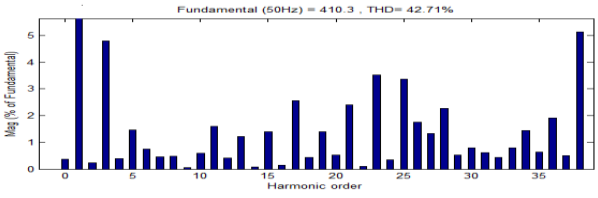

Fig 36: FFT plot for output voltage of COPWM-B strategy

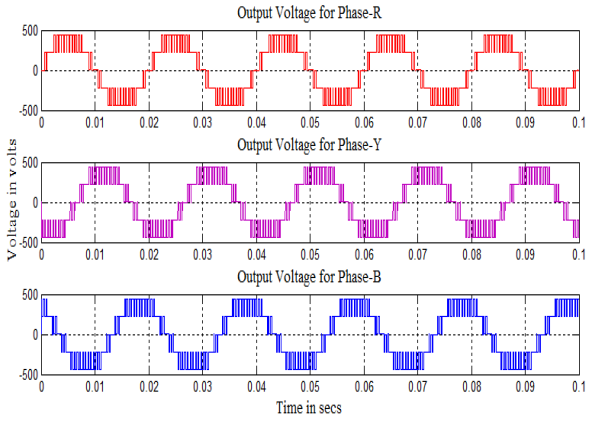

Fig 37: Output voltage generated by COPWM-C strategy

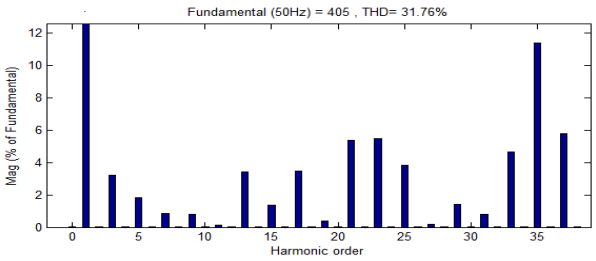

Fig 38: FFT plot for output voltage of COPWM-C strategy

Table 1. % THD for different modulation indices for sinusoidal reference

m_a	COPWM-A	COPWM-B	COPWM-C
1	33.57	31.39	26.00
0.9	38.51	36.11	29.92
0.8	43.72	40.93	33.83
0.7	50.27	46.68	36.95
0.6	58.88	55.01	40.38

Table 2. V_{RMS} (fundamental) for different modulation indices with sinusoidal reference

m_a	COPWM-A	COPWM-B	COPWM-C
1	333.1	332.9	332.8
0.9	311.9	312	311.9
0.8	288.7	288.6	288.6
0.7	261.9	262.2	261.5
0.6	233.8	233.7	234.4

Table 3. % THD for different modulation indices for THI PWM reference

m_a	COPWM-A	COPWM-B	COPWM-C
1	33.37	32.32	30.84
0.9	38.25	37.02	34.84
0.8	42.15	40.71	37.99
0.7	45.62	43.91	40.65
0.6	52.86	50.40	43.19

Table 4. V_{RMS} (fundamental) for different modulation indices with THI PWM reference

m_a	COPWM-A	COPWM-B	COPWM-C
1	370.3	370.1	370.1
0.9	346.5	346.5	346
0.8	323.5	323.8	323.7
0.7	300	299.7	299.5
0.6	269.4	270.1	269.5

Table 5. % THD for different modulation indices with 60 degree PWM reference

m_a	COPWM-A	COPWM-B	COPWM-C
1	36.39	35.93	25.79
0.9	41.50	41.06	31.06
0.8	45.34	44.78	35.10
0.7	48.57	47.86	38.12
0.6	51.24	50.21	39.99

Table 6. V_{RMS} (fundamental) for different modulation indices with 60 degree PWM reference

m_a	COPWM-A	COPWM-B	COPWM-C
1	394	390.3	372.5
0.9	363.1	363.2	346.4
0.8	339.4	339.4	323
0.7	315.6	315.5	299
0.6	291.5	291.6	273.6

Table 7. % THD for different modulation indices with stepped wave reference

m_a	COPWM-A	COPWM-B	COPWM-C
1	33.34	31.35	25.43
0.9	38.17	35.63	29.73
0.8	39.48	42.71	31.76
0.7	50.42	47.12	36.97
0.6	57.99	53.72	40.27

Table 8. V_{RMS} (fundamental) for different modulation indices with stepped wave reference

m_a	COPWM-A	COPWM-B	COPWM-C
1	335.4	334.8	332.8
0.9	310.6	309.2	306.7
0.8	290.1	289.6	286.4
0.7	263.8	262.7	261.5
.6	236.7	236.4	236.6

Table 9. Crest factor for different modulation indices with sinusoidal reference

m_a	COPWM-A	COPWM-B	COPWM-C
1	1.4143	1.4140	1.4144
0.9	1.4145	1.4141	1.4142
0.8	1.4142	1.4141	1.4142
0.7	1.4142	1.4141	1.4140
0.6	1.4140	1.4139	1.4145

Table 10. Crest factor for different modulation indices with THI PWM reference

m_a	COPWM-A	COPWM-B	COPWM-C
1	1.4141	1.4152	1.4140
0.9	1.4141	1.4141	1.4139
0.8	1.4140	1.4142	1.4143
0.7	1.4138	1.4141	1.4139
0.6	1.4142	1.4141	1.4144

Table 11. Crest factor for different modulation indices with 60 degree PWM reference

m_a	COPWM-A	COPWM-B	COPWM-C
1	1.4142	1.4144	1.4140
0.9	1.4142	1.4142	1.4143
0.8	1.4142	1.4145	1.4139
0.7	1.4143	1.4141	1.4143
0.6	1.4143	1.4139	1.4144

Table 12. Crest factor for different modulation indices with stepped wave reference

m_a	COPWM-A	COPWM-B	COPWM-C
1	1.4138	1.4140	1.4144
0.9	1.4138	1.4143	1.4143
0.8	1.4139	1.4145	1.4160
0.7	1.4141	1.4141	1.4144
0.6	1.4143	1.4140	1.4141

Table 13. Form factor for different modulation indices with sinusoidal reference

m_a	COPWM-A	COPWM-B	COPWM-C
1	16655	INF	INF
0.9	3119	INF	INF
0.8	INF	INF	INF
0.7	INF	INF	INF
0.6	3340	INF	INF

Table 14. Form factor for different modulation indices with THI PWM reference

m_a	COPWM-A	COPWM-B	COPWM-C
1	925	INF	INF
0.9	INF	INF	INF
0.8	6470	INF	INF
0.7	1875	INF	INF
0.6	2993	INF	INF

Table 15. Form factor for different modulation indices with 60 degree PWM reference

m_a	COPWM-A	COPWM-B	COPWM-C
1	2814	INF	INF
0.9	1396	INF	INF
0.8	1257	INF	INF
0.7	3156	INF	INF
0.6	5830	INF	INF

Table 16. Form factor for different modulation indices with stepped wave reference

m_a	COPWM-A	COPWM-B	COPWM-C
1	1597	INF	INF
0.9	6212	INF	INF
0.8	763	INF	INF
0.7	497	INF	INF
0.6	1183	INF	INF

Table 17. Distortion factor for different modulation indices with sinusoidal reference

m_a	COPWM-A	COPWM-B	COPWM-C
1	0.840	0.840	0.830
0.9	0.742	0.751	0.753
0.8	0.571	0.552	0.574
0.7	0.248	0.271	0.211
0.6	0.053	0.053	0.042

Table 18. Distortion factor for different modulation indices with THI PWM reference

m_a	COPWM-A	COPWM-B	COPWM-C
1	2.634	2.643	2.648
0.9	2.603	2.625	2.589
0.8	2.545	2.557	2.543
0.7	2.431	2.437	2.541
0.6	2.294	2.242	2.328

Table 19. Distortion factor for different modulation indices with 60 degree PWM reference

m_a	COPWM-A	COPWM-B	COPWM-C
1	3.334	3.329	3.330
0.9	3.343	3.347	3.329
0.8	3.318	3.315	3.309
0.7	3.276	3.265	3.288
0.6	3.169	3.209	3.207

Table 20. Distortion factor for different modulation indices with stepped wave reference

m_a	COPWM-A	COPWM-B	COPWM-C
1	0.700	0.787	0.648
0.9	0.601	0.645	0.475
0.8	0.543	0.583	0.364
0.7	0.316	0.311	0.121
0.6	0.100	0.087	0.266

8. CONCLUSIONS

In this paper various new schemes adopting the constant switching frequency multicarrier CFD concepts are developed and simulated for chosen inverter. Performance factors like %THD, V_{RMS} (indicating the amount of DC bus utilization), CF, FF and DF related to power quality issues have been evaluated, presented and analyzed. It is observed from Tables 1, 3, 5 and 7 that COPWM-C strategy provides output with relatively low distortion for all the four strategies developed. COPWM-A is found to perform better for all strategies since it provides relatively higher fundamental RMS output voltage (Tables 2, 4, 6 and 8) and in particular highest output is obtained for 60 degree PWM reference. Tables 9, 10, 11 and 12 show CF. Next four tables provide FF for all chosen modulating indices and DF is found in last four tables. The result indicate that appropriate PWM strategies have to be employed depending on the performance measure required in a particular application of MLI based on the criteria of output voltage quality (Peak value of the fundamental, THD and dominant harmonic components).

9. REFERENCES

[1] Donald Grahame Holmes, P.Brendam and Mcgrath, "Opportunities for Harmonic Cancellation with Carrier-Based PWM for Two-Level and Multilevel Cascaded Inverters", IEEE Trans. on Industry Applications, 2001, 37(2), 574-582.

[2] Loh, P.C. Holme, D.G. and Lipo, T.A. 2003. Synchronisation of Distributed PWM Cascaded Multilevel Inverter with Minimal Harmonic Distortion and Common Mode Voltage, IEEE Conf.Rec:0-7803-7754-0/03, 177-182.

[3] Mariethoz, S. and Rufer, A. 2004. Resolution and Efficiency Improvements for Three Phase Cascaded Multilevel Inverters, IEEE Conf. Rec: 0-7803-8399-0/04, 4441-4446.

[4] Xianglian Xu,Yunping Zou, Kai Ding, and Feiliu, 2004. Cascaded Multilevel Inverter with Phase-Shift SPWM and its Application in STATCOM, IEEE Conf.Rec: 0-7803-8730-9/04, 1139-1143.

[5] A.Keith, Corzine, W.Mike, Wielebski, Z.Fang, Peng, and Jin Wang, "Control of Cascaded Multilevel Inverter", IEEE Trans. on Power Electronics, 2004, 19(3), 732-738.

[6] Deng, Y. Wang, H. Zhang, C. Hu, L and He, X. 2005. Multilevel PWM Methods based on Control Degrees of Freedom Combination and Its Theoretical Analysis, IEEE Conf. Rec: 0-7803-9208-6/05, pp. 1692-1699.

[7] B. Shanthi, S.P.Natarajan, "Carrier Overlapping PWM Methods for Single Phase Cascaded Five Level Inverter", International Journal of Science and Technology of Automatic Control & Computer Engineering (IJ-STA, Tunisia). Special issue on Control of Electrical Machines, 2008, 590-601.

[8] Roozbeh Naderi, Abdolreza Rahmati, "Phase-Shifted Carrier PWM Technique for General Cascaded Inverters", IEEE Trans. on Power Electronics, 2008, 23(3), 1257-1269.

[9] Gierri waltrich and Ivo Barbi. "Three-Phase Cascaded Multilevel Inverter using Power Cell Switch with Two Inverter Legs in Series", IEEE Trans. on Industrial Electronics, 2010, 57(8), 2605-2612.

[10] Gierri Waltrich and Ivo Barbi. 2010. Three-Phase Cascaded Multilevel Inverter using Commutation Sub-Cells. IEEE Conf. Rec.978-1-4244-3370-4/09. 362-368.

[11] Jose Ignacio Leon, Samir Kouro, Sergio Vazquez, Ramon Portillo, Leopoldo Garcia Franquelo, Juanmanuel Carrasco and Jose Rodriguez, "Multidimensional Modulation Technique for Cascaded Multilevel Converters", IEEE Trans. on Industrial Electronics, 2011, 58(2), pp 412-420.

[12] G.Yerri Babu, B.Loveswara Rao, "A Novel Cascaded Multilevel Inverter with Half Bridge and Full Bridge Cells in Series", International Journal of Science and Advanced Technology, 2012, 2(1), 71-76.

.[13] A.L.Batschauer, S.A.Mussa and M.L.Heldwein, "Three Phase Hybrid Multilevel Inverter Based on Half Bridge Modules", IEEE Trans. on Industrial Electronics , 2012, 59(2), 668-678.

[14] N.Yousefpoor, S.H.Fathi, N.Farokhnia and H.A.Abyaneh, "THD Minimization Applied Directly on the Line-to-Line Voltage of Multilevel Inverters", IEEE Transactions on Industrial Electronics, 2012, 59(1), pp. 373-380.

[15] B.Urmila, and D.Subbarayudu, "Multilevel Inverters: A Comparative Study of Pulse Width Modulation Techniques", Journal of Scientific and Engineering Research, 2010, 1(13), 1-5.