Design of 4x4 bit Vedic Multiplier using EDA Tool

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ABSTRACT
The need of high speed multiplier is increasing as the need of high speed processors are increasing. A Multiplier is one of the key hardware blocks in most fast processing system which is not only a high delay block but also a major source of power dissipation. A conventional processor requires substantially more hardware resources and processing time in the multiplication operation, rather than addition and subtraction. This paper presents a high speed 4x4 bit Vedic Multiplier (VM) based on Vertically & Crosswise method of Vedic mathematics, a general multiplication formulae equally applicable to all cases of multiplication. It is based on generating all partial products and their sum in one step. The coding is done in VHDL (Very High Speed Integrated Circuit Hardware Descriptive Language) while the synthesis and simulation is done using EDA (Electronic Design Automation) tool - XilinxISE12.1i. The combinational path delay of 4x4 bit Vedic multiplier obtained after synthesis is compared with normal multipliers and found that the proposed Vedic multiplier circuit seems to have better performance in terms of speed.

General Terms
Vedic Multiplier (VM)

Keywords
Vedic Multiplication, Urdhva Tiryakbhyam Sutra, Ripple Carry Adder.

1. INTRODUCTION
Multipliers are extensively used in Microprocessors, DSP and Communication applications. For higher order multiplications, a huge number of adders are to be used to perform the partial product addition. The need of low power and high speed Multiplier is increasing as the need of high speed processors are increasing. The Vedic multiplication technique is based on 16 Vedic sutras or aphorisms, which are actually word formulae describing natural ways of solving a whole range of mathematical problems [1]. The mathematical operations using, Vedic Method are very fast and requires less hardware, this can be used to improve the computational speed of processors. This paper describes the design and implementation of 4x4 bit Vedic multiplier based on Urdhva-Tiryakbhyam sutra (Vertically and Crosswise technique) of Vedic Mathematics using EDA (Electronic Design Automation) tool. The paper is organized as follows. Section 2 describes the basic methodology of Vedic multiplication technique. Section 3 describes the hardware architecture of 2x2 and 4x4 bits Vedic Multiplier (VM) based on Vedic multiplication. Section 4 illustrates the implementation and result of Vedic multiplier module so obtained while Section 5 comprises of Conclusion. Section 6 is the Acknowledgment whereas Section 7 comprises of References.

2. ANCIENT VEDIC METHODS
The use of Vedic mathematics lies in the fact that it reduces the typical calculations in conventional mathematics to very simple ones. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. Vedic Mathematics is a methodology of arithmetic rules that allow more efficient speed implementation. It also provides some effective algorithms which can be applied to various branches of engineering such as computing.

2.1 Vertically & Crosswise Technique
The proposed Vedic multiplier is based on the "Urdhva Tiryakbhyam" sutra (algorithm). These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. In this work, we apply the same ideas to the binary number system to make the proposed algorithm compatible with the digital hardware. It is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and crosswise". It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. The algorithm can be generalized for n x n bit number. Since the partial products and their sums are calculated in parallel, the multiplier is independent of the clock frequency of the processor. The Multiplier based on this sutra has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other conventional multipliers.

To illustrate this scheme, let us consider the multiplication of two decimal numbers 252 * 846 by Urdhva Tiryakbhyam method as shown in Figure 1. The digits on the both sides of the line (say, 2 and 6) are multiplied (6 x 2 = 12) and added with the carry from the previous step (initially, carry=0). This generates one of the bits of the result (i.e. 2) and a carry (i.e. 1). This carry (1) is added in the next step and hence the process goes on. If more than one line are there in one step, all the results are added to the previous carry. In each step, Least Significant Bit (LSB) acts as the result bit and all other bits act as carry for the next step. Initially the carry is taken to be zero.

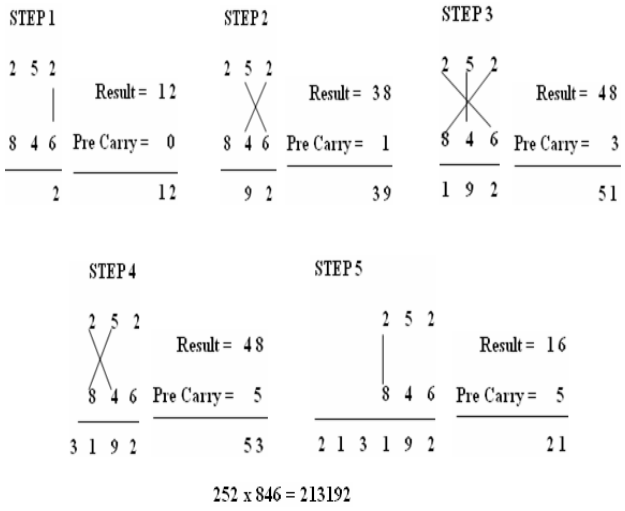

Figure 1: Multiplication of two decimal numbers 252 * 846

3. PROPOSED VEDIC ARCHITECTURE

The hardware architecture of 2x2 and 4x4 bit Vedic multiplier (VM) modules are displayed in the below sections. Here, "Urdhva-Tiryakbhyam" (Vertically and Crosswise) sutra is used to propose such an architecture for the multiplication of two binary numbers. The beauty of Vedic multiplier is that here partial product generation and additions are done concurrently. Hence, it is well adapted to parallel processing. The feature makes it more attractive for binary multiplications. This in turn reduces delay.

3.1 Vedic Multiplier for 2x2 bit

The method is explained below for two, 2 bit numbers *A* and *B* where $A = a1a0$ and $B = b1b0$ as shown in Figure 2. Firstly, the Least Significant Bits are multiplied which gives the Least Significant Bit (LSB) of the final product (vertical). Then, the LSB of the multiplicand is multiplied with the next higher bit of the multiplier and added with, the product of LSB of multiplier and next higher bit of the multiplicand (crosswise). The sum gives second bit of the final product and the carry is added with the partial product obtained by multiplying the most significant bits to give the sum and carry. The sum is the third corresponding bit and carry becomes the fourth bit of the final product.

$$s0 = a0b0; \quad (1)$$

$$c1s1 = a1b0 + a0b1; \quad (2)$$

$$c2s2 = c1 + a1b1; \quad (3)$$

The final result will be $c2s2s1s0$. This multiplication method is applicable for all the cases. The 2x2 bit Vedic multiplier (VM) module is implemented using four input AND gates & two half-adders which is displayed in its block diagram in Figure 3.

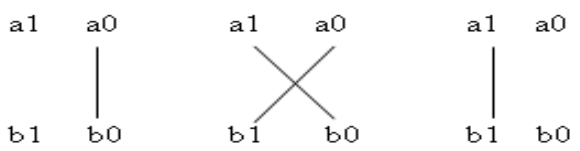

Figure 2: The Vedic Multiplication Method for two 2-bit binary numbers

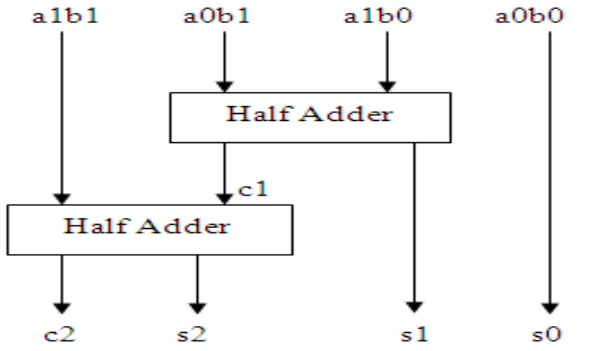

Figure 3: Block Diagram of 2x2 bit Vedic Multiplier (VM)

The same method can be extended for higher no. of input bits (say 4). But a little modification is required as discussed in section 3.2. This section illustrates the implementation of 4x4 bit VM which uses 2x2 bit VM as a basic module.

3.2 Vedic Multiplier for 4x4 bit

Divide the no. of bits in the inputs equally in two parts. Let's analyze 4x4 bit multiplication, say multiplicand A=A3A2A1A0 and multiplier B= B3B2B1B0. Following are the output line for the multiplication result, S7S6S5S4S3S2S1S0. Let's divide A and B into two parts, say "A3 A2" & "A1 A0" for A and "B3 B2" & "B1B0" for B. Using the fundamental of Vedic multiplication, taking two bit at a time and using 2 bit multiplier block, we can have the following structure for 4x4 bit multiplication as shown in Figure 4.

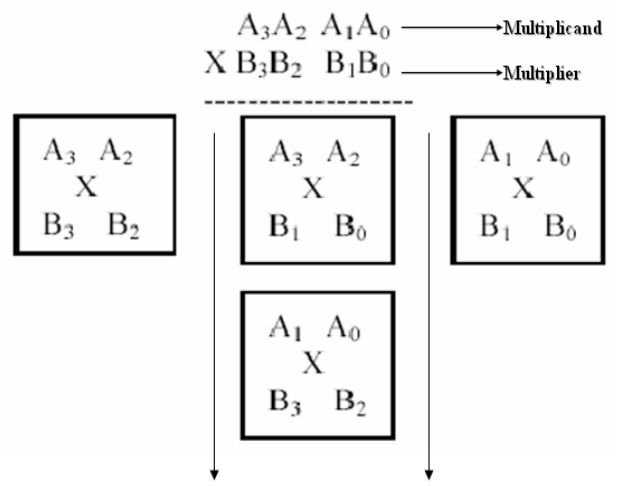

Figure 4: Structure for 4x4 bit Multiplication

Each block as shown above is 2x2 bit multiplier. First 2x2 multiplier inputs are "A1 A0" and "B1 B0". The last block is 2x2 bit multiplier with inputs "A3 A2" and "B3 B2". The middle one shows two, 2x2 bit multiplier with inputs "A3A2" & "B1B0" and "A1A0" & "B3B2". So the final result of multiplication, which is of 8 bit, "S7S6S5S4S3S2 S1S0".

To understand the concept, the block diagram of 4x4 bit Vedic multiplier is shown in Figure 5. To get final product S7S6S5S4S3S2S1S0 four, 2-bit Vedic multiplier (Figure 3)

and three 4-bit Ripple Carry (RC) Adders are required. In this proposal, the first 4-bit RC Adder is used to add two 4-bit operands obtained from cross multiplication of the two middle 2x2 bit multiplier modules. The second 4-bit RC Adder is used to add two 4-bit operands, i.e. concatenated 4-bit ("00" & most significant two output bits of right hand most of 2x2 multiplier module as shown in Figure 5) and one 4-bit operand we get as the output sum of first RC Adder. Its carry "ca1" is forwarded to third RC Adder. Now the third 4-bit RC Adder is used to add two 4-bit operands, i.e. concatenated 4 - bit (carry ca1, "0" & most significant two output sum bits of 2nd RC Adder as shown in Figure 5) and one 4-bit operand we get as the output sum of left hand most of 2x2 multiplier module. Early literature speaks about Vedic multipliers based on array multiplier structures. The arrangement of Ripple Carry Adder as shown in Figure 6 helps us to reduce delay.

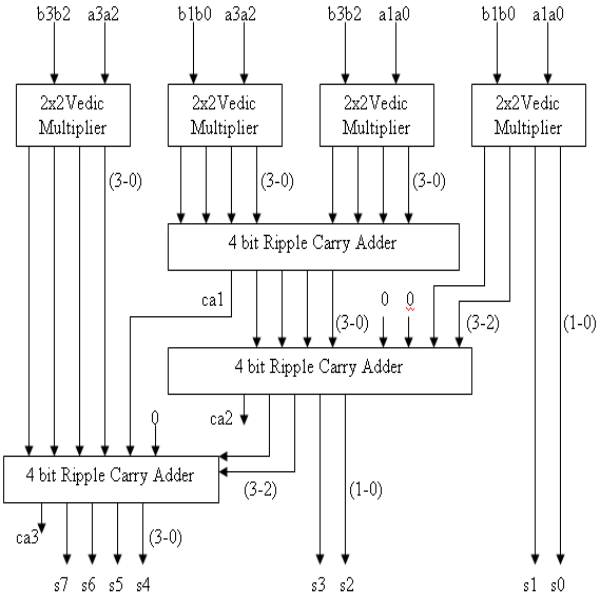

Figure 5: Block Diagram of 4x4 bit Vedic Multiplier (VM)

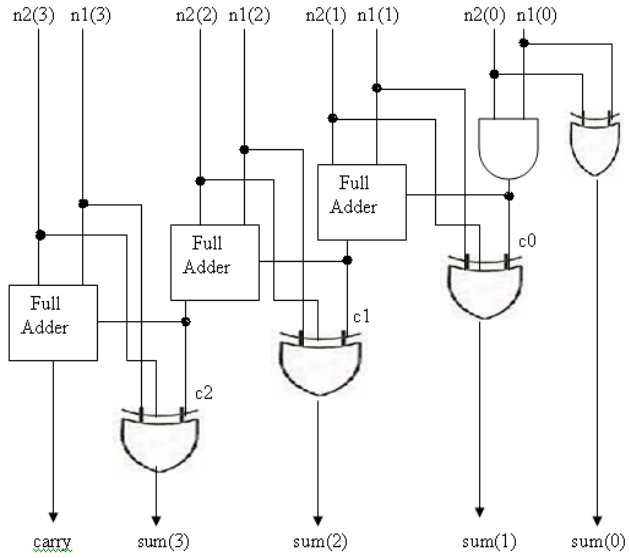

Figure 6: Circuit Diagram of 4 bit Ripple Carry Adder

4. IMPLEMENTATION & RESULTS

In this work, 4x4 bit VM (Vedic multiplier) using "Urdhva Tiryakbhyam" Sutra is implemented in VHDL (Very High Speed Integrated Circuit Hardware Descriptive Language). Logic synthesis and simulation was done using EDA (Electronic Design Automation) tool in XilinxISE12.1i - Project Navigator and ISim simulator integrated in the Xilinx package respectively. Table 1 displays the comparison of synthesis results of the proposed Vedic multiplier with the Conventional multipliers in terms of time delay (in nanoseconds). The combinational path delay obtained for the proposed 4x4 bit Vedic multiplier is 13.102 ns whereas the results of 4x4 bit Array and Booth multipliers have been taken from Umesh Akare et al [16].The performance is evaluated on the Xilinx device family Spartan3, package tq144 and speed grade -5.

Table 1 Comparison of Multipliers (in nanosecond)

Device: Spartan xc3s50a-5tq144	Array Multiplier	Booth Multiplier	Vedic Multiplier
4x4 bit VM	32.001 ns	16.276 ns	13.102 ns

The RTL (Register Transfer Level) schematic of the 4x4 bit Vedic multiplier comprises of four 2x2 bit Vedic multiplier (vedic_multi_struct) v1, v2, v3, v4 and three 4-bit Ripple Carry Adder (rc_adder) v5, v6, v7 as shown in Figure 7 while the simulation results obtained are shown in Figure 8 for verification. In behavioral simulation we have tested for input bits: - "0100" (in decimal number system 4) and "0100" (decimal number system 4) as inputs and we get output as "00001000" (decimal number system 8). The inputs of 4-bits are decomposed into the input of 2-bits. The input for MSB (Most Significant Bit) & LSB (Least Significant Bit) of multiplicand are kh=01 and kl=00, while the input for MSB (Most Significant Bit) & LSB (Least Significant Bit) of multiplier are lh=00 and ll=01. Finally, the output1=00010000, indicates the final 8-bit result. However the rest signals indicate the intermediate results like partial products (sum & carry).

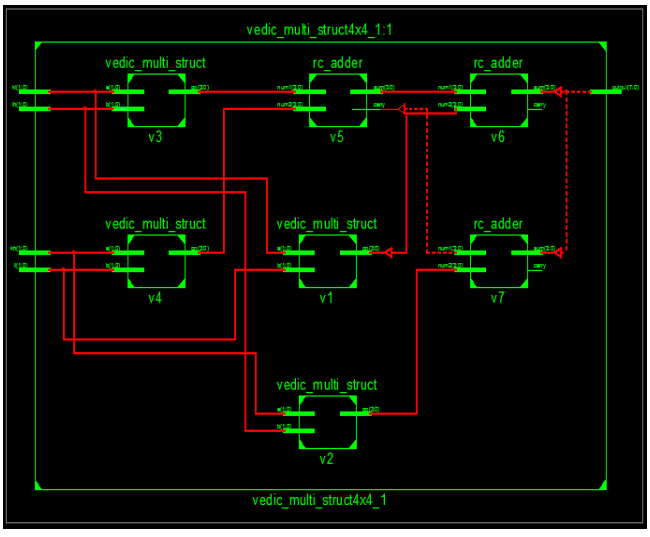

Figure 7: RTL schematic of 4x4 bit Vedic Multiplier

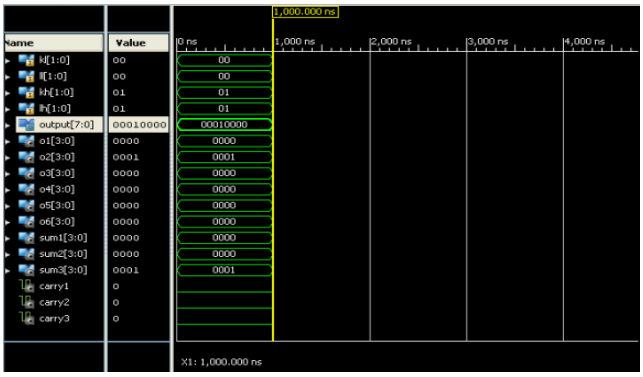

Figure 8: Simulation Result of 4x4 bit Vedic Multiplier

5. CONCLUSION

This paper presents a new method of multiplication "Urdhva Tiryakbhyam" Sutra based on Vedic Mathematics. The design of the proposed 4x4 bit Vedic multiplier is implemented on Spartan xc3s50a-5-tq144 device. The computational path delay of the Vedic multiplier is found to be 13.102 ns. Hence it can be concluded that the performance of the proposed 4x4 bit Vedic multiplier seems to be highly efficient in terms of speed when compared to Conventional multipliers. Reducing the time delay is very essential requirement for many applications and Vedic Multiplication technique is very much suitable for this purpose. The idea proposed here may set path for future research in this direction.

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