

Comparative Analysis of Polynomial FIR Multirate DSP Applications

S. Arunkumar

Department of ECE, P.S.N.A. College of
Engineering and Technology,
Dindigul-624622. India.

P. Ganesh Kumar, PhD.

Professor, Department of ECE, KLN
College of Engineering and
Technology, Madurai, India.

ABSTRACT

Multirate DSP systems in which different parts at different sampling rates. The increase in the sampling interval results in more time available for processing. Decimation generally includes first low-pass filtering the signal and then discarding some of the samples. Zero stuffing is performed in the process of interpolating a discrete-time signal, and then low-pass filtering the resulting signal. The proposed decimator is implemented using MATLAB as standard FIR, Half Band FIR and Nyquist FIR by using the multistage design techniques. The performance of different decimator designs is compared in terms of error and hardware requirements. The results show that the performance of all designs is almost identical but their implementation cost varies greatly in terms of hardware requirements. The hardware saving of 49% to 84% can be achieved by using multistage Nyquist decimator design. Reduced computational work load, lower filter order, lower coefficient sensitivity and noise and less stringent memory requirements.

Keywords: Zero-stuffing, Decimation, MUSIC, aliasing.

1. INTRODUCTION

Sampling rate conversions are needed when systems with different sampling frequencies are to be interconnected. In other cases the sampling rate is changed internally, while the input and output rates are the same. This is done in order to improve the efficiency of the processing. These techniques are commonly used in narrow band low-pass, high-pass, and band-pass filters, filter banks, so called transmultiplexers. (converters between FDM and TDM systems), and delays of a fraction of the time interval. Polynomial-based interpolation is that it can be efficiently implemented using the so called Farrow structure [1]. This method is based on the relationship between the Taylor series of the approximating continuous-time signal and the Farrow structure as introduced in [2]. It enables us to design the FIR filters in the Farrow structure separately. A new synthesis technique for polynomial-based interpolation filters was presented. In this technique, the linear-phase Type II and Type IV FIR filters in the modified Farrow structure are designed separately. Consequently, the design of the interpolation filter reduces to the design of $L+1$ linear-phase FIR filters. The conventional super-heterodyne receiver has very good performance due in part to its discrete components. It uses an external image reject (IR) filter and an external, narrow-band, IF channel filter within the receive path [3].

Polyphase decomposition results in reduction of computation complexity in FIR filter realization [4]. The recursive structure, proposed in [5], also known as the *cascaded integrator-comb (CIC filter)*, consists of two main sections: an integrator section and a differentiator section separated by a down-sampler. The non-recursive structure is realized by cascading $\log_2 M$ identical filters $(1 + z^{-1})^K$ each down-sampled by a factor of 2 [6]–[7]. A new efficient structure for a sharpened comb factor-of-decimation filter is proposed. The structure consists of two main sections: a cascade of comb filters followed by down-sampling with a factor M_1 , and a sharpened comb filter followed by downsampling with a factor M_2 where $M = M_1 M_2$. Over sampled filter banks are used to minimize aliasing by reducing the number of significant aliasing terms [8], [9]. This paper presented an approach for designing low-delay nonuniform filter banks. The low delay is achieved by relaxing the linear phase constraints of traditional pseudo-QMF banks.

Digital interpolation filters are often referred to as filters with adjustable fractional delay and are widely used in symbol timing recovery block [10][11][12]. This paper deals with the efficient implementation of conventional Farrow-type polynomial interpolator based on the analysis of optimization constraints. The resulting proposed structure avoids the use of two sub-filters without any performance degradation, leading to a very efficient interpolator. It is shown that the required hardware complexity reduces to about 50 % or more for a moderate polynomial order such as 2 or 3

Digital interpolation filters have been widely employed in Consumer areas to simplify the analog front end, and to improve the overall receiver performances. In this paper, efficient implementation techniques of polynomial interpolation filter has been shown. The proposed method would be useful in that it can improve the interpolation performance for the given limited hardware, or reduce the hardware complexity for the given performance criterion. In [13], only a half band filter is stored in a memory, and the M th-band filters are calculated by using cosine modulation. In this work, we present the interpolated M th-band filters that closely approximate the M th-band eigen filters. The interpolated M th-band filter can be calculated easily from a prototype M th-band eigen filter. This paper deals with the design and implementation of a decimation filter to be used in wideband radio-frequency wireless systems. A decimation filter cascade structure is designed to meet the GSM and DECT standards specifications [14], [15] and to be very efficient computationally. In this work, we have described the architecture, the synthesis and the

hardware implementation of a decimation filter designed for 6-bit data stream input, from a fourth-order sigma-delta modulator adapted for multistandard wireless receiver.

The prototyped filter is based on fifth-order comb filter, one half-band filter stages and a FIR correction filter. Interpolators and decimators are utilized to increase or decrease the sampling rate [16]. For example, in digital audio three different sampling rates are used like 32 KHz for broadcasting, 44.1 KHz for digital CD and 48 KHz for digital audio tape. In video applications, the sampling rates of NTSC and PAL are 14.318 MHz and 17.734 MHz respectively. Down sampler is basic sampling rate alteration device used to decrease the sampling rate by an integer factor [17]. The Nyquist multistage decimator design results in alias removal and improved area utilization ranging from 49% to 84%. So multistage Nyquist decimators are the best to perform down sampling and provide cost effective solutions for DSP based wireless communication applications.

The comb filter is an efficient way to decimate the output of the analog modulator to four times the Nyquist rate [18]. The non-recursive architecture [19] for comb filters has lower power consumption compared with Hogenauer's cascaded-integrator-comb (CIC) architecture [20] especially when the filter orders and decimation ratios are high. In this paper the non-recursive architecture is employed to design the comb filter. Low power techniques have been developed for VLSI implementation of the non-recursive architecture. A low-power fifth-order comb decimation filter with programmable decimation ratios (16 and 8) and sampling rates (12.8 MHz and 44.8 MHz) has been presented for GSM and DECT applications. Low power consumption is achieved by the following approaches: 1) the non-recursive architecture for comb decimation filter is employed; 2) unnecessary computation is eliminated with polyphase implementation of each stage.

2. POLYNOMIAL INTERPOLATION AND DECIMATION

2.1. Efficient Implementation of Polynomial Interpolation Filters for Full Digital Receivers.

Digital interpolation filters are often referred to as filters with adjustable fractional delay and are widely used in symbol timing recovery block [10][11][12]. This paper deals with the efficient implementation of conventional Farrow-type polynomial interpolator based on the analysis of optimization constraints. The resulting proposed structure avoids the use of two sub-filters without any performance degradation, leading to a very efficient interpolator. It is shown that the required hardware complexity reduces to about 50 % or more for a moderate polynomial order such as 2 or 3.

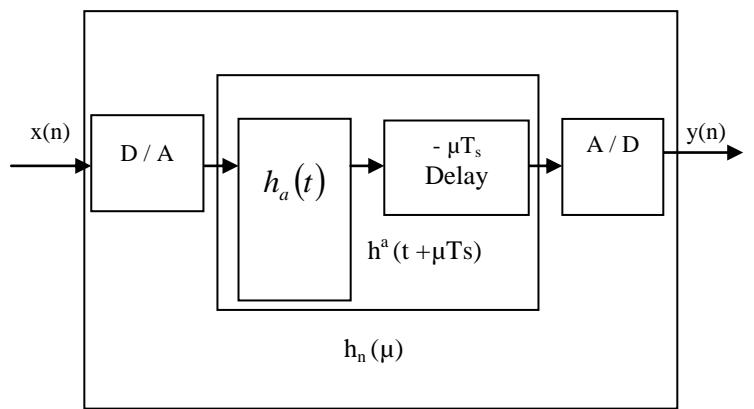


Fig. 1 Conceptual model for Digital Interpolation Filter

For a given fractional delay value μ and input sequence $x(n)$, digital Interpolation filter which produces an output $y(n)$ delayed by $-\mu T_s$, where T_s is the input sampling time, can be modeled as depicted in Fig. Input sequence $x(n)$ is converted to a discrete time signal $\sum_k x(k) \delta(t - kT_s)$ through an ideal D/A converter, and is approximated to its original analog signal by filtering it with analog interpolation filter $h_a(t)$. The output delayed by $-\mu T_s$ is transformed again to digital signal $y(n)$ via an ideal A/D converter. In what follows we assume $T_s = 1$ for simplicity. Let impulse response of equivalent discrete interpolator shown in Fig.1 be $h_n(\mu)$. Then it can be represented as

$$h_n(\mu) = h^a(t) \Big|_{t \leftarrow n + \mu} \quad (1)$$

Now assume that $h^a(t)$ satisfies the following properties :

[1] $h^a(-t) = h^a(t)$.

[2] $h_a(t)$ is non zero only in the interval

$$-N \leq t \leq N.$$

Digital interpolation filters have been widely employed in Consumer areas to simplify the analog front end, and to improve the overall receiver performances. In this paper, efficient implementation techniques of polynomial interpolation filter has been shown. The proposed method would be useful in that it can improve the interpolation performance for the given limited hardware, or reduce the hardware complexity for the given performance criterion.

2.2. Optimized Design of Decimator for Alias Removal in Multirate DSP Applications

Interpolators and decimators are utilized to increase or decrease the sampling rate [16]. For example, in digital audio three different sampling rates are used like 32 KHz for broadcasting, 44.1 KHz for digital CD and 48 KHz for digital audio tape. In video applications, the sampling rates of NTSC and PAL are 14.318 MHz and 17.734 MHz respectively. Down sampler is basic sampling rate alteration device used to decrease the sampling rate by an integer factor [17]. In this paper, decimator is implemented and analyzed using different designs. So multistage Nyquist decimators are the best to perform down sampling

and provide cost effective solutions for DSP based wireless communication applications. When decimating, the bandwidth of a signal is reduced to an appropriate value so that minimal aliasing occurs when reducing the sampling rate. An acceptable transition width needs to be incorporated into the design of the low pass filter used for decimation along with pass band ripple and finite stop band attenuation. In this proposed work decimator is designed using 0.01 transition width, 0.02dB pass band ripples, 60dB stop band attenuation and decimation factor of 8.

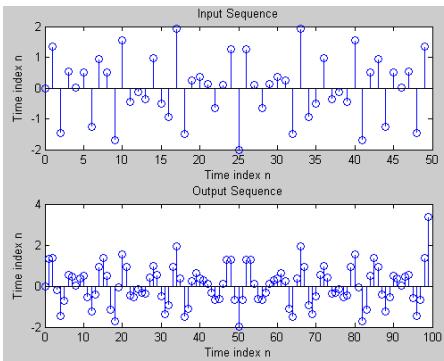


Fig.2 Interpolation Design and Implementation

3. RESULTS AND DISCUSSIONS

Digital interpolation filters have been widely employed in consumer electronics areas to simplify the analog front end, and to improve the overall receiver performances. The decimator is implemented and analyzed using different designs. The results show of the all designs is almost identical but their implementation cost varies greatly in terms of hardware requirements. The Nyquist multistage decimator design results in alias removal and improved area utilization ranging from 49% to 84%.

4. CONCLUSION

Multistage Nyquist decimators are the best to perform down sampling and provide cost effective solutions for DSP based wireless communication applications. Digital interpolation filters have been widely employed in Consumer areas to simplify the analog front end, and to improve the overall receiver performances. In this paper, efficient implementation techniques of polynomial interpolation filter has been shown. The proposed method would be useful in that it can enhance the antialiasing, antiimaging, and zero stuffing are employed in **MUSIC** systems such as **Dolby** stereo sound, **QUBE** and **UFO** sound systems.

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