Implementation of Code Division Multiple Access using Asynchronous Sequential Techniques

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ABSTRACT
Digital Code Division Multiple Access (CDMA) scheme allows many users to transmit and receive at the same time using a single channel. CDMA techniques can use synchronous or asynchronous mechanisms. The work in this paper uses the less studied asynchronous mechanism. The transmitter and receiver are synchronized with the help of a delay element. The simulation and synthesis carried out using VHDL tool shows minimum power consumption and an increase in the overall speed of the system.

General Terms
Code Division Multiple Access, Simulation, Synthesis, Asynchronous.

Keywords
CDMA, correlator, spreading sequence.

1. INTRODUCTION
CDMA technique is based on the spread spectrum communication, originally developed for military applications. For a spread spectrum signal the transmission bandwidth is much wider than the bandwidth of the original signal. In a CDMA communication system, a unique binary spreading sequence (a code) is assigned for each call to every user. The users signal is multiplied by the assigned code and "spread" onto a bandwidth much wider. All the active users share the same frequency spectrum at the same time.

The signal of each user is separated or "de-spread" from the others at the receiver using a correlator key with the associated code sequence. Spreading codes of a spreading sequence can be divided into pseudo-noise (PN) code and/or orthogonal codes. PN codes are pseudo-random codes generated by a feedback mechanism using shift registers. In a CDMA transmitter, the information is modulated by a spreading code, and in the receiver it is correlated with a replica of the same code.

Thus, low cross-correlation between the desired and interfering users is important to suppress the multiple access interference. Good auto-correlation properties are required for reliable synchronization and reliable separation of the multipath components. Having good auto-correlation properties is also an indication of good randomness of a sequence, which allows us to connect other important sequences properly.

The design procedure of CDMA has not been studied fully by researchers. This paper presents a brief idea about multiuser detection techniques [2], [5] followed by a technique for efficient use of bandwidth in a wireless communication system. This design method requires less circuitry for implementation and provides better simulation results. The modulation process, i.e., using binary phase shift keying (BPSK) at the output of transmitter is shown in Figure 1 to regenerate the signal strength in its original form after being attenuated by the interferences of several users. Different amount of time delay and attenuation factors provides the multipath diversity, where the diversity order is equal to the number of combined multipath components. The implementation of Transmitter and Receiver side of the circuit were coded using VHDL.

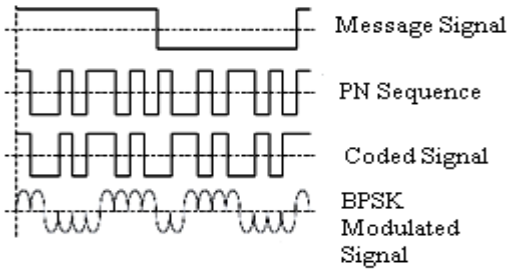

Fig. 1 Modulation using BPSK

2. DESIGN
The CDMA system consists of a transmitter and receiver and is shown in Figures 2.1 and 2.2. The transmitter receives data from three users, designated as user1, user2 and user3. The information from the three users is mixed by the transmitter in such a way as to generate single output. The single output is also known as channel/channel bandwidth. The Receiver receives the transmitted data from Transmitter and then decodes the signal into original form and extracts one desirable datum. In this system, the transmitter and receiver are assumed to be synchronized using internal clock pulses (delay element) to both transmitter and receiver [3].

If we include asynchronous sequential techniques instead of synchronized clock pulses in above system, the speed of the overall system is increased and it reduces the power consumption [4]. The asynchronism used in CDMA system is somewhat difficult to achieve, but it gives better performance than that of synchronous sequential circuits. Transmitter receives data from three users i.e., user1, user2 and user3 and it includes three kinds of PN code sequences (seq1, seq2 and seq3 respectively) for each user. It also needs three exclusive OR gates for each transmitting signal/channel. Each data is XORed with the corresponding PN sequence and the signals are summed up to generate 2 bits width Tx_{Out} output signal as shown in Figure 2.3 [10], [11].

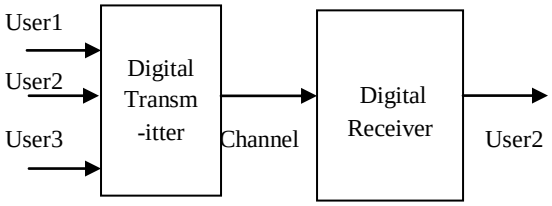

Fig. 2.1 Digital CDMA system

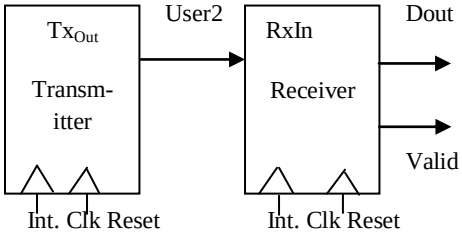

Fig. 2.2 Digital CDMA system with Clk & Reset

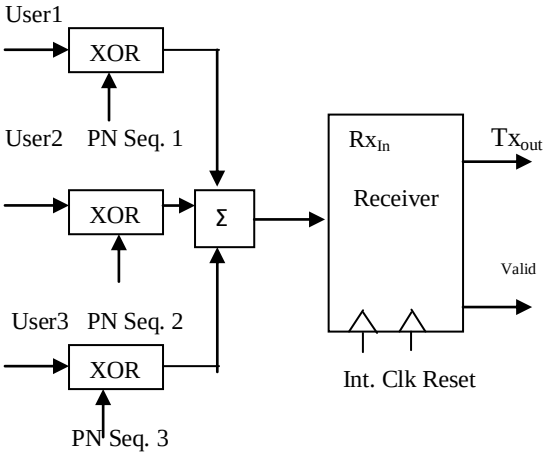

Fig. 2.3 CDMA design with number of inputs

During rising edge of the clock pulse, the Tx_{Out} signal starts synchronizing. As the length of the PN code is 127 (i.e., 7 bit PN sequence, having 2^8-1 possible combinations), so it takes 127 cycles to send 1 bit datum for each user. Delay element made of shift registers and a single multiplexer are shown in Figures 2.4 and 2.5 of synthesized RTL Viewer and Technology Schematics respectively, whose output is equal to 1 [6]. In order to indicate the timing of the PN code starting point, the synchronizing signal $SYNC_{OUT}$ is asserted.

In the CDMA design, there is no such $SYNC_{OUT}$/$SYNC_{IN}$ signal between transmitter and receiver. Thus the receiver shall have a mechanism to find out the starting point of a PN Sequence (generated from feedback shift registers). The transmitter output (Tx_{Out}) sends 2 bits signal to the receiver input Rx_{In}. The signal from Tx_{Out} to Rx_{In} is actually sum of signals of user1, user2 and user3. The preferred user data has to be extracted from the Rx_{In} signal according to the 2 bits width user inputs (01 for user 1, 10 for user 2, 11 for user3) and any data extracted out of such combinations will be the output of D_{out} pin [1], [2].

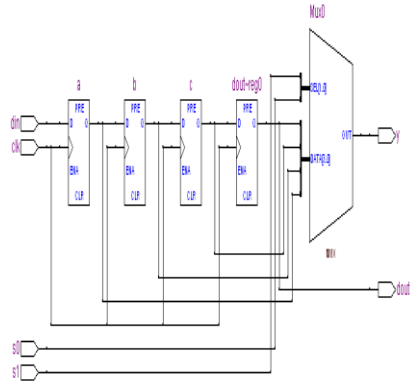

Fig. 2.4 RTL Viewer of delay circuit

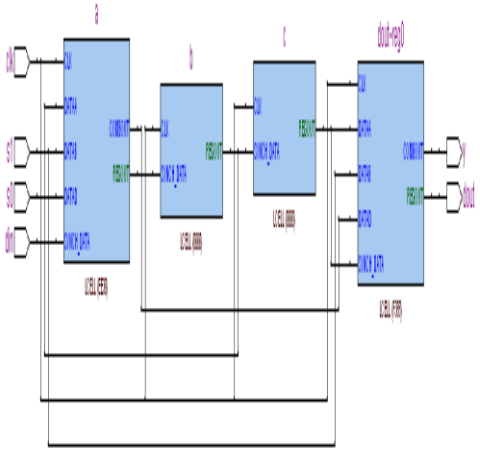

Fig. 2.5 Technology Map Viewer of delay circuit

3. ADVANCED DESIGN OF CDMA

Figures 3.1 and 3.2 depict a configuration in which there are 3 users, each transmitting a different, orthogonal, PN sequence. For each user, the data stream to be transmitted, $User_n$ (where n = 1, 2 and 3) is Exclusive ORed with the spreading code for that user PN Seq_n (where n = 1, 2 and 3). The spreading sequence is then modulated for transmission over the wireless channel [8], [13]. Because of multipath effects, the channel generates multiple copies of the signal, each with a different amount of time delay (τ_1, τ_2, τ_3) and each with a different attenuation factor (a_1, a_2, a_3). At the receiver end, the combined signal is demodulated. The demodulated chip stream is then fed into multiple correlators, and in each correlator, the received signal is correlated by a spreading code, which is time-aligned with the delay of multipath signal.

These signals are then weighted and combined by a maximal ratio combiner, which means that, each signal is weighted by the path gain (attenuation factor) [9]

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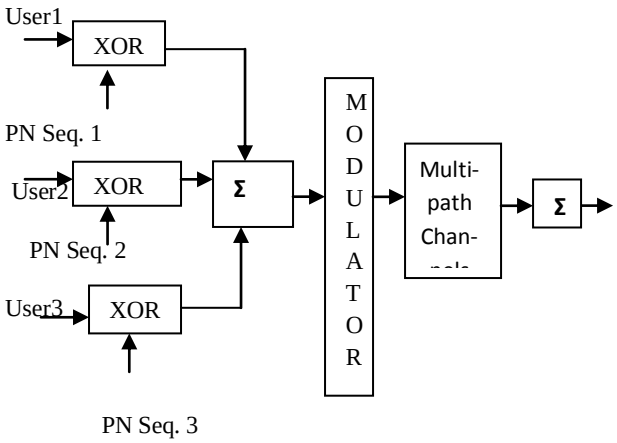


Fig. 3.1 Design of CDMA Transmitter

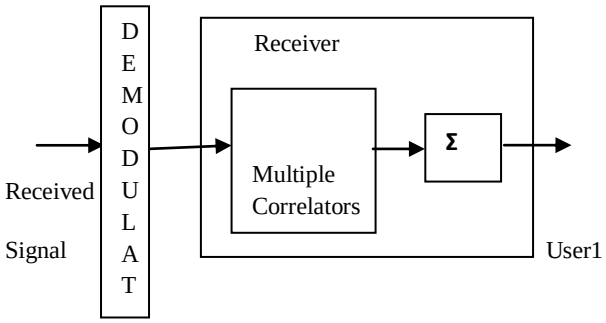


Fig. 3.2 Design of CDMA Receiver

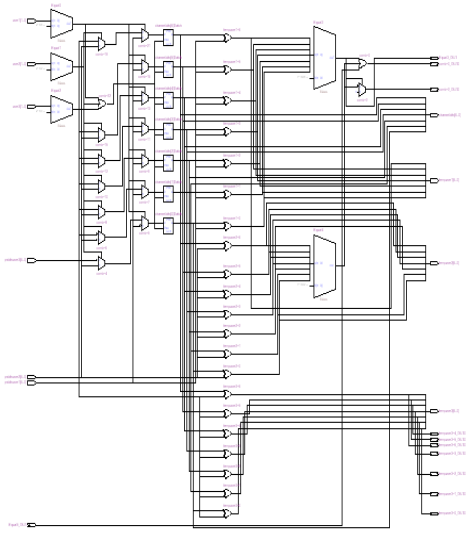


Fig. 3.3 Display RTL Viewer of CDMA Transmitter (User Inputs & PN Sequences) and Channel

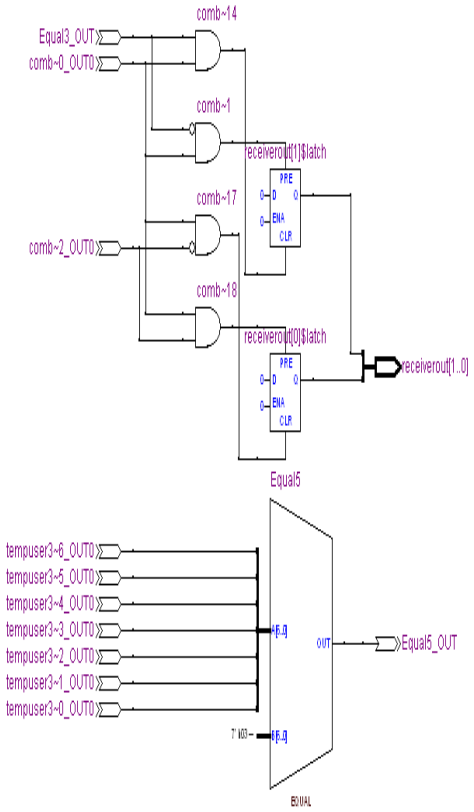


Fig. 3.4 Display RTL Viewer of CDMA Receiver

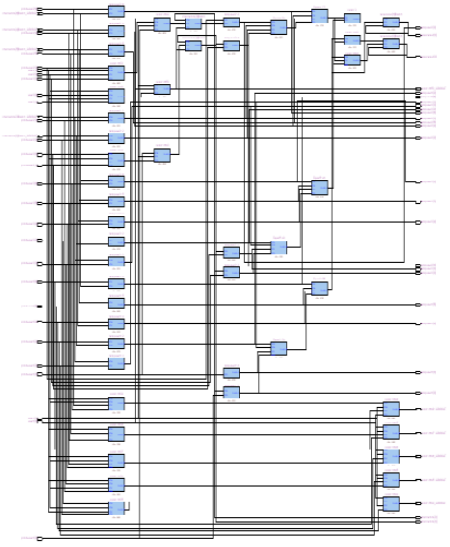


Fig. 3.5 Technology Map Viewer of CDMA Transmitter and Receiver

Let us assume that the receiver is attempting to recover the data of User1. The incoming signal is Exclusive ORed with spreading code of User1 and then demodulated [14]. The effect is to narrow the bandwidth of that portion of the incoming signal corresponding to User1 to the original bandwidth of the unspread signal, which is proportional to the data rate. The remainder of the incoming signal is orthogonal to the spreading code of User1, the unwanted signal energy remains spread over a large bandwidth and the wanted signal is concentrated in a narrow bandwidth. The band pass filter at the demodulator, therefore, recovers the desired signal

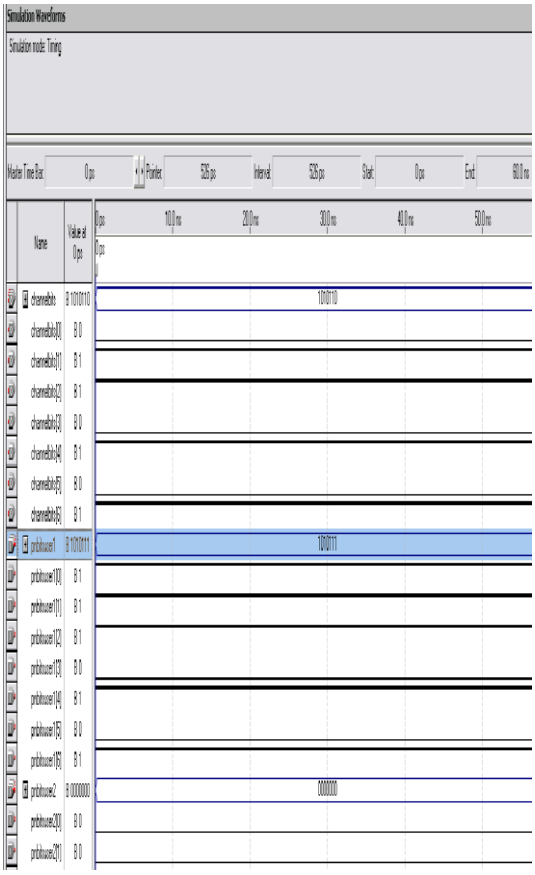
correctly. The synthesized RTL Viewer and Technology Schematics are shown in the Figures 3.3, 3.4. and 3.5 respectively.

4. SIMULATION ENVIRONMENT

Simulation allows us to test a design thoroughly to ensure that it responds correctly in every possible situation before we program or configure a device.

Depending on the type of information needed, one can perform functional or timing simulation with a simulator [6], [7]. Functional simulation tests only the logical operation of a design by simulating the behavior of flattened netlists extracted from the design files, while timing simulation uses a fully compiled netlist containing timing information to test both the logical operation and the best or worst case timing for the design in the target device [10].

The simulator used in this study is the Quartus II simulator that allows circuit design using VHDL. The simulated wave forms of the CDMA (transmitter and receiver) and delay element are shown in the Figure 4.1 and Figure 4.2 respectively. The Quartus II development software provides a complete design environment for system-on-chip (SOC) design.



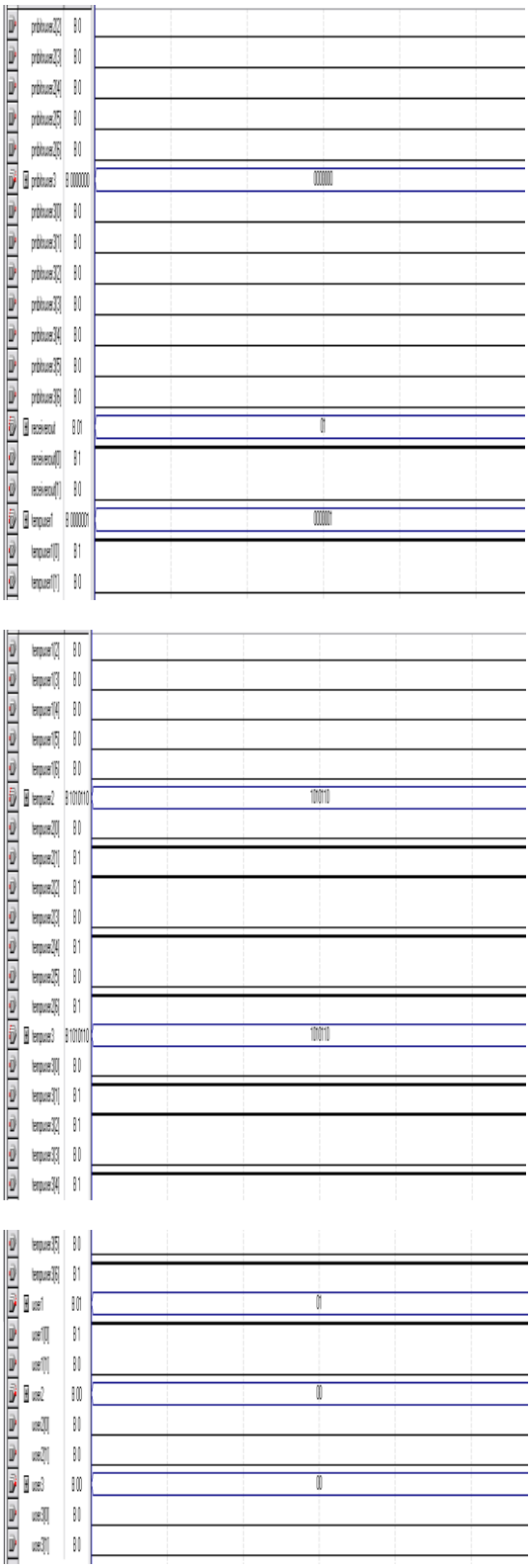


Fig. 4.1 Simulation Waveforms of CDMA Transmitter and Receiver

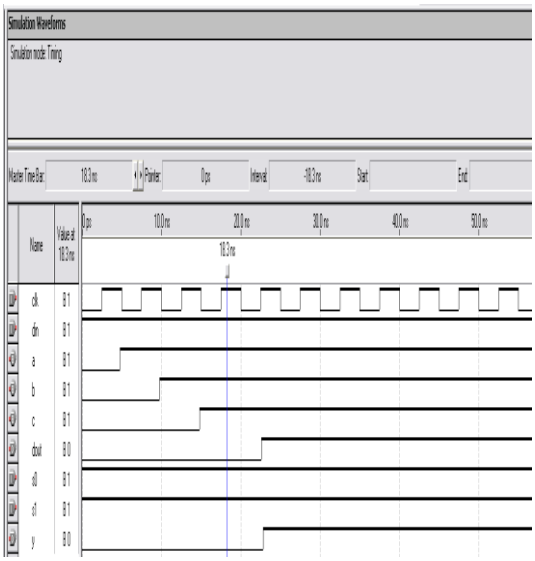


Fig. 8 Simulation Waveforms of Delay Circuit

5. FUTURE PROSPECTS

In this paper a technique for CDMA was presented that minimized the interference of several users by sharing the same kind of bandwidth. The higher cost of bandwidth is taken care of by utilization of the bandwidth in an efficient manner. However, the implementation is being considered for a worst case, where the bandwidth is not utilized fully to test for any problems during reception of several users. The sharing of channel increases the overall performance of the system.

Asynchronous logic seems to be winning niches in the digital electronics business within the next few years. It will share circuit boards with clocked chips and integrated circuits with clocked sub circuits. It is likely to become established as a viable alternative technology in many areas and the technology of choice for some.

6. CONCLUSIONS

This design procedure of CDMA finds applications in multiple access modes to minimize multipath interference by efficient use of bandwidth. The technique used here is a modified version of RAKE receiver and by introducing asynchronism for an increase in speed and reduction in power consumption.

7. REFERENCES

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