Hardware Description of Multi-Directional Fast Sobel Edge Detection Processor by VHDL for Implementing on FPGA

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ABSTRACT
The VHDL is an appropriate Hardware Description Language (HDL) for providing hardware models of practical image processing algorithms. The aim of this paper is to present hardware architecture of Sobel edge detection algorithm for implementing on field programmable gate array (FPGA) chips. The proposed architecture calculates the edges of gray scale images in four directions; vertical, horizontal, right diagonal and left diagonal. Simulation results and synthesizing proposed Sobel edge detection processor on Xilinx Spartan3 XC3S200 FPGA chip demonstrate the efficiency of proposed architecture for edge detecting of gray scale 1024×1024 images for real-time image processing applications.

General Terms
FPGA, Application Specific Processors, Image Processing.

Keywords
Hardware Description, Edge Detection, Sobel Algorithm, VHDL, FPGA.

1. INTRODUCTION
Hardware implementation and description is one of the most important issues in employing edge detection approaches for real-time image processing applications such as image segmentation, pattern recognition and texture analysis. Task processing speed is a key designing issue for hardware implementation of edge detection algorithms which also depends on the type and nature of algorithms and their suitability for hardware implementing. Although many algorithms were introduced for different schemes of image processing applications but due to their complexity and long processing time, are not considered for hardware implementing. Generally, simple and efficient algorithms are considered for real-time and fast hardware implementing.
There are some well-known methods for edge detection such as Prewitt, Canny, Sobel, and Roberts algorithms which are different in terms of performance on hardware, speed and simplicity. The Sobel operator is mainly used for hardware implementing due to efficiency and simple mathematical model that make it easy for real-time edge detection applications [1].
The introduction of Hardware Description Languages (HDLs) such as VHDL [2] provided an interesting modeling and

simulation environments for fast prototyping of digital circuits and systems on field programmable gate array (FPGA) chips.
The FPGA technology [3] is quit mature for digital signal and image processing applications [4]. The FPGA devices provide fully programmable system-on-chip environments by incorporating the programmability of programmable logic devices and the architecture of gate arrays. They consist of thousands of logic gates and some configurable logic blocks which make them an appropriate solution for prototyping the application specific integrated circuits with dedicated architectures for specified digital signal and image processing applications.
The FPGA technology has been received much attention by digital electronic engineer for implementing image processing applications. In [5] a new technique for face detection and lip feature extraction was proposed and implemented on field programmable gate array. Design and implementation of a video image edge detection system based on FPGA was presented in [6]. An improved Canny edge detector and its realization on FPGA was presented in [7]. Implementation of FPGA based architecture of Prewitt edge detection algorithm using Verilog HDL was proposed in [8]. Image edge detection based on FPGA was described in [9]. A novel FPGA-based architecture for Sobel edge detection operator was presented in [10]. Performance analysis of FPGA based Sobel edge detection operator was described in [11].
In this paper a FPGA based hardware architecture for implementing a real-time system for image edge detection based on Sobel operator is considered. In proposed architecture, the edges of images are detected separately in four directions; left, right, left diagonal and right diagonal. Furthermore, in two cases, one of the algorithm outputs is the resultant of vertical and horizontal directions and another is the resultant of left diagonal and right diagonal directions. These outputs could be used depends on the application purpose.
The size of input image is 1024×1024 pixels in gray scale where each pixel is represented by 8 bits which means 256 intensity levels are considered during pixel processing. The output has six gray scale images with 1024×1024 pixels considering 256 gray levels.
The rest of the paper is organized as follows; Section 2 describes Sobel edge detecting algorithm. Hardware architecture of

proposed processor is presented in section 3. FPGA implementation of Sobel edge detection method and some simulation results are presented in section 4 and finally the paper is concluded in section 5.

2. SOBEL EDGE DETECTION METHOD

This section presents the Sobel approach for image edge detection. Generally edges are significant local changes in a typical image and are important features for analyzing images. Edge detection is frequently considered as the first step for image information recovery. In gradient based edge detection approaches, for a typical image array *f(x,y)* the gradient of location *(x,y)*, shown in Figure 1, is defined as follows.

$$\nabla f = \left[\left(\frac{\partial f}{\partial x} \right)^2 + \left(\frac{\partial f}{\partial y} \right)^2 \right]^{\frac{1}{2}} \quad (1)$$

This hardware implementation of (1) is difficult and not desirable coming from the computational burden required for square roots. An alternative approach is to approximate the gradient absolute values:

$$\nabla f = \left| \left(\frac{\partial f}{\partial x} \right) \right| + \left| \left(\frac{\partial f}{\partial y} \right) \right| \quad (2)$$

Computation the gradient of an image is based on obtaining partial derivatives $\frac{\partial f}{\partial x}$ and $\frac{\partial f}{\partial y}$ for every image pixel location [1].

The Sobel edge detection consists of taking 3 by 3 masks and convolving them over the image, shown in Figure 2. The 3×3 image region shown in Figure 2 represents the gray levels in a neighborhood of a typical image. The kernel coefficients contain Sobel method as shown in Figure 3. For instance for A=1 and B=2 the Sobel operator will act. The mentioned method calculate gradient just in vertical and horizontal direction but for more accuracy we can do this in diagonal directions. The gradient calculation mask in diagonal directions is shown in Figure 3. The gradient of the image in all pixels and in all directions should be calculated for detecting the edges. Therefore four parameters (E_V, E_H, E_{DL}, E_{DR}) are considered for each pixel in original image that need the eight neighbors of that pixel. For pixels in margin of original image it is impossible to do these calculations because there is no mentioned eight neighbors for this pixels. There are two ways in these cases ; spotting hypothetical required neighbors (black or white) for that pixel and calculate the gradient for the pixel or spotting constant value gradient for these pixels that mean there is no edge in these pixels.

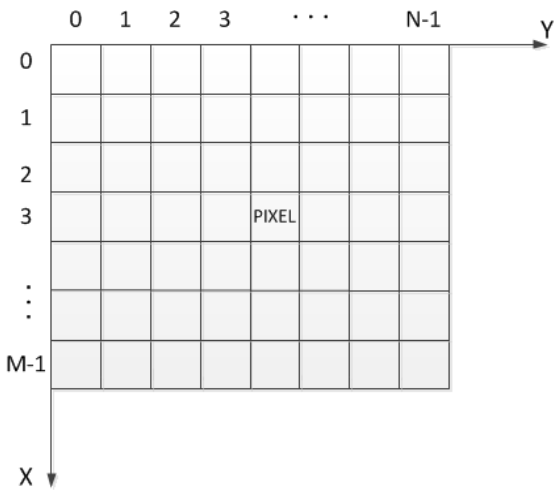


Fig 1: A typical image array

P1	P2	P3
P4	P5	P6
P7	P8	P9

Fig 2: A typical 3×3 image mask

E_H =

A	B	A
0	0	0
-A	-B	-A

E_V =

-A	0	A
-B	0	B
-A	0	A

E_{DL} =

0	A	B
-A	0	A
-B	-A	0

E_{DR} =

B	A	0
A	0	-A
0	-A	-B

Fig 3: The four considered parameters for each pixel

3. HARDWARE ARCHITERCTUR

This section presents the hardware ASIC architecture for implementing real-time edge detection on FPGA considering Sobel algorithm. The proposed architecture is for gray scale images where each pixel is represented by eight bits providing one byte. Therefore, the intensity range changes from 0 to 255. The proposed architecture is shown in Figure 4 which consists of several operational blocks described in rest of this section in details.

3.1 Array Generator

The input image data comes from a digital camera in serial format using a synchronous clock. The input data is entered into array generator block and this block arrange data in 3*3 array format. Then gradient calculations on input data should be done [6]. Three cascade shift registers shown in Figure 5 performs the gradient calculations. For example, suppose that the size of input arrays is M×N where M and N are the total numbers of rows and columns of digital image respectively. The size of first shift register should be three pixels and size of second and third ones should be N pixels. At every rising edge of clock, one input pixel enters into shift registers of array generator. Therefore after 2N+3 clocks the specified pixels (P1 to P9 in Figure 5) can be used as the input pixels frame where P5 is the center pixel. This deduction isn't always true because after many clocks the pixels in column N-1 and N-2 (suppose the number of columns is 0 to N-1) may be located in P1 place that produce wrong input pixels frame. For avoiding these wrong cases another block is used called controller.

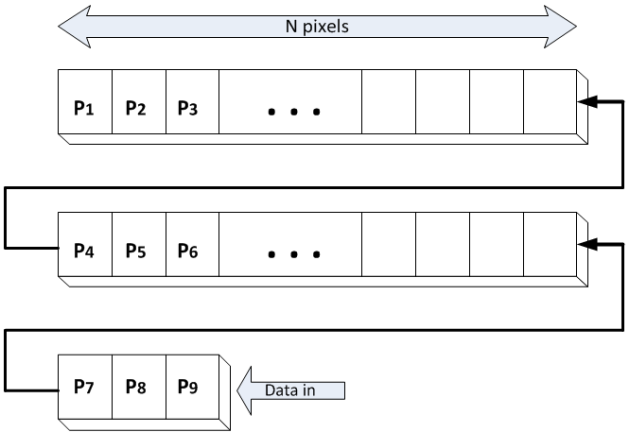


Fig 5: The array Generator

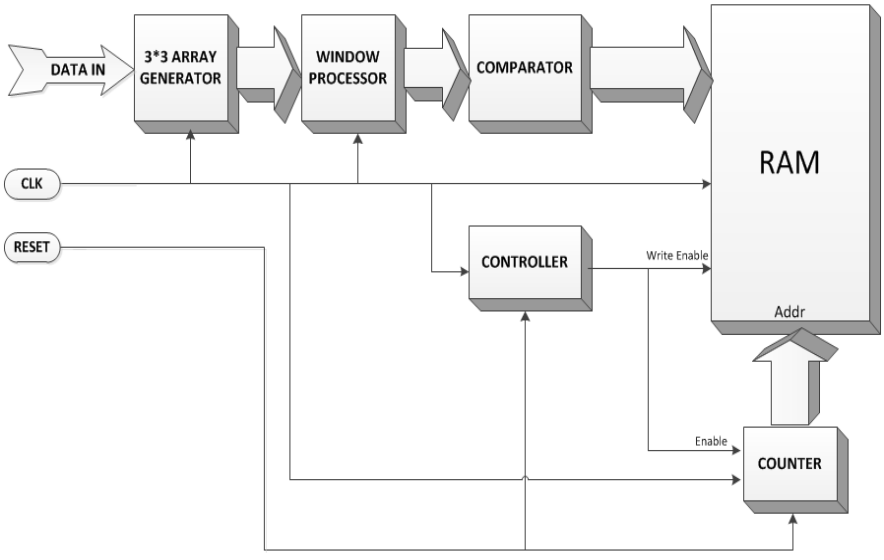


Fig 4: The hardware architecture of implementing Sobel algorithm

3.2 Window Processor

The produced pixels frame (P1 to P9) by the 3×3 Array Generator block is the input of Window Processor block which calculates the gradient values based on Sobel operator for pixel P5 in all directions for detecting edges. Therefore four parameters (E_V, E_H, E_{DL}, E_{DR}) will be produced for each frame pixels, Figure 6. This block contains four segments that each of them calculates the gradient in one direction and then the gradients in four directions are produced concurrently, shown in Figure 7. The block outputs may be positive, negative or zero where the absolute value of them is in integer range 0 to 1020.

3.3 Comparator

The outputs of window processor enter to comparator block, Figure 8. This block has three main tasks; taking the absolute value of the four inputs, calculating the resultant value in two cases separately as the first is sum of the absolute value of E_H and the absolute value of E_V and the second is sum of the absolute value of EDL and the absolute value of the E_{DR} and finally performing thresholding on all results so if the each result exceeds from 255 then the result is fixed in 255.

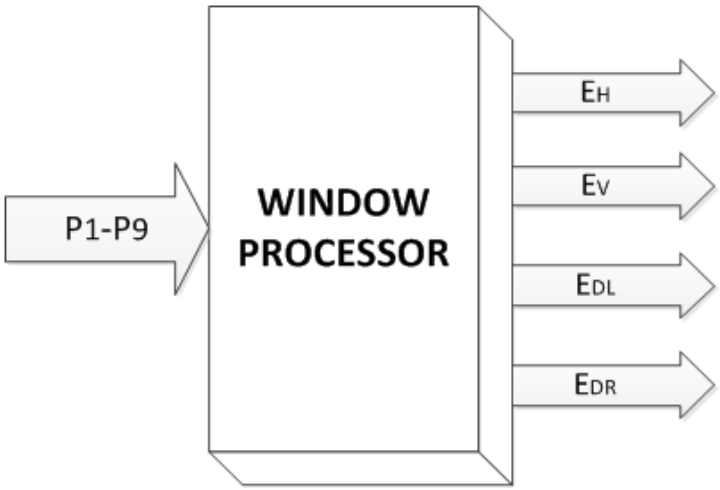


Fig 6: The window processor

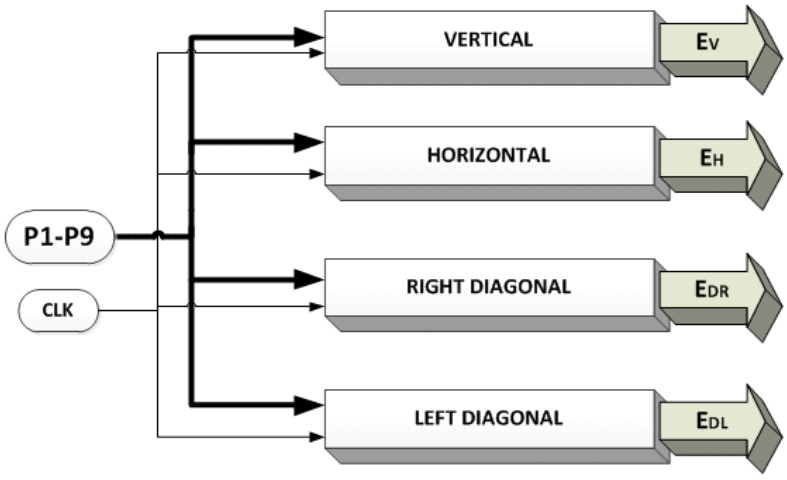
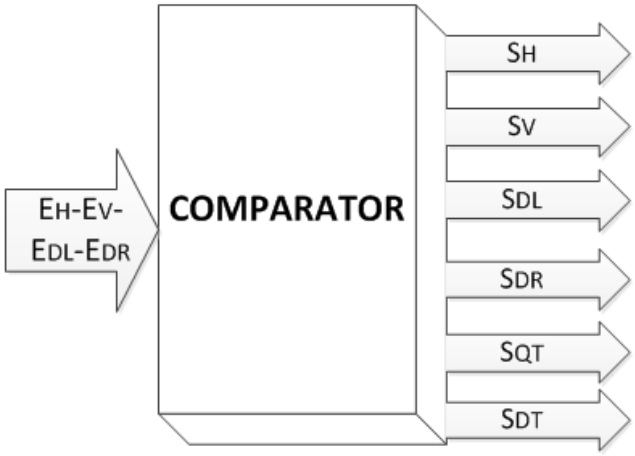


Fig 7: The architecture of window processor



3.4 Controller

Controller is the main block of this architecture. It decides when the output data of comparator should be saved in the RAM block. In other words it recognizes that the output data is valid or not. This block works based on the input clock where it can recognizes when the input pixels frame is valid. Furthermore, it controls the counter that generates the addresses for the RAM block.

3.5 Counter

This block produced appropriate addresses for the RAM block to save the resultant output images pixels data from the comparator. As the width of pixels are eight bits, so for every address six 8-bit data are saved.

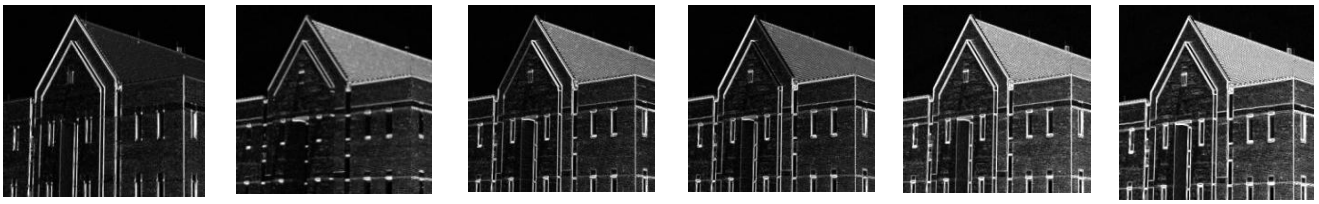
4. SIMULATION RESULTS

This section provides some simulation results for implementing the proposed Sobel edge detection processor on Xilinx Spartan3 XC3S200 FPGA chip. The ISE9.2 is used for synthesizing the VHDL modeling codes. The device utilization summary is shown in Table 1. The maximum clock frequency is 111.97 MHz on this chip. For providing simulation results the ModelSim and Matlab software are used. Three gray scale 1024×1024×8 bits are used as test-bench images for evaluating the proposed processor. The simulation results for all images are presented in Figures 9, 10, 11.

Table 1. The device utilization summary

Logic Utilization	Used	Available	Utilization
Number of slice Flip Flops	176	3,840	4%
Number of 4 input LUTs	333	3,840	8%
Number of occupied slices	751	1,920	39%
Total Number of 4 input LUTs	1,448	3,840	37%
Number used as Logic	333		
Number used as Shift registers	1,032		
Number of bonded IOBs	80	141	56%
IOB Flip Flops	8		
Number of GCLKs	1	8	12%

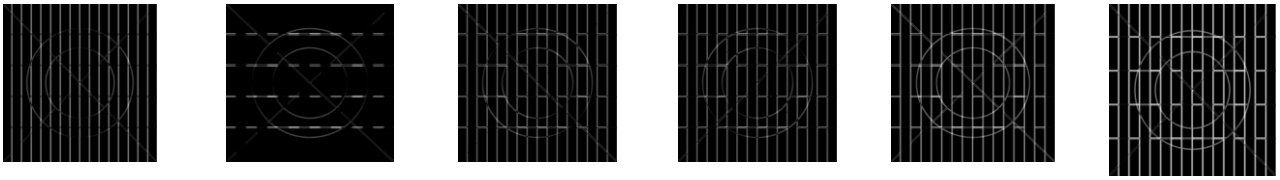
It should be emphasized that the meant of S_{QT} is the resultant (summation and thresholding) of S_V and S_H and the meant of S_{DT} is the resultant (summation and thresholding) of S_{DR} and S_{DL}.



(b) S_V (c) S_H (d) S_{DL} (e) S_{DR} (f) S_{QT} (g) S_{DT}

(a) Original Input Image

Fig 9: Image Test-bench #1



(b) S_V (c) S_H (d) S_{DL} (e) S_{DR} (f) S_{QT} (g) S_{DT}

(a) Original Input Image

Fig 10: Image Test-bench #2

(b) S_V (c) S_H (d) S_{DL} (e) S_{DR} (f) S_{QT} (g) S_{DT}

(a) Original Input Image

Fig 11: Image Test-bench #3

5. CONCLUSION

Hardware description of a real-time edge detection system based on VHDL was considered of high-speed processing in image edge detection. A hardware architecture of Sobel edge detection algorithm for implementing on field programmable gate array (FPGA) chips was proposed. The proposed architecture calculates the edges of gray scale images in four directions; vertical, horizontal, right diagonal and left diagonal. Simulation results and synthesizing proposed Sobel edge detection processor on Xilinx Spartan3 XC3S200 FPGA chip demonstrated the efficiency of proposed architecture for edge detecting of gray scale 1024×1024 images for real-time image processing applications.

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