Performance Evaluation of Dual-X CCII designed using Bulk CMOS and Hybrid approach @ 32nm Technology Node

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ABSTRACT
There is a rapid need to explore the design issues of circuits in deep submicron nodes. This paper presents the design and performance analysis of Dual-X CCII, a widely used analog building block using state of the art Si CMOS and a proposed Hybrid (employing both CMOS and CNFET) configuration at 32nm. Current bandwidths port resistances along with power consumption have been chosen as the parameters for comparison. HSPICE simulator has been used to carry out the extensive simulations at a reduced power supply of ±0.9V..

Keywords
Dual-X Current Conveyor, Si CMOS, CNT, CNFET, Hybrid configuration, Bandwidth, Port Resistance.

1. INTRODUCTION
Silicon CMOS technology has been the primitive source driving the world's economy for the last 40 years. The secret behind this success remains simple i.e. keep delivering more functionality with fewer resources. Device scaling makes this possible. Device scaling not only helps in improving the performance, but also plays a significantly important role in improving the yield as well. As a matter of fact, the latest microprocessors, microcontrollers and memories available in the market today operate well in deep submicron nodes and that's why it is of pivotal importance that the design related issues of analog building blocks is explored at the same level. However, the fact to be remembered is that once the physical gate length of the CMOS is reduced below 65nm, I-V characteristics tend to differ substantially from those operating in micron range. In fact, according to the predictions made by International Technology Roadmap for Semiconductor (ITRS), the fundamental limits of semiconductor physics will soon be reached. And therefore it's of utmost importance that new molecular size devices are explored to help extend the saturating Moore's Law.

Off late, various materials have been investigated, among which, Carbon Nanotubes (CNT's) have emerged as the pioneer candidate for the future of nanoelectronics. It's electrical properties of greater mobility and high current carrying capacity offers the potential for evolving to the next stage of devices and circuits. CNT based FET's i.e. Carbon Nanotube Field Effect Transistors (CNFET's) have been successfully fabricated and reportedly show superior performance as compared to the state of the art Silicon transistors at the same technological node .Thereupon, interests have grown, to evaluate the performance of these relatively newer devices in widely used building blocks of both digital and analog domain.

Another reason that fascinates the ongoing research in CNFET's is its ability to be clubbed with existing CMOS technology on the same chip. In this work, performance of Dual-X Current Conveyor (DXCCI), a widely used analog building block has been evaluated & compared using both CMOS & Hybrid (utilizing CMOS &CNFET on the same chip) approaches. DXCCII is basically a current mode device, used for the implementation of various analog circuits. In fact, the last decade has witnessed a tremendous interest in current mode analog signal processing, as it brings versatility to the already existing domain. Current mode devices generally offers better dynamic ranges, higher frequency response, greater linearity , simpler architectures etc to name a few among the various merits. Though various architectures of this building block exist in micron range, designing it at 32nm, in deep submicron node still remains an unexplored territory and that's what motivated this work.

Paper is organized as follows: After a brief introduction, CMOS based design of DXCCII along with its performance parameters is discussed in Section II. Hybrid design analysis and the performance comparison by varying the CNFET parameter is discussed in the subsequent section, before concluding the paper in section V.

2. CMOS BASED DESIGN OF DUAL-X CCII
Dual-X Current Conveyor is a relatively new but versatile current mode device, utilizing the combined features of second generation current conveyor and inverting second generation current conveyor. The module utilizes two X terminals i.e. Xp(non-inverting X terminal) and Xn (inverting X terminal).Currents at terminals Xp and Xn are reflected to their counterpart Z terminals i.e. Zp and Zn. The block and transistor level implementations of the widely used DXCCII module are shown in Fig 1 & 2 respectively. Though various transistor level implementations of the intended module, exists in literature, the schematic shown in Figure 2 has been chosen, because of its superior high frequency performance. Using standard notation, terminal characteristics of DXCCII shown in Fig.1 can be

$$\begin{bmatrix} I_Y \\ V_{XP} \\ V_{XN} \\ I_{ZP} \\ I_{ZN} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_Y \\ I_{XP} \\ I_{XN} \end{bmatrix}$$

For carrying out the design and evaluating the performance of CMOS Dual-X CCII at 32nm, the tool of Nano-CMOS has been used for customizing the PTM parameters and the dual power supply i.e. V_{DD} and V_{SS} has been set to ±0.9V. Port Resistances, Bandwidth and the Power dissipated have been chosen as the parameters for carrying the comparisons between the designed building blocks using different approaches. Aspect Ratios of the transistors used in the design of CMOS Dual-X CCII along with its evaluated parameters are described in Tables 1 & 2 respectively.

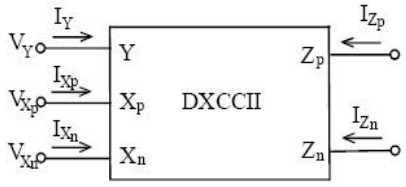

Figure 1 : Block representation of Dual-X CCII

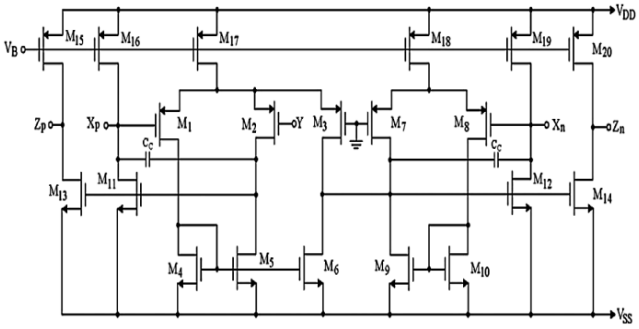

Figure 2 : Transistor level implementation of Dual-X CCII

Table 1 : Width's and Length's of the Transistor's used

MOS TRANSISTOR	LENGTH(nm)	WIDTH(nm)
M_3,M_6,M_7,M_8,M_9,M_{10}	32nm	1152nm
M_{11},M_{12},M_{13},M_{14}	32nm	3456nm
M_1,M_2,M_4,M_5,M_{15},M_{16},M_{17},M_{18} ,M_{19},M_{20}	32nm	384nm

Table 2: Results of the Designed CMOS Dual-X CCII

PARAMETER	DESIGNED Dual-X CCII
Channel Length	32nm
Power Supply	0.9V
Current Gain α	0.99
Voltage Gain β	1.01
3-dB Current BW	8.45GHz
Parasitic elememt at X_p terminal	5.62KΩ
Parasitic elememt at X_n terminal	5.74 KΩ
Parasitic element at Y terminal	655 KΩ
Parasitic element at Z_p terminal	828 KΩ
Parasitic element at Z_n terminal	845KΩ

3. HYBRID DESIGN USING CNFET AND CMOS

Carbon Nanotube Field Effect Transistor's (CNFET's) are generally considered to be the device with the potential to take over from Silicon CMOS, beyond the ITRS roadmap. Various factors like exceptional electrical and structural characteristics such as ballistic transport of electrons and holes, higher drive currents, larger transconductances, lower intrinsic capacitances , high temperature resilience, near ideal sub-threshold slope, strong covalent bonding contribute to its image as the most promising carbon nanostructure material for realizing nanoscale transistors. Furthermore it's operating principle and device structure are quite analogous to the Si CMOS, with the difference that 1-D Carbon Nanotubes (CNT) are employed in the channel region of CNFET. Unlike CMOS, CNFET's are generally designed in terms of Number of CNT's in the channel (N),centre-center distance between two consecutive tubes known as Inter-CNT Pitch (S) and the Diameter of CNT (D_{CNT}). The inter-relationship among the various parameters of the CNFET i.e. diameter of the CNT(D_{CNT}), it's threshold voltage(V_{TH}), number of CNTs in the channel (N), Pitch(S) and the energy gap ($\sum_g$) is given with the help of the following equations:

$$Ch = a(n_1^2 + n_2^2 + n_1 n_2)^{1/2} \quad (1)$$

$$D_{CNT} = Ch / \pi \quad (2)$$

$$\sum_g = 0.84eV / D_{CNT} \quad (3)$$

Variation of the drive current i.e. I_{ds} with the increasing number of CNTs is illustrated in Fig. 3. Since CNFET's enjoy similar infrastructure and could be clubbed with CMOS, utilizing Hybrid configurations (combining CMOS and CNFET on the same chip) for designing and analyzing of different circuits and modules seems to be a good prospect. Hybrid configurations are obtained using NCNFET as a current sink and a conventional PMOS transistor as sourcing device or vice versa i.e. NMOS as the sinking device while PCNFET as the sourcing device. In order to carry out a valid comparison, threshold voltages (V_t) of both CMOS and CNFET based transistors have been kept identical. . The fixed parameters and specifications of the transistors used in the Hybrid CMOS and CNFET design of Dual-X CCII module are specified in Table 3, 4 and 5 respectively

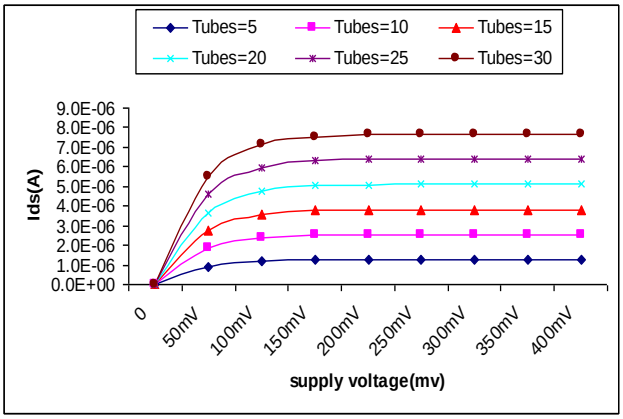

Figure.3: I_{DS} VS Supply Voltage for varying no. of CNT

Table. 3: Design parameters of CNFET

FIXED PARAMETERS	
Oxide Thickness (T_{OX})	4 nm
Power Supply	±0.9V
Gate Dielectric	HfO_2
Dielectric Constant	16
Csub(The coupling capacitance between the channel region and the substrate)	20.0e-12
Efi(The Fermi level of the doped S/D tube)	0.6eV
Inter-CNT Pitch	18nm
Mean free path: Intrinsic CNT	200nm
Lss (The length of doped CNT source-side extension region)	32nm
Ldd(The length of doped CNT drain-side extension region)	32nm
Work Function (CNT)	4.5eV

Table 4: Design of DXCCII using PMOS –NCNFET Configuration

PMOS –NCNFET CONFIGURATION					
PMOS Transistors		NCNFET Transistors			
Transistor Number	AspectRatio (W/L)	Transistor Number	No. of CNT	Inter CNT Pitch (nm)	Dia of CNT (nm)
M3,M7, M8	1472/ 32	M4,M5, M6,M9, M10,M11 M12,M13 M14	8	18	1.5
M15,M16 M17,M18 M19,M20 M1,M2	448/ 32				

Table 5: Design of DXCCII using NMOS –PCNFET Configuration

NMOS –PCNFET CONFIGURATION					
NMOS Transistors		PCNFET Transistors			
Transistor	Aspect Ratio (W/L)	Transistor	No. of CNT	Inter CNT Pitch (nm)	Dia of CNT (nm)
M11,M12, M13,M14	1792 / 32	M1,M2, M3,M7, M8, M15 M16 M17, M18 M19, M20	8	18	1.5
M4.M5	448/ 32				
M6,M9 M10	1472 / 32				

4. PERFORMANCE ANALYSIS OF HYBRID DESIGN

Dual-X Current Conveyor is a well known analog building block commonly used in the realization of filters, oscillators, integrators etc. Current Bandwidth, Input Port Resistance (Port X and Port Y), Output Port Resistance (Port Z) along with average power consumed are chosen as the four performance parameters for comparing the CMOS & Hybrid design configurations. For proper signal transfer ratio's to be maintained, it's of prime importance that correct values of port resistances are obtained. Port X, being an input current port must ideally exhibit zero input impedance, whereas the resistance of Port Y should reflect towards the higher side. Moreover for proper cascading of the device it is crucial, that port Z must exhibit high output impedance. HSPICE (High-performance simulation program with integrated circuit emphasis) simulator has been used to demonstrate the results at 32nm technology node and CNFET's have been modeled using Jie Deng's PTM model.

4.1 Hybrid NMOS-PCNFET Design

The configuration is obtained by substituting PMOS with PCNFET and leaving the NMOS transistors unaltered. MOSFET-like CNFET has been chosen over SB-controlled FET as the reference for carrying out the analysis. After extensive simulation, Number of CNT's have been kept at 8 In fact effect of the diameter variations on the performance parameters have been explored as shown in Figures 4-8.Simulated results indicate that bandwidth's of higher order are obtained utilizing the hybrid configuration as compared to Si CMOS. NMOS-PCNFET scores over its PMOS-NCNFET

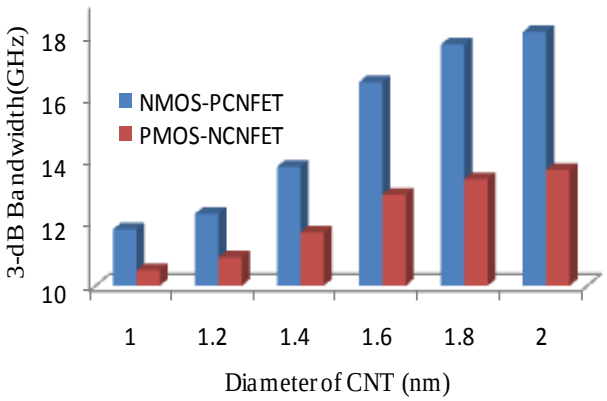

Figure 4: Variation of Bandwidth with Diameter of CNT(nm)

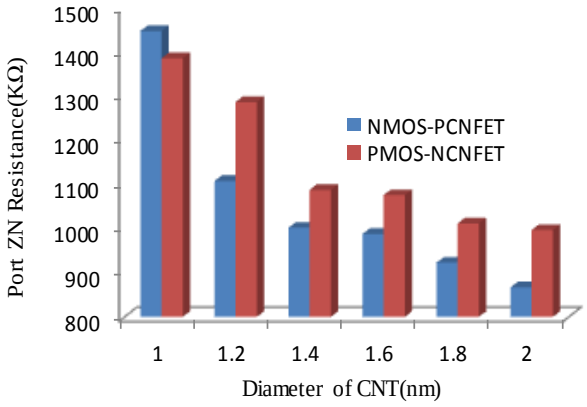

Figure 5: Variation of Output Port Resistance with Diameter of CNT (nm)

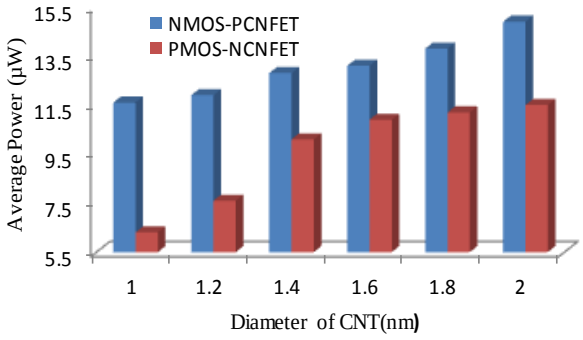

Figure 6: Variation of Average power with Diameter of CNT(nm)

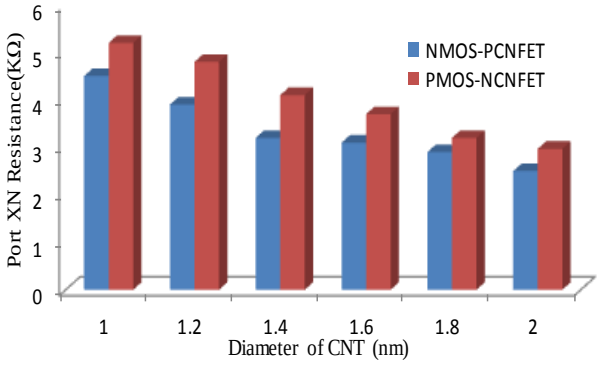

Figure 7: Variation of Resistance at Port X_N with Diameter of CNT (nm)

configuration in terms of lower input resistance and larger bandwidth's. Improvement is observed in the 3-dB bandwidth of the circuit because of the fact that NMOS transistors offers high current drive and low internal capacitances, compared to its counterpart. The key parameter variations for hybrid configurations with respect to Inter-CNT Pitch (S) are shown in Figures 9-13. On increasing Inter-CNT Pitch, the 3-dB Current Bandwidth improves slightly because of the fact that as the CNT's are brought farther the net capacitance between the gate and each CNT channel is reduced .Also with the increase in the pitch the capacitance between the inter-nanotubes decreases.

4.2 Hybrid PMOS-NCNFET Design

This configuration is obtained by using PMOS transistors as the sourcing and NCNFET transistors as the sinking device. On varying the diameter of CNT it was noticed that though the bandwidth supported by hybridized NMOS-PCNFET is much higher as compared to PMOS-NCNFET, however the average power dissipated by PMOS-NCNFET configuration is much less. Based on the simulation results for variation of CNT diameter, it's deduced that PMOS-NCNFET provides better prospect for lower power, whereas NMOS-PCNFET should be preferred for circuits operable in Ultra wide band frequency range. On performing the small signal analysis, the output resistance of Port Z is given as :

$$R_{Zn} = (r_{ds14} // r_{ds20}) \quad (4)$$

As the Inter-CNT Pitch is being increased, it is observed that the output port resistance decreases slightly, because of the

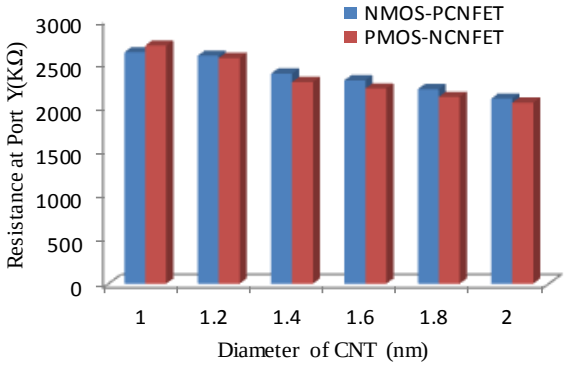

Figure 8: Variation of Resistance at Port Y with Diameter of CNT (nm)

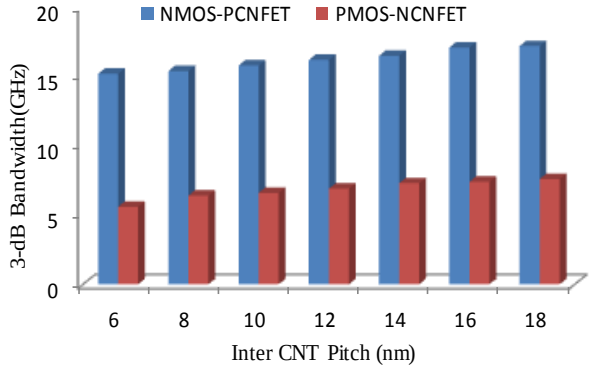

Figure 9: Variation of Bandwidth with Inter-CNT Pitch

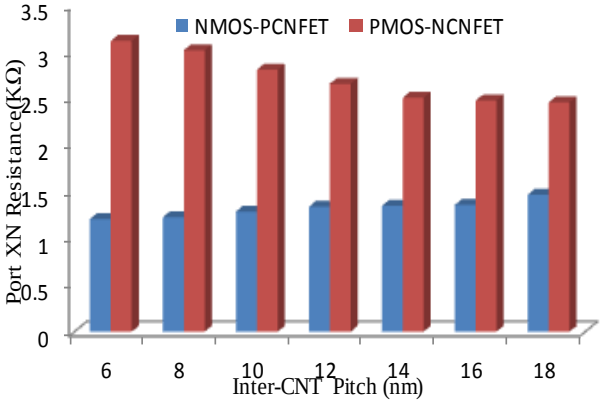

Figure 10: Variation of Resistance at Port X_N with Inter-CNT Pitch

fact that the drain-source coupling deteriorates, resulting in the reduction of resistance at port Z as depicted in Fig 11.Comparing the results of the Hybrid configuration (Figures4-13) with the standard Si CMOS, it's observed that a significant improvement is obtained in the 3-dB Bandwidth of the circuit. Furthermore, the power consumed by the Hybrid configuration is also less, when compared to the CMOS

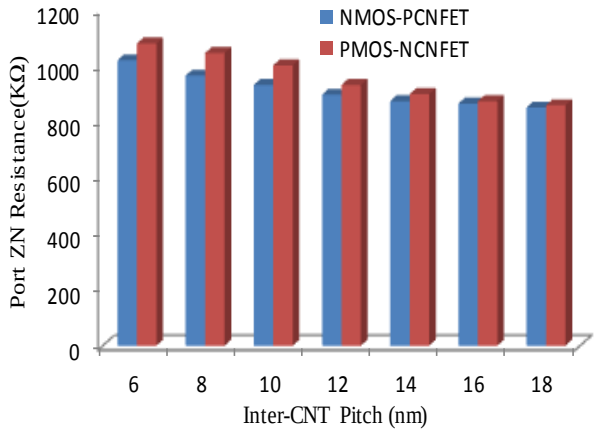

Figure 11: Variation of Output Port Resistance with Inter-CNT Pitch

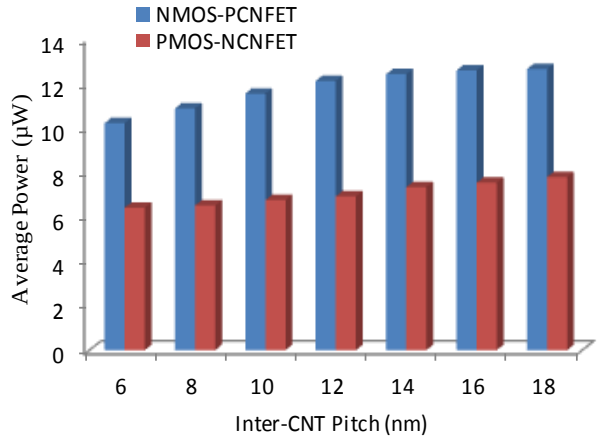

Figure 12 : Variation of Average Power with Inter-CNT Pitch

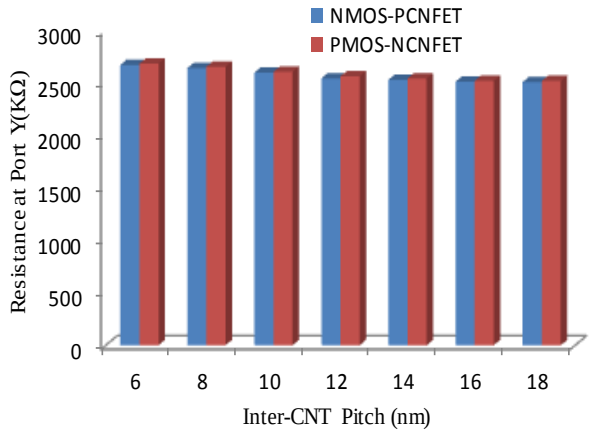

Figure 13: Variation of Resistance at Port Y with Inter-CNT Pitch

Table 6. summarizes the results of comparison between the Si CMOS and Hybrid configurations.

Parameter	*Technology*		
	Si-CMOS	*Hybrid*	
		NMOS-PCNFET	*PMOS-NCNFET*
Current Bandwidth	8.45GHz	13.8GHz	10.8GHz
Port XN Resistance	5.74 KΩ	3.35 KΩ	4.3 KΩ
Port Y Resistance	655 KΩ	2460 KΩ	2390 KΩ
Port ZN Resistance	845KΩ	1045 KΩ	1265 KΩ
Average Power	23.43µW	13.05µW	9.8µW

5. CONCLUSION

In this paper, an attempt has been made to compare the performance of a well known analog building block using CMOS and hybrid configurations. It was observed that Hybrid design outperforms the results obtained using Si CMOS, especially when considering the higher bandwidth's obtained using the former. Results showed that CNFET nano electronics can be a potential solution beyond Moore's law, however for successful integration in new micro devices ,development of robust and compatible technologies that provide controlled synthesis, positioning ,manipulation and modification of CNTs properties is still a great challenge.

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