Performance Evaluation of MISISFET- TCAD Simulation

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ABSTRACT
A novel device n-MISISFET with a 'dielectric stack' instead of the single insulator of n-MOSFET has been described and its characteristics has been obtained in this paper. The desired variation of threshold voltage is obtained with biasing for the novel n-MISISFET for various substrate doping concentrations, the effect temperature variation on various electrical characteristics is studied in the paper. The variation of electric field with substrate doping is also studied in this paper. The device is based on the principle of resonant tunneling diode (RTD).

Keywords
n-MISISFET, n-MOSFET, RTD.

1. INTRODUCTION
In the scaling scenario, the gate oxide thickness has been reduced drastically. The gate dielectric is a mere 1.2 nm in implementation of the 65nm node. The ultra thin dimensions give rise to a large number of problems. Reduction of gate oxide thickness results in an increase of field across the oxide which leads to tunneling current. Nevertheless, making the dielectric ever thinner is necessary in order to meet increasing performance goals of high drive currents and minimized short channel effects [1]-[3]. The leakage current contributes to excessive standby power consumption. As a result the magnitude of power per unit area has been growing. The entire semiconductor industry is struggling with the exponentially increasing heat of chips due to high functional and transistor density.

To extend the scenario of transistor scaling and Moore's Law, a lot of research has been done in the recent past. The research can be categorized as - research on alternative gate dielectrics like hafnium dioxide (HfO_2), zirconium dioxide (ZrO_2) and titanium dioxide (TiO_2) and alternative device geometries like Double Gate MOSFET (DGMOSFET), tri-gate, gate all around) structures, silicon nanowire transistors (SNWT) etc. Effective gate control can be achieved by the multigate structures [4]-[6]. Another effective device structure was proposed in [8]-[9] which involves replacing the gate oxide of the MOSFET with a RTD (resonant tunneling diode) based structure. In this structure instead of single insulator, two insulators and a semiconductor layer sandwiched in between thus it is named as MISISFET (metal insulator semiconductor insulator semiconductor FET). In this paper the I_d-V_g (transfer) characteristics and I_d-V_d (output) characteristics of the n-MISISFET structure are studied. The variation of threshold voltage with substrate doping with body biasing of the n-MISISFET device is done in the paper, the effect temperature variation on various electrical characteristics is studied in the paper. The variation of electric field with substrate doping is also studied in this paper. The device is utilising the principle of operation of RTD to reduce the direct tunneling leakage current of the transistor.

2. DEVICE DESCRIPTION
As explained above the device is like an ordinary n-MOSFET but the oxide structure of the n-MOSFET is replaced with the RTD (resonant tunneling diode) structure for n-MISISFET. The 'dielectric stack' of n-MISISFET has three layers, Insulator-Semiconductor-Insulator (Fig 1). The sandwiched semiconductor layer is made thinner than the insulators. Thus, the semiconductor layer forms a quantum well (SQW) within the walls of the insulator. The band diagram of n-MISISFET's 'dielectric stack' is shown in Fig 2.

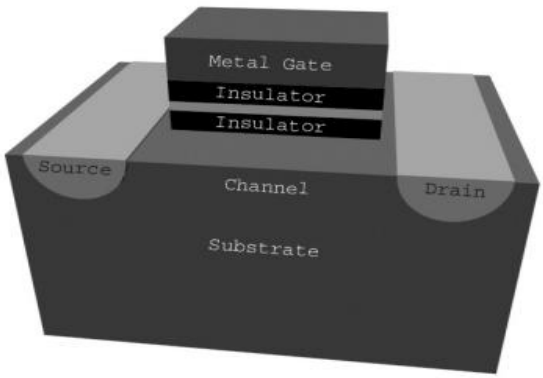

Fig 1: Schematic structure of MISISFET

2.1 Principle
This device utilises the principle of operation of RTD to reduce the direct tunneling leakage current of the transistor. The energy levels of the thin SQW are quite spread out i.e. they are far away from each other. It can be assumed for simplicity that there are only two energy levels in our region of concern. Direct tunneling (DT) electron transport can occur only through the energy levels of SQW. Hence the DT component of current can be reduced if

the energy levels of SQW are situated where the value of the distribution function in the channel is low [8]-[9].

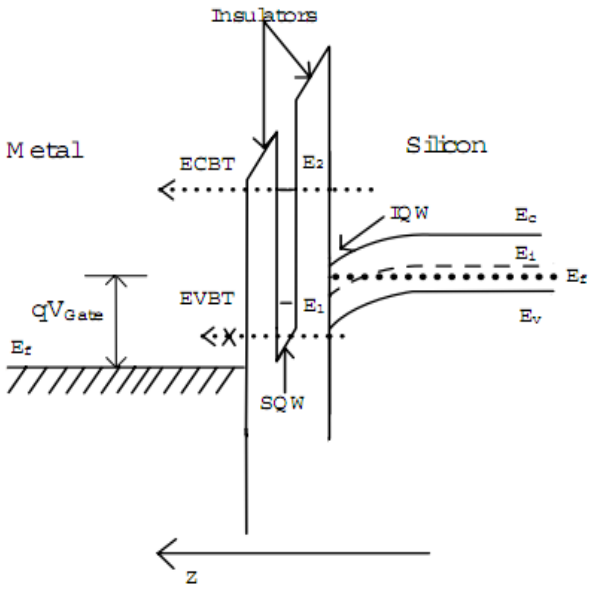

Fig 2: Band diagram of MISIS showing all the possibilities of various types of direct tunneling

In very thin oxide layers (less than 3 to 4 nm) direct tunneling current dominates, which is given by the following equation for MOSFET [10].

$$J_{DT} = AE^2{}_{ox} \exp\{-\frac{B\left[1-\left(1-\frac{V_{ox}}{\varphi_{ox}}\right)^{\frac{3}{2}}\right]}{E_{ox}}\} \quad (1)$$

where $A = \frac{q^3}{16\pi^2 h\varphi_{ox}}$ and $B = \frac{4\sqrt{2m^*}\varphi^{3/2}{}_{ox}}{3hq}$

2.1.1 To study the characteristics of nMISISFET

The basic structure of the n-channel MISISFET (n-MISISFET) transistor built on a p-type substrate is shown in Fig. 3. The MISISFET consists of a resonant tunneling diode structure instead of gate oxide with two p-n junctions placed immediately adjacent to the *channel* region that is controlled by the gate. The carriers i.e. electrons in the n-MISISFET transistor, enter through the source contact (S), leave through the drain (D) and are subject to the control of the gate (G) voltage. For $V_{GS} < V_{T0}$ the region between the source and drain is depleted and thus no carrier flow is observed in the channel. As the gate voltage is increased beyond the threshold voltage the inversion layer is established and once the inversion layer is established on the surface, an n-type conducting channel forms between the source and drain, which is capable of carrying the drain current [11].

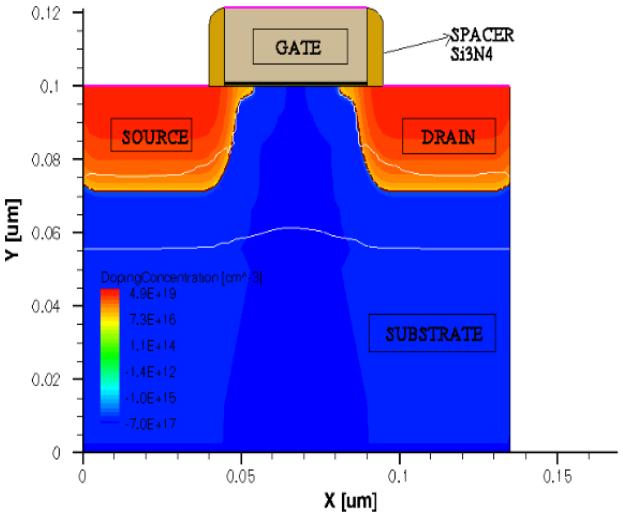

Fig 3: Structure of n-MISISFET

For n-MISISFET if a small drain voltage $V_{DS} > 0$ is applied a drain current proportional to V_{DS} will flow from the source to drain through the conducting channel. The channel forms a continuous current path from the source to the drain. This operation mode is called the *linear mode*, or the *linear region.* The I_d-V_g characteristics for n-MISISFET for linear mode of operation are shown in the Fig 4a.

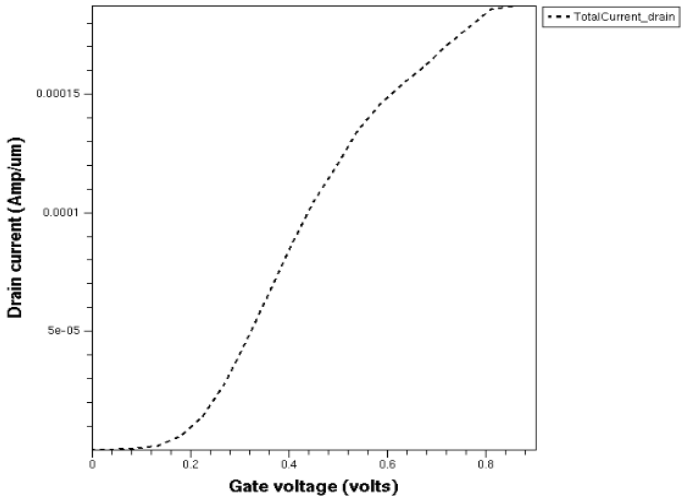

Fig 4a: I_d-V_g characteristics of n-MISISFET

For n-MISISFET as the drain voltage is increased, the inversion layer charge and the channel depth at the drain end start to decrease. Eventually, for $V_{DS} > V_{DSAT}$, a depleted surface region forms adjacent to the drain, and this depletion region grows toward the source with increasing drain voltages. This operation mode of the n-MISISFET is called the *saturation mode* or the *saturation region.* The I_d-V_d characteristics of n-MISISFET are shown in the Fig 4b [11].

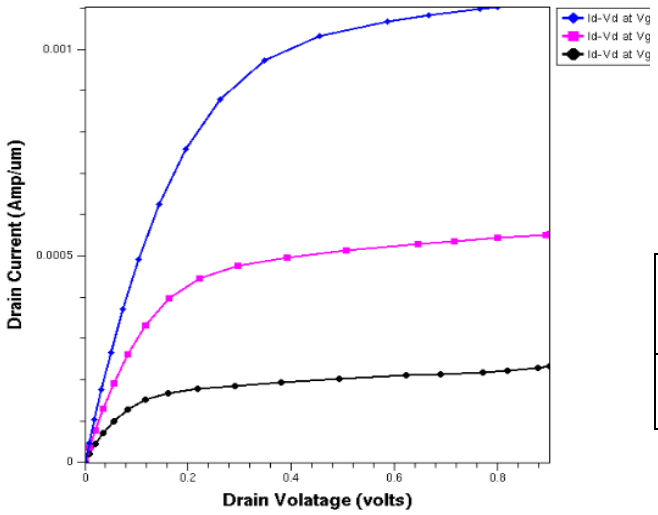

Fig 4b: I_d-V_d characteristics of n-MISISFET

2.1.2 Threshold voltage variation with substrate doping for reverse and forward body bias

For a MOSFET if the substrate (body) is biased at a different voltage level than the source which is at ground potential (reference), then the depletion region charge density can be expressed as a function of the source-to-substrate voltage V_{SB} [11].

$$Q_B = -\sqrt{2q.N_A.\varepsilon_{Si}.|-2\varphi_F + V_{SB}|} \quad (2)$$

In n-MOSFET for a nonzero substrate bias the generalised expression of threshold voltage is

$$V_T = \phi_{GC} - 2\varphi_F - \frac{Q_B}{C_{OX}} - \frac{Q_{OX}}{C_{OX}} \quad (3)$$

Where ϕ_{GC} is the work function difference of the metal gate and channel, φ_F is the Fermi potential of the substrate, Q_{ox} is the voltage component required to offset the fixed charges in the gate oxide and silicon-oxide interface, Q_B is the depletion charge density and c_{OX} is the oxide charge capacitance.

The most general expression of the threshold voltage V_T for n-MOSFET is given as

$$V_T = V_{T0} + \gamma.(\sqrt{|-2\varphi_F + V_{SB}|} - \sqrt{|2\varphi_F|}) \quad (4)$$

Where the parameter $\gamma = \frac{\sqrt{2q.N_A.\varepsilon_{Si}}}{C_{ox}}$ is the substrate-bias (or body effect) coefficient [11].

For n-MISISFET the analysis is done to study its behaviour of variation of threshold voltage V_T when substrate doping is changed and keeping the body bias constant. First of all we have analysed the variation in threshold voltage with reverse body biasing of -0.3V and increasing the substrate doping levels. In general for n-MOSFET whenever we increase the levels of substrate doping the threshold voltage will increase at a particular body biasing voltage.

Table.1 Variation of Threshold voltage with substrate doping

Substrate Doping ($x10^{17}$ cm^{-3})	5	7	8	20	40
Threshold Voltage (V)	0.178	0.196	0.207	0.285	0.403

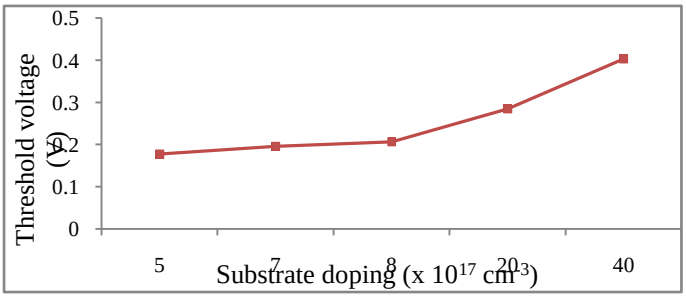

Fig 5: Variation of threshold voltage with substrate doping at a reverese body bias voltage -0.3V.

From the above shown table and graph it is clear that threshold voltage is increasing with increase in substrate doping concentration at a reverse body biasing of -0.3V. The same results would be analysed for forward body biasing 0.3V. Here we will again vary the substrate doping concentration and see its effects on the threshold voltage.

Table.1 Variation of Threshold voltage with substrate doping

Substrate Doping (x 10^{17} cm^{-3})	5	7	8	20	40
Threshold Voltage (volts)	0.162	0.185	0.201	0.255	0.385

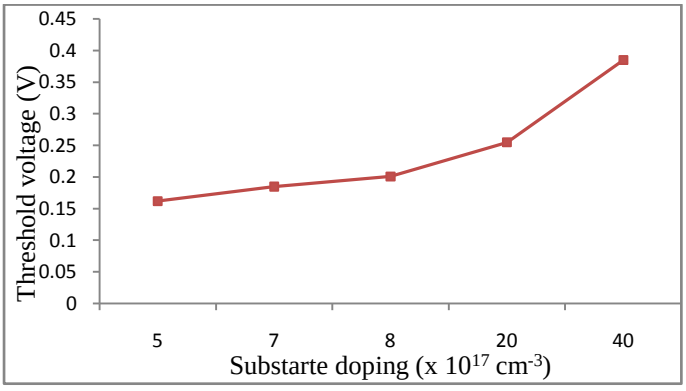

Fig 6: Variation of threshold voltage with substrate doping at a forward body bias voltage of 0.3V.

Thus from the graph it is clear that thresold voltage will increase as we increase the value of substrate doping concentration. Hence for a particular body biasing and at different substrate doping concentration the threshold voltage of n-MISISFET can be varied.

3. Effect of Temperature variation on Electrical charcteristics of MISISFET

The effect of temperature variation on various electrical characteristics of MISISFET are studied in this section of the paper. The temperature is varied from 300K to 345K. The effect of temperature variation is seen on threshold voltage, DIBL, and Subthreshold slope.

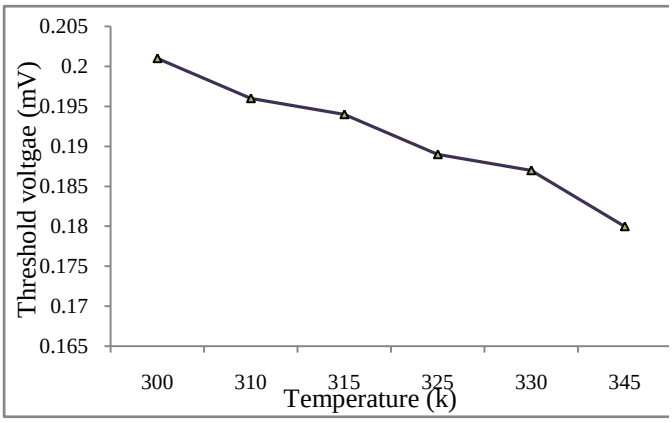

Fig 7: Variation of threshold voltage with temperature

From the above shown figure we can see the threshold voltage is decreasing with increase in temperature for MISISFET. Increase in temperature increases the fermi potential and thus leads to decrease in threshold voltage.

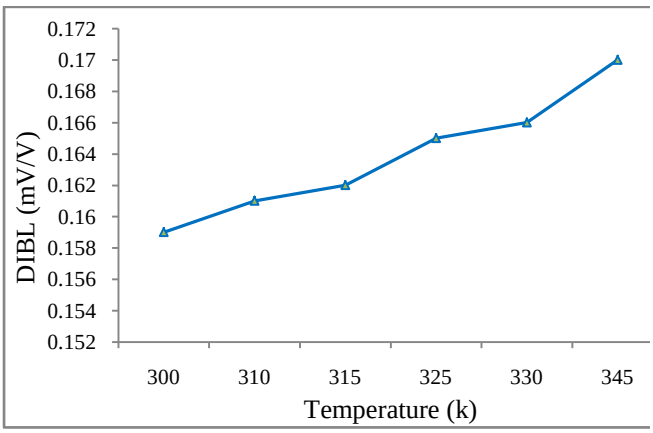

Fig 8: Variation on DIBL with temperature

DIBL (drain induced barrier lowering) increases with increase in temperatrure as the electrons gains enough kinetic energy with increase in temperature and thus they can easily cross the barrier and leads to increase in DIBL for MISISFET.

Subthreshold slope indicates how effectively the drain currents swithches to zero with reduction in gate voltage, its value increases with increase in temperature for MISISFET.

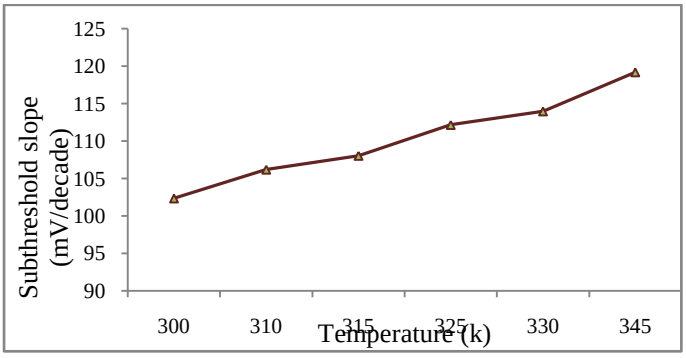

Fig 9: Variation of Subthreshold Slope with Temperature

4. Effect of Variation of Electric Field on MISISFET

Two different electric field distribution exist in MISISFET structure Transverse field and Lateral field. The Transverse field is caused by the potential difference between the conductive gate and substrate. The field supports the substrate depletion region and inversion layer. The lateral field arises due to non zero source drain potential and is the main mechanism for current flow in MISISFET. The effect of electric field variation at different substrate doping concentration is studied.

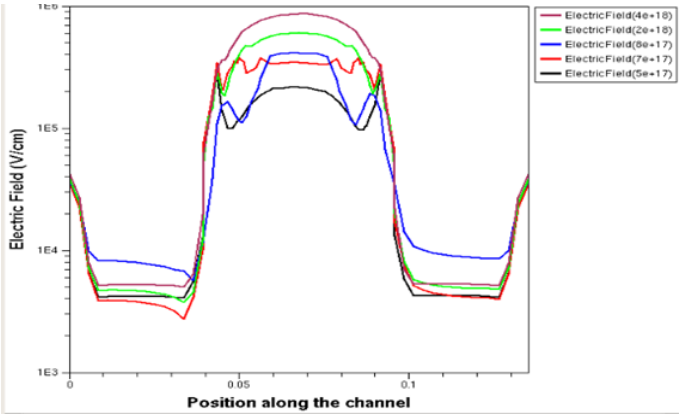

Fig 10: Electric field variation with substrate doping

From the above figure we can see that the electric field variation with the postion along the channel is more for higher value of substrate doping for MISISFET.

5. CONCLUSION

The I_d-V_g characteristics and I_d-V_d characteristics of n-MISISFET has been studied in the paper in the linear and saturation mode of operation. The n-MISISFET device shows result similar to that of n-MOSFET for variation of threshold voltage with increasing substrate doping concentration at a particular body biasing voltage, and variation of temperature and its effect on electrical characteristics. The electric field variation

is also studied with substrate doping concentration. The device will show good results for gate leakage current reduction as here the tunneling will occur whenever the quantised energy level is available is to electron.

6. REFERENCES

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