High Performance Precision Rectifier for Analog Signal Processing

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ABSTRACT

This paper presents two improved precision rectifiers, each employing two active elements and two MOS transistors. The new circuits are advantageous when compared to the most recent work [5] by enjoying high input impedance and resistor-less realization, which makes them ideal for CMOS implementation. High precision and wide frequency operation of the circuits is shown along with parasitic insensitivity. The dual-X current conveyor based novel circuits have useful analog signal processing applications and are verified through extensive computer simulations.

General Terms

Analog Signal Processing, Current Conveyors.

Keywords

Precision Rectification, Dual-X Current Conveyor.

1. INTRODUCTION

Analog signal processing has become an important area of continuous study owing to the inevitable need of high performance analog interfaces and processing circuits to support the ever-increasing digital demands [1]. As a result, the use of current conveyors has increased so as to fulfill the challenging requirements of high performance analog circuits [2]. Precision rectifier is one such application which has been extensively studied in open literature. Use of various types of current conveyors has ensured novel circuits which are ideal to cater to the present requirement [3, 4]. The most recent precision rectifier further highlights the preceding statement [5]. However, the most recent work is found lacking with respect to the input impedance. It may be emphasized that voltage-mode circuits with high input impedance are desirable to avoid the loading of the signal source [6, 7]. The recent work does not exhibit this feature [5]. Additionally, the most recent work employs a number of floating resistors which are not ideally suited for monolithic implementation. This leaves further scope for alternatives with high input impedance and fewer (or in the best case, no) resistors. This paper is an attempt to cater to these needs by offering two novel precision rectifiers with the same active element count (two) as in the recent work [5] but additional advantages as already mentioned above. The active element used is the Dual-X Current Conveyor (DXCCII) which continues to find most recent attention in technical literature [8 - 11]. Computer simulation results are given to validate the proposed theory.

The remainder of this paper is arranged as follows. Section-2contains details of two new precision rectifier circuits based on DXCCII. Section-3 contains the non-ideal study of the proposed circuits. Section-4 contains PSPICE simulation results of the proposed circuits for various signal waveforms. Concluding remarks are presented in Section-5.

2. PROPOSED CIRCUIT

The Dual-X Current Conveyor (DXCCII) is a versatile building block for analog signal processing applications. It is conceptually a combination of the regular CCII and the inverting current conveyor (ICCII).It has two X terminals, namely X_P (non-inverting X terminal) and X_N (inverting X terminal). The X_P and X_N terminal currents are reflected to the respective Z terminals, namely Z_P and Z_N . Fig. 1 shows the symbolic diagram of a typical DXCCII whose port relations are given in (1). A CMOS realization of the DXCCII is shown in Fig. 2 [9].



Fig 1: Symbolic representation of DXCCII

$$\begin{bmatrix} I_Y \\ V_{XP} \\ V_{XN} \\ I_{ZP} \\ I_{ZN} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_Y \\ I_{XP} \\ I_{XN} \end{bmatrix}$$
(1)

The two new precision rectifier circuits using DXCCII are presented in Fig. 3 and Fig. 5 from where it is readily evident that both the rectifier circuits employ the same active element count (two) as in a recent work [5], but with additional advantages of high input impedance and the avoidance of the use of floating resistors. The operation of the proposed rectifier circuit of Fig. 3 can be understood as follows. The DXCCII-2 acts as a high gain saturated amplifier (comparator) which converts the input sinusoidal waveform to a square wave with a maximum value of V_{DD}, as shown in Fig. 4. Forthe positive half of the input cycle, the positive half of the square wave turns $M_N on$ and $V_{out} = V_{in}$. During the negative half of the cycle, the output voltage at Z_P of DXCCII-2 is saturated at the negative biasing supply (V_{SS}) thereby turning M_{Pon} and ensuring $V_{out} = -V_{in}$. As a result, full-wave rectification is achieved.



Fig 2: CMOS realization of DXCCII



Fig 3: Proposed precision rectifier circuit - I



Fig 4: Control voltage (V_C) as obtained in the proposed precision rectifier circuit – I

The discrete load resistance R_L in Fig. 3 can be removed by utilizing the high output resistance available at the currentoutput terminals (Z_P and Z_N) of the DXCCII. Such a resistorless realization of the precision rectifier is presented in Fig. 5.



Fig 5: Proposed precision rectifier circuit - II

3. NON-IDEAL STUDY

In the case of an ideal DXCCII, it was considered that the voltage transfer gains, from Y to X_{P} and X_{N} terminals, are unity in magnitude, as given in (1). However, a real implementation of the DXCCII exhibits non-idealities in the voltage transfer gains and therefore the DXCCII port relationships are modified as given below.

$$V_{XP,n} = \beta_P V_Y; \quad V_{XN,n} = \beta_N V_Y \quad (2)$$

The effect of parasitics associated with the DXCCII is further considered. The parasitic resistances appearing at the XP and XN terminals are denoted by RXPand RXNrespectively. The equivalent circuit including the parasitic resistances and the resistance associated with the MOSFETs MN and MP, for the positive half cycle of the input, as obtained from Fig. 3, is shown in Fig. 6.



Fig 6: Equivalent circuit showing the parasitics during the positive half cycle

Taking the above non-ideal transfer gains and parasitics into account, the output voltage during the positive half cycle of the input waveform in Fig. 3 is found to be

$$\frac{V_{out}}{V_{in}}\Big|_{n} = \frac{\beta_{P} + \beta_{N} \left(\frac{R_{XP} + R_{on,MN}}{R_{XN} + R_{off,MP}}\right)}{1 + \frac{R_{XP} + R_{on,MN}}{R_{L}} + \frac{R_{XP} + R_{on,MN}}{R_{XN} + R_{off,MP}}} (3)$$

From (3), it is evident that since

$$R_{XN} + R_{off,MP} \gg R_{XP} + R_{on,MN}$$

the transfer function in the presence of non-ideal and parasitic effects can be approximated as

$$\frac{V_{out}}{V_{in}}\Big|_{n} \simeq \frac{\beta_{P}R_{L}}{R_{L} + R_{XP} + R_{on,MN}} (4)$$

Similarly, during the negative half cycle of the input, the nonideal transfer gain becomes

$$\frac{V_{out}}{V_{in}}\Big|_{n} \simeq \frac{\beta_{N}R_{L}}{R_{L} + R_{XP} + R_{on,MN}} (5)$$

From (4) and (5), it is evident that the output voltage deviates from its ideal value in the presence of device non-idealities and parasitics, and the amplitude of the obtained output voltage is slightly less than the ideally expected value.

Similar expressions can be readily obtained for the second proposed precision rectifier circuit, of Fig. 5, by replacing R_L with ($R_{ZP} \parallel R_{ZN}$).

4. SIMULATION RESULTS

To verify the proposed theory, the precision rectifiers of Fig. 3 and Fig. 5were designed and simulated using PSPICE. All simulations werecarried out using 0.35 μ mTSMC CMOS process parameters available through MOSIS and the supply voltages were kept at ± 1.25 V.

The internal circuit implementation in CMOS technology wastaken from [9]. The NMOS and PMOS switches are implemented with *W/L* ratios of1 μ m/0.35 μ m and 2.4 μ m/0.35 μ m respectively and the value of the load resistance R_L was kept as 10 K Ω . It may be mentioned that DXCCII–1 in Fig. 3 does not use the Z_P and Z_N terminals and therefore, the transistors corresponding to these current-output stages need not be implemented during the actual integration of the circuit, thereby saving chip area. The same is true for the transistors employed in the X_N and Z_N stages of DXCCII–2, the actual realization of which is not needed. The resulting DC transfer characteristics of the proposed precision rectifier of Fig. 3are shown in Fig. 7.

The rectification performance for the circuit of Fig. 3 was verified by applyingfour different sinusoidal inputs of 50mV peaks at 500 KHz, 750 KHz, 1 MHz and 1.25 MHz, the results of which are depicted in Fig.8 through Fig. 11 from where the expected operation of the proposed precision rectifier is ascertained.



Fig 7: DC transfer characteristics of the proposed precision rectifier circuit – I



Fig 8: Input and output waveforms at 500 KHz of the precision rectifier – I



Fig 9: Input and output waveforms at 750 KHz of the precision rectifier – I



Fig 10: Input and output waveforms at 1 MHz of the precision rectifier – I



Fig 11: Input and output waveforms at 1.25 MHz of the precision rectifier – I



Fig 12: Input and output waveforms at 1 MHz of the precision rectifier – II

A similar performance evaluation using computer simulations was also carried out for the circuit in Fig. 5. The input and output signal waveforms at 1MHz are presented in Fig. 12. The distortions visible in the output, corresponding to the zero crossing points in the input waveform, are mainly due to the switching limitations of the transistors M_P and M_N , and the transistors comprising the Z+ output stage of the DXCCII-2. These may be reduced by employing high frequency transistors.

5. CONCLUSION

This study enriches the existing knowledge on current conveyor based precision rectifiers by presenting two new circuits, each based on two active elements and two MOS transistors, which outperforms the most recent work [5, and the references cited therein]. The new circuits benefit by exhibiting high input impedance, resistor-less realization, and simpler& parasitic insensitive topology, making them ideal for integration in CMOS technology. The new circuits exhibit good precision and high frequency operation. Non-ideal study is also given along with attractive computer simulation results. Incorporation of a buffer at the output is an area under investigation for future communication.

6. REFERENCES

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