Survey on High Performance Multiprocessor System on Chips

T.Naga Swathi
Assistant Professor
School Of Computing Science & Engineering
VIT University,Vellore-632014

M.K.Jayanthi
Associate Professor
School Of Computing Science & Engineering
VIT University,Vellore-632014

ABSTRACT
This paper surveys the High Performance Computing Architectures. Embedded Systems Requires the combination of Different Hardware's selected based on application. MPSOC can be designed based on two categories whether it's a homogeneous or heterogeneous Processors. Design Complexity involves in Power Consumption. The high Performance Embedded systems are required in Wireless Networks, Networking, Multimedia, Mobile Phones These applications demand real time processing and high throughput. MPSOC consists of Application Specific Processors, DSP's, General Purpose Processors Hardwired Accelerators, Mixed signal circuits which forms a Heterogeneous Processor. In this paper comparison of different architectures is been explained in a detailed form and the hardware challenges involved in designing MPSoCs

General Terms
MultiProcessor system on chip,Heterogeneous Processors

Keywords
MPSOC, VLSI, DSP

1. INTRODUCTION
W Multiprocessor System on chip is mainly introduced for obtaining high performance in Embedded Systems Complex Hardware is designed which contains more than one processor which is used in both analog and Digital Applications on the same Integrated circuit .In real world the multiprocessor systems gives high efficiency and speed for processing .MPSoCs design requires knowledge of VLSI Design Flow which involves Behavioral ,functional, physical, design library, Methodology and Technology implementation of Application Specific circuit.

2. MPSOC ARCHITECTURE
Multiprocessor System on chip gives higher Performance than Multicore-systems. It is an important unique concept which is mainly used in distributed embedded system where it is going to process from various locations gives a single output with high Performance. Now a day's embedded systems can be used in many applications. Heterogeneous computing is obtained by designing high performance Architectures. Before designing the MPSOC we need to consider the design based on Cost limitations in large markets comparison of products takes place between different companies. designing the same features .The systems integrity, such as reliability and safety working within the confines of available elemental functionality processing power, memory, battery life marketability and salability are deterministic requirements. The application specially requires image processing and computer vision use parallelism. Earlier MPSOC was not used Embedded consists of single processor and necessary hardware is built. .The main use of MPSOC is it offers great amount of parallelism. While in a single chip SoC with hardware accelerators, the single processor is expected to coordinate the various accelerators, in a

3. Hardware Architecture
The hardware components of the MPSoCs depend up on the applications .In this research paper the main constraint is to develop a circuit which consists of more than one processor at the same time. The increasing number of processors will increase the Performance of a system used in High Performance Embedded Computing devices .The Application specific circuits are required for a high end computing .The communication circuits ,interfacing circuits with a reuse IP need s to be developed.

3.1 Software Constraints
There are so many constraints involved for the software programmers for developing a product .the memory will be a key factor for developing an embedded product since the limited memory and low power systems needs to be improved .In all the mobile application the software will be developed by the Java mobile applications in order to improve the performance of a system.

3.2 Mpsoc Performance
MPSOC performance depend up on the number of processors it can be more than two and execution time will be increased so the need of synchronizing of the process is required .Interprocessor Communication is using the shared memory concept needs to be developed in order to improve the performance of the MPSOC.

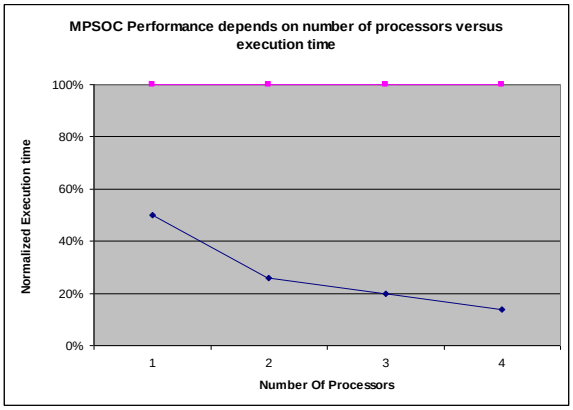

Fig 1: Mpsoc Performance depends on the number of processors versus execution time

2.4 Intel Ixp2800 Network Processor

It delivers programmable high-performance processing power with flexibility to address a wide variety of LAN, WAN, and Telecommunications applications .This network processor is a second-generation, highly integrated, hybrid data processor that provides high-performance parallel processing power It combines the state-of-the-art Intel XScale core microprocessor with 16 independent 32-bit RISC data engines with hardware multi-thread support that, when combined, provide a total of 25.2 giga operations per second. . The Intel IXP2800 network processor is the highest performance member of Intel's second-generation network processor family. It combines 16 fully programmable Multi-threaded micro engines for packet forwarding and traffic management with an Intel XScale core on a single chip. offers a possible customization opportunity wherein the datapath is itself designed keeping the above fact in mind. This decreases the word size of the ALU,and flexibility to a wide variety of OC-192 networking, communications, and data-intensive applications. It is designed specifically as a data control element for applications that require access to a fast memory
subsystem, a fast interface to I/O devices such as network MAC devices, and processing power to perform efficient manipulation on bits, bytes, words, and double-word data. It combines the state-of-the-art Intel XScale core microprocessor with 16 independent 32-bit RISC data engines with hardware multi-thread support that, when combined, provide a total of 25.2 giga operations per second. The Intel IXP2800 network processor is the highest performance member of Intel's second-generation network processor family. It combines 16 fully programmable Multi-threaded micro engines for packet forwarding and traffic management with an Intel XScale core on a single chip.

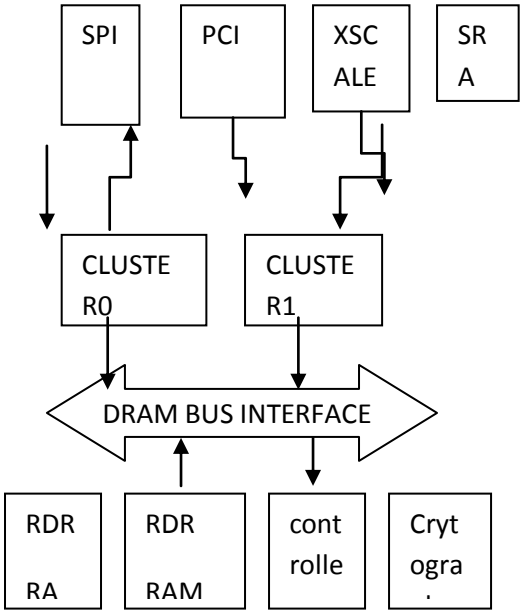

Fig. 2: Block Diagram Of IXP2800

3. NI OMAP 4460

Building upon the strengths of the OMAP4460 processor, the OMAP4470 is the first processor designed for mobile computing, with enhanced graphic and memory performance to support intense computing applications and operating systems. Its used for powering high-end smart phones to the rapidly growing tablet and ultra thin laptop market. that support symmetric multiprocessing (SMP) and deliver speeds up to 1.8 GHz each. These complemented by two ARM Cortex-M3 cores that can offload real-time processing functions, lowering overall power consumption. Other key architectural features include an Image Signal Processor (ISP) and IVA 3 accelerator offering unparalleled imaging and video performance and supporting multiple video encode/decode standards, and a programmable DSP. The processor architecture has been enhanced to deliver top-notch graphics by increasing its predecessor processor specifications in a balanced manner. In addition to the latest-generation 3D graphics core –Imagination Technologies' POWERVR SGX544, the OMAP4470 system-on-chip (SoC) includes a dedicated 2D

composition engine. This composition engine is able to accelerate rich UI composition with multilayer blending with transparency on high resolution displays to allow
Highly-optimized mobile applications platform including: applications processors, multimedia software and power management IVA 3 accelerator enables full HD 1080p,multistandard video encode/decode• Integrated Image Signal Processor for faster, higher-quality image and video capture with digital SLR-like 20-megapixel imaging SMP for higher mobile computing performance and PC-like, uncompromising web browsing experience Support for leading mobile operating systems including Microsoft Windowsand Linux (Android, Chrome) ,Software and pin-to-pin compatibility with other OMAP 4 family processors , Programmability and performance

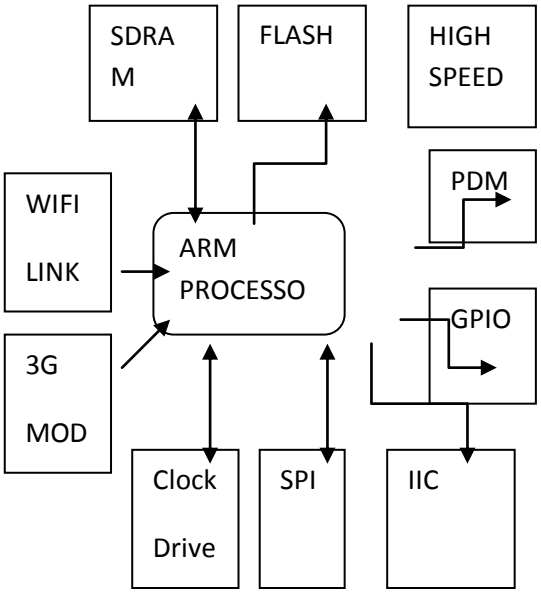

Fig 3: Omap 4460

4. NEXPERIATM PNX8550

MIPS based embedded microcontroller architecture. The Philips NexperiaTM PNX8550 is a highly integrated media processor for building mid- to high-end analogue/digital and digital TV receivers with advanced TV and connectivity features. Developed in co-operation with Philips Semiconductors, the toolset offers a comprehensive solution for NexperiaTM PNX8550 application development by both Independent Software Vendors (ISVs) and TV manufacturers. ISVs have a requirement to provide TV manufacturers with software that allows them to implement features, such as MHEG, without having to do the core development themselves. The Ashling tools allow those ISVs to closely integrate their code via the Nexperia Home API with the capabilities of the silicon For developers at TV manufacturers, whether exclusively integrating their own applications or that from ISVs, the Ashling tools enable that code to be integrated into the operating system with minimal effort. Ashling provides a full range of emulation, compilation, debug tools to support the Ne Ashling's powerful real-time debug technology, the Ashling tools design team will ensure that users of Philips NexperiaTM PNX8550 microcontrollers can benefit from a powerful and flexible development and debug toolset from the outset. The toolset includes: Path Finder Source-level Debugger xperia TM PNX8550. By applying

STNomadik - Open multimedia platform for next generation mobile devices Most application processors are single ARM CPUs or DSP+ARM combo architectures. These monolithic and split architectures can only do so
much without increasing clock frequencies and data movement between the processor(s) and memory. So designers augment them with acceleration hardware to create video-adapted versions. The NomadiK platform has instead a distributed-processing architecture with programmable smart accelerators engineered for real-time application processing. These smart accelerators
operate independently and concurrently as needed to ensure the lowest absolute system power and deterministic performance .

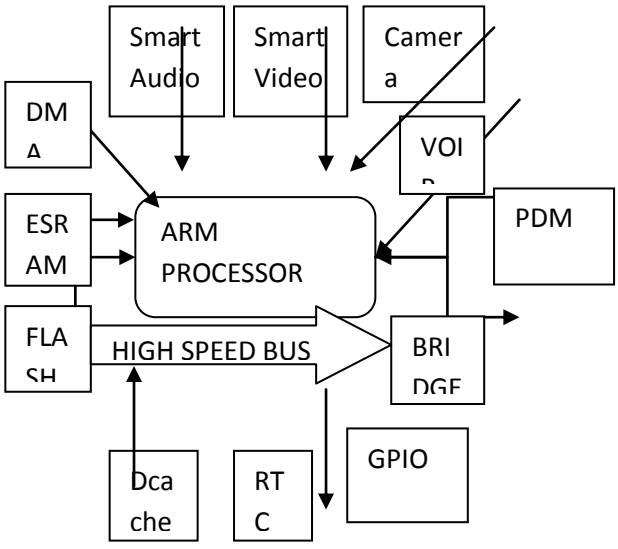

Fig 4: STNomadik Architecture

5. SOFTWARE CHALLENGES

Embedded Software Development Tools requires System designs and manufactures In-Circuit Emulators, JTAG/BDM Emulators, Smart Card development tools, Source Debuggers, Integrated Development Environments, Development Boards and Software Quality Assurance tools.. The hardware designer should design based on the Software challenges keep it in mind .Because the software code should be written in the ROM after fabrication of the Multiprocessor System based on the application to know what can be thrown out from the hardware and what must be left in. The architects must also understand the characteristics of the application software that affect real-time and low-power operation. Software plays a critical role in MPSoC design because the chip won't do anything without software. But the fullest view of software challenges relating to MPSoCs starts with the design environment and then moves to the chip itself. With an advanced set of features, including dedicated 2D and 3D graphics, display and imaging subsystems, high security and a programmable DSP, the processors should have feature-rich, high-performance mobile computing devices that offer compelling displays, rich UIs, and applications for both the consumer and enterprise markets. TI provides a comprehensive software suite that supports the leading mobile OSes, including Microsoft Windows and Linux (Android, Chrome), and is integrated and tested up to the application level, enabling faster and easier development for end equipment manufacturers and application developers. Additionally, the software platform has been performance and power optimized for the OMAP 4 platforms to ensure the highest performance in customers' products. The software suite allows OEMs and partners to spend their resources on differentiating their product at the user interface and
Application level while reusing most of the system platform software components directly from TI. Code compatibility among processors makes it easy to port software and a sophisticated development environment speeds

5.1 Development Environments And Tools

Development environments are necessary to allow programmers to create code for the system, starting well before the chip is fabricated. We normally think of the host software when we talk about a development environment, but in fact the development environment includes the target hardware as well. If the development environment requires a complete chip to operate, then software development will be intolerably delayed. Software and hardware designers must work together to develop methodologies that allow them to develop as much software as possible without a working MPSoC's. At least part of the solution is a software architecture that partitions functions such that a great deal of software can be implemented on a subset of the architecture's processors, using a configuration that can be supplied by existing software and development environment configurations.. A great deal of the software effort is to port the reference implementation of the standard to the platform. Because reference implementations are usually written with functionality, not performance in mind, porting the code requires the use of software analysis tools .A great deal of the performance analysis for MPSoC's designs is done using execution traces. A trace is gathered from an Existing system, or perhaps synthesized, and then used to drive a simulation. The simulation is monitored to evaluate

5.2 Operating Systems and Middleware

The Multi Processor includes the latest-generation graphics core from Imagination Technologies, the POWERVR SGX544. SGX544 offers more than two times the performance of the previous SGX540 core.This core provides full support for DirectX with maximum hardware acceleration, channel architecture, even when running at the same speed. Enhanced 2D and 3D cores allows it to offer up to two times the performance of many real-time operating systems .consumers get extreme multi-tasking ability and download times. The dual-channel architecture enables 100 percent higher bandwidth than the conventional single-channel architecture allows. It maintains a higher number of instructions actually executed by processor cores as usage gets more complex and consumers run more intensive applications or multiple screens compared to single screens.

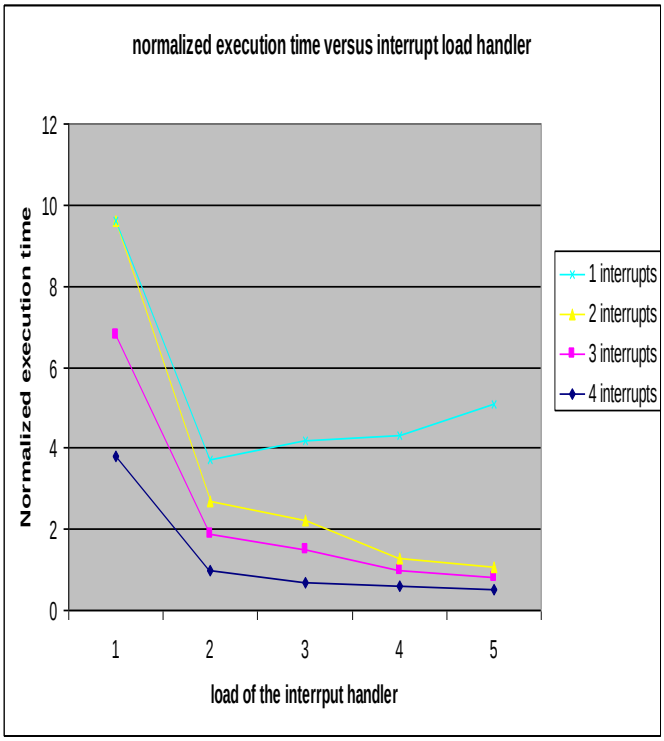

Fig. 5: Normalized Execution Time Versus Interrupt Load Handler

5.3 Multi Processor Security

Mobile security technology is a hardware and software solution that enables robust protection of premium copyrighted digital media content, secure protocol applications and e-commerce applications such as ticketing, banking, brokering and shopping. M-Shield is based on open APIs and provides an

environment for secure applications that deliver robust performance, interoperability, greater development speed and large economies of scale. However, as MPSoCs start to include Internet connections, they will become vulnerable to a variety of security attacks. When MPSoCs are used in safety-critical applications, such as cars and airplanes, those security problems must be a central concern of the system architects .

in non-safety-critical systems, such as home Entertainment systems, poor security on the MPSoC's can make the chip unusable in practical systems. However, MPSoCs that are used in real-time systems must secure the continuous operation of that real-time Control function. Attackers may try to disrupt the MPSoC's real-time characteristics in a variety of ways, such as quality of-service attacks. The MPSoC must be designed from the ground up for secure operation. Software and hardware architects must work together to provide the proper system modes and operations that allow the chip to do its job with minimum threat from the outside

6. CONCLUSIONS

Multiprocessor implementation is going to be the advanced technique .It can be used in almost all the applications of Embedded systems in real time The architecture is going to be a key role in developing the High Performance Multiprocessors which is applicable in real future .But the Memory Constraints and Real time applications will be a challenging task while designed a full fledged systems.

7. REFERENCES

[1] Synthesizing Application Specific Multiprocessor Architectures For Process Networks, ***by BK Dwivedi.***

[2] Intel ix2800 and ixp 2850, available at : http://int.xscale-freak.com/XSDoc/IXP2xxx/b1_qual_report.pdf

[3] OMAP4470 mobile application processor available at http://focus.ti.com/pdfs/wtbu/OMAP4470_07-05-v2.pdf

[4] VoIP over WLAN: a use case based on ST Nomadic™ chipset, ***by Diego Malignant.***

[5] The Future of Multiprocessor Systems-on-Chips, ***by Wayne Wolf.***

[6] Website of Texas Instruments : www.ti.com