Reconfigurable Voltage Mode First Order Multifunctional Filter using Single Low Voltage Digitally Controlled CMOS CCII

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ABSTRACT
The digitally controlled current conveyor has been used to realize a novel digitally controlled reconfigurable continuous time voltage mode first order multifunctional filter. The realized filter can provide first order voltage mode low pass, high pass and all pass responses. The pole frequency of the continuous time filter is directly proportional to an n-bit digital control word. The realized digitally controlled continuous time filter is designed and verified using PSPICE and the results thus obtained justify the theory.

General Terms
Digitally programmable continuous time filters.

Keywords
Current conveyors, filters, oscillators.

1. INTRODUCTION
Introduction of digital control to the current conveyor (CCII) has boosted its functional flexibility and versatility in addition to its higher signal bandwidth, greater linearity and large signal bandwidth [1-12]. This digital control has eased the on chip control of continuous time systems through digital word with high resolution capability and reconfigurability [1-5], [11], [12].

This paper basically deals with the realization of a reconfigurable continuous time voltage mode first order multifunctional filter using Low voltage digitally controlled CCII. The new realized filter can provide first order voltage mode low pass, high pass and all pass responses. The pole frequency of the continuous time filter is directly proportional to an n-bit digital control word. To verify the theory, the realized digitally controlled continuous time filter is designed and verified using PSPICE and the results thus obtained justify the theory.

2. THE CIRCUIT
The digitally controlled CCII symbol is shown in “Figure 1(a)” and its CMOS implementation with 4-bit control is shown in “Figure 1(b)”. The current summing network (CSN) is included at port-X. The transfer matrix can be expressed as

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm N^m & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (1)$$

Thus the port voltages and currents for the digitally programmable current conveyor (DPCCII) can be expressed as

$$I_Y = 0, \; V_X = V_Y \quad and$$

$$I_Z = \pm N^m I_X \quad (2)$$

where, N is an n-bit digital control word, the plus sign(+) is for I_{Z+} and minus sign(-) is for I_{Z-}. The power integer m = 1 for current summing network (CSN) at port-Z and m = -1 for the CSN at port-X of the DPCCII [1], [4].

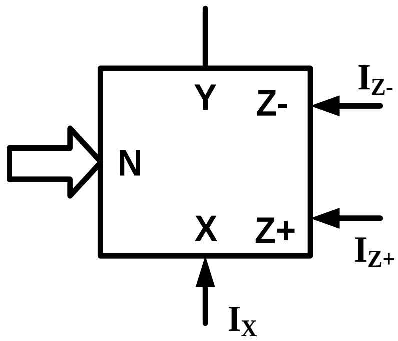

Fig 1(a): Symbol for 4-bit DPCCII

The voltage mode first order multifunctional filter using low voltage digitally controlled CMOS DPCCII is shown in “Figure 2”. The DPCCII uses the CSN at port-X as shown in “Figure 1(b)”, so in equation (2), m = -1.

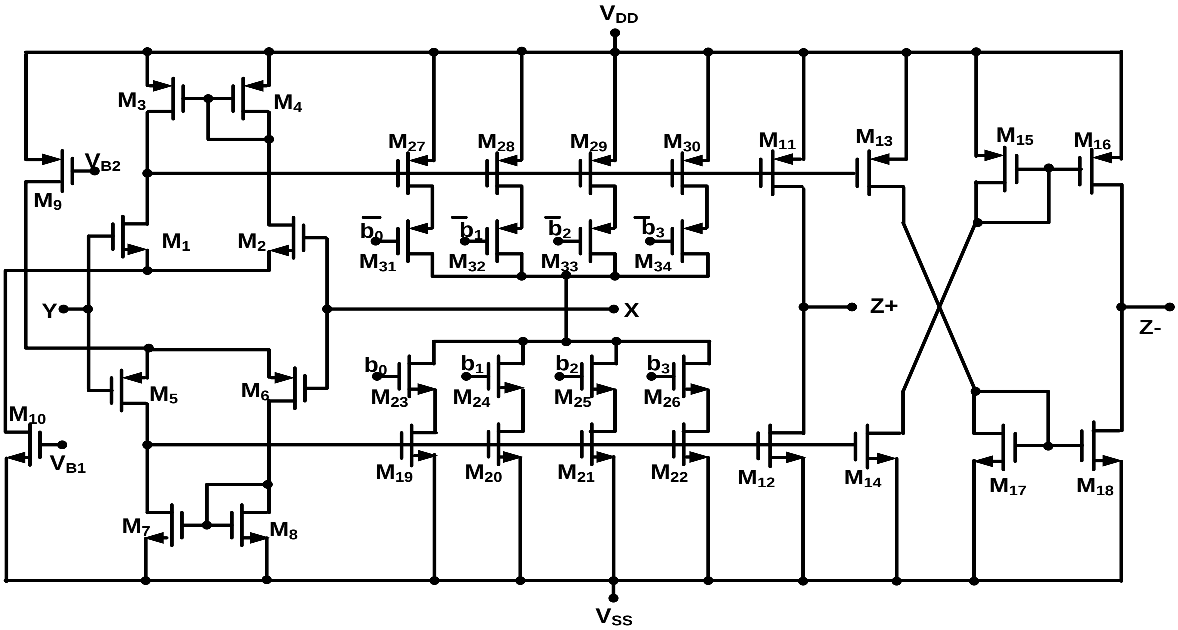

Fig 1(b): The CMOS implementation of a 4-bit DPCCII with CSN at port X

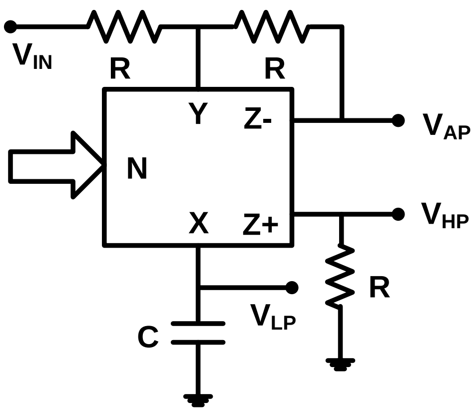

Fig 2: The digitally controlled voltage mode first order multifunctional filter

The routine analysis yields its voltage transfer functions T_{LP}, T_{HP} and T_{AP} respectively for low pass(LPF), high pass (HPF) and all pass (APF) responses as follows.

$$T_{LP} = \frac{V_{LP}}{V_{IN}} = \frac{\frac{N}{RC}}{S + \frac{N}{RC}} \qquad 3(a)$$

$$T_{HP} = \frac{V_{HP}}{V_{IN}} = \frac{S}{S + \frac{N}{RC}} \qquad 3(b)$$

$$T_{AP} = \frac{V_{AP}}{V_{IN}} = -\frac{S - \frac{N}{RC}}{S + \frac{N}{RC}} \qquad 3(c)$$

The pole frequency (ω_0) and the phase angle (ϕ) for the APF can be expressed as follows.

$$\omega_0 = \frac{N}{RC}$$
$$\Phi = -2\tan^{-1}\left(\frac{\omega RC}{N}\right) \qquad (4)$$

From equation (4) it is evident that the pole frequency ω_0 is directly proportional to the digital control word N. Also the phase can be controlled through N at any constant pole-ω_0. The control through external digital control word N, facilitate the on chip system control. Thus the multifunctional filter of "Figure 2" can be used as a programmable module of a field programmable analog array (FPAA)[12].

3. EFFECT OF NON-IDEALITIES

Taking the non-idealities of CCIIs into account, the relationship of the terminal voltages and currents can be rewritten as:

$$V_X = \beta V_Y$$
$$I_Z = \pm \frac{\alpha\, I_X}{N} \qquad (5)$$

In equation (5) β is the voltage transfer gain from terminal-Y to terminal-X for the CCII and α is the current transfer gain for CCII from X to Z+ and Z- respectively. Using equation (5) the ideal transfer functions given in (3) respectively, yield the following non-ideal transfer functions:

$$T_{LP} = \frac{V_{LP}}{V_{IN}} = \frac{\frac{N}{\alpha\beta RC}}{s + \frac{N}{\alpha\beta RC}} \quad 6(a)$$

$$T_{HP} = \frac{V_{HP}}{V_{IN}} = \frac{s}{s + \frac{N}{\alpha\beta RC}} \quad 6(b)$$

$$T_{AP} = \frac{V_{AP}}{V_{IN}} = -\frac{s - \frac{N}{\alpha\beta RC}}{s + \frac{N}{\alpha\beta RC}} \quad 6(c)$$

Also the equation (4) reduces to

$$\omega_0 = \frac{N}{\alpha\beta RC}$$

$$\Phi = -2\tan^{-1}\left(\frac{\omega\alpha\beta RC}{N}\right) \quad (7)$$

The equations (6) and (7) show that the pole-frequency and the phase angle ϕ for the APF are slightly affected due to non-idealities.

4. DESIGN AND VERIFICATION

The realized digitally controlled voltage mode first order multifunctional filter of "Figure 2", was designed and verified by performing PSPICE simulation with supply voltage ± 0.75V using CMOS TSMC 0.25μm technology parameters. The CMOS DPCCII with 4-bit current summing network at port-X (i.e. m = -1) of "Figure 1(b)" was used. The aspect ratios used are given in the "Table 1". The realized filter pole frequency given in equation (4)) was initially designed for a pole frequency of ω_0 = 50 Krad/sec with N = 1, R = 0.5KΩ and C =40nF. Then the pole frequency was controlled through 4-bit digital control word N. The observed frequency responses of the all-pass filter for different control words are given in "Figure 3(a)". The input and output wave shapes of the APF at N = 4 and ϕ = - 90^0 are shown in "Figure 3(b)". The variation of phase angle with frequency of the APF at different control word was also studied and the results are given in "Figure 3(c)". The frequency responses for the LPF and HPF at different control words are given in Fig.4. Thus the results in "Figure 3" and "Figure 4", clearly confirms the close conformity with the theory.

Table 1: The aspect ratios of the MOSFETs of the DPCCII

MOSFETs	W μm	L μm
M_1, M_2, M_5, M_6	5	0.25
M_3, M_4, M_7, M_8	0.5	0.5
M_9, M_{10}	0.5	0.25
M_{11}, M_{12}, M_{13}, M_{14}, M_{15}, M_{16}, M_{17}, M_{18}, M_{19}, M_{23}, M_{27}, M_{31}	25	0.25
M_{20}, M_{24}, M_{28}, M_{32}	50	0.25
M_{21}, M_{25}, M_{29}, M_{33}	100	0.25
M_{22}, M_{26}, M_{30}, M_{34}	200	0.25

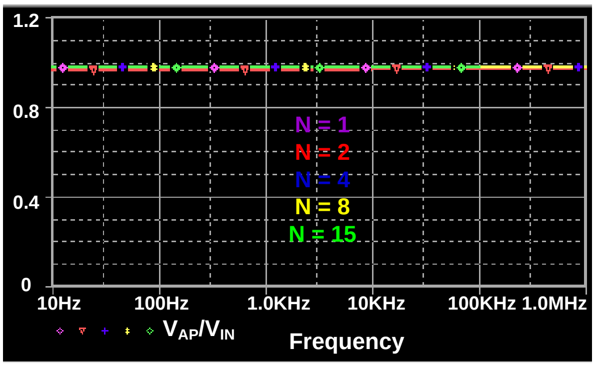

Fig 3(a): Frequency response of AP-Filter at different control word N

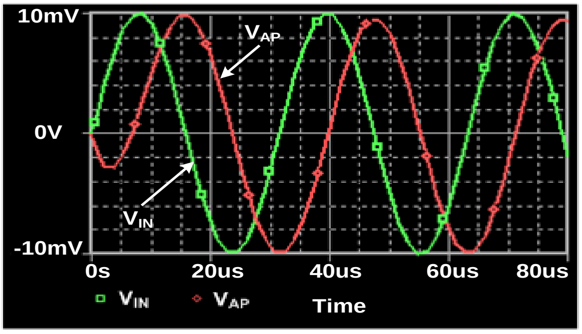

Fig 3(b): Input and output wave shapes of the AP-Filter at control word N = 4 and ω_0 = 200 Krad/sec, with ϕ = - 90^0

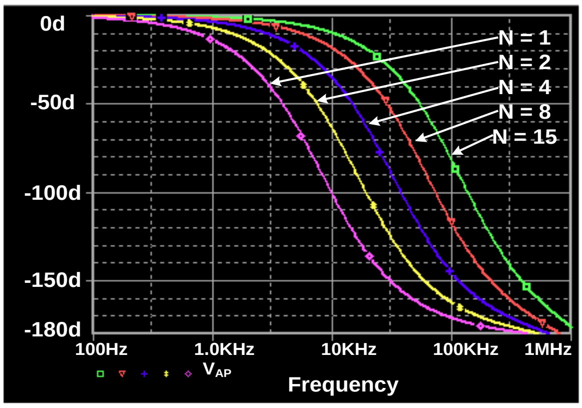

Fig. 3(c). Variation of phase angle of AP-Filter at different control word N

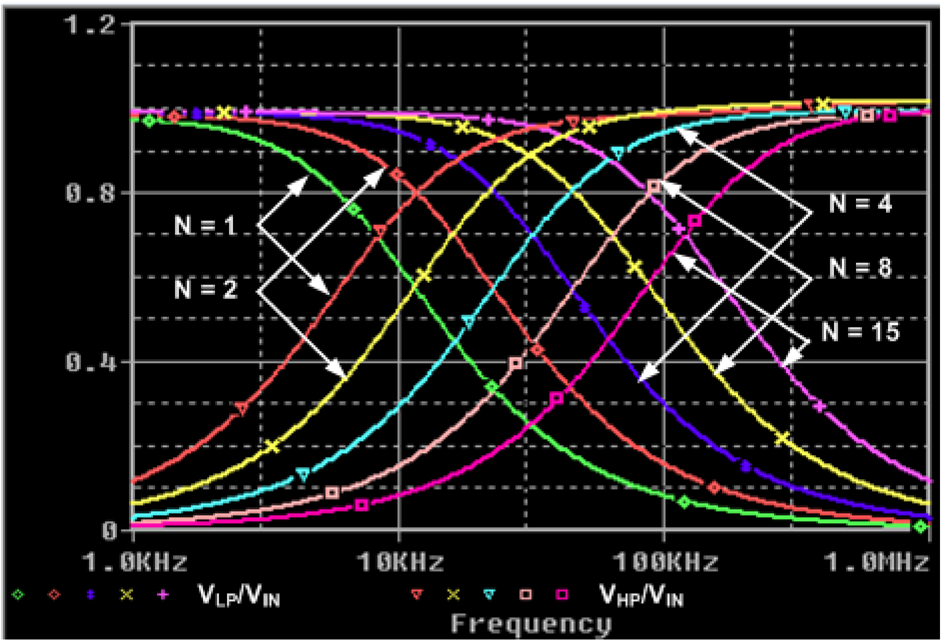

Fig. 4. Frequency response of LP and HP Filters at different control word N

5. CONCLUSION

A novel digitally controlled voltage mode first order multifunctional filter using digitally programmable current conveyor has been presented. The realized filter can provide first order voltage mode low pass, high pass and all pass responses without any component matching constraints. The pole frequency of the continuous time filter is directly proportional to an n-bit digital control word which yields the reconfigurable control.

To verify the theory, the realized digitally controlled continuous time voltage mode first order filter was designed and verified using PSPICE and the results thus obtained justify the theory.

6. REFERENCES

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