Three Dimensional Numerical Simulation and Modeling of Small Geometry Fully Depleted SOI MOSFET

K.Gowri
Assosiate Professor
Department of ECE
PSNA CET, Dindigul

C. Karthikeyini
Assosiate Professor
Department of ECE
PSNA CET, Dindigul

T. Thangam
Assosiate Professor
Department of ECE
PSNA CET, Dindigul

ABSTRACT
A threshold voltage model for small geometry fully depleted Silicon-On-Insulator (SOI MOSFET), based on the numerical solution of three dimensional Poisson's equation is presented in this paper. Liebmann's iteration method was used to solve the three dimensional Poisson's equation with necessary boundary conditions. By using the solution of the Poisson's equation potential profile, electric field profile, mobility profile, transfer characteristics and transconductance Vs gate voltage characteristics were calculated and plotted.

General Terms
Device modeling , Numerical model

Keywords
Fully depleted, silicon-on-insulator (SOI) MOSFET, small geometry, threshold voltage.

1. INTRODUCTION
Numerical modeling of the electrical behavior of semiconductor devices is playing an increasingly important role in their development. Examples that pertain to advanced MOSFETs and bipolar transistors are presented to illustrate the importance of taking into account three-dimensional as well as non-equilibrium and non-local physical phenomena to effectively characterize the electrical behavior of such devices [1]. CMOS circuits fabricated on silicon-on-insulator (SOI) wafers are gaining prominence in present-day very large-scale integration (VLSI) technology. SOI technology shows better performance over its bulk counterpart. The main advantages of SOI technology are the following. As the individual devices are perfectly isolated, latch up can be totally eliminated. SOI MOSFETs are having higher radiation tolerance. These devices have lower leakage current. The switching of these devices is fast due to the lower capacitance between device and substrate. Also power dissipation of SOI MOSFET is small; it is achieved because of the steeper sub threshold characteristics of the SOI transistor allow it to be operated at lower voltages [2]. Although SOI CMOS technology is now being widely used, there still exists the need to develop numerical device models for SOI-based MOSFETs suitable for circuit simulation. The analytical modeling of the threshold voltage of FD SOI MOSFETs has already been reported by numerous authors [3]-[5]. It is becoming increasing difficult to use one-dimensional or even two-dimensional (2D) models to describe the behavior of many small device structures; three-dimensional (3D) models are necessary to address the geometric dependencies of such structures [6]. There fore three dimensional numerical device models are important for the accurate electrical characterization of small geometry devices [7] – [8]. The reason for this is that the numerical approach is readily applicable to any 2 dimensional and 3 dimensional problems. Therefore it is worthwhile to realize a device using numerical modeling to get a more accurate result than that of an analytical model. The 3-D Poisson's Equation is numerically solved by using Liebman's iteration. The boundary conditions used for the solution of Poisson's equation are applicable only for bulk MOSFETs. The surface potential for the SOI MOSFET can be obtained from this solution of three dimensional Poisson's equation. The electric field and mobility is also calculated based on the surface potential. David Esseni [9] described a mobility model for SOI MOSFET using solution of 1D Poisson's equation. A short-channel threshold voltage model for FDSOI MOSFET is developed using a quasi-two-dimensional approach similar to those used for modeling threshold voltage, substrate current, and other hot-electron phenomena in bulk MOSFET's are also discussed in [10]-[14].

2. MODELING OF SOI MOSFET
The cross-sectional view of an n- channel SOI MOSFET along the channel length is shown in Fig. 1. If the silicon channel thickness is small, it will become fully depleted before channel inversion. In general, in order to analyze this structure, we need to solve both the Poisson's equation and current continuity equation. However, in the sub threshold regime, and in the linear regime with small V_{ds}, the currents are small and Poisson's equation alone is sufficient [15].

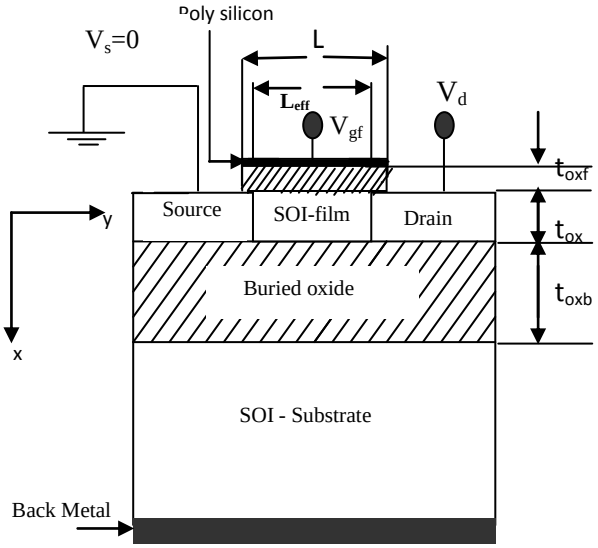


Fig: 1 Cross sectional view of SOI MOSFET along channel length

The source–SOI film and drain–SOI film junctions are located at y=0 and y=L_{eff}, respectively, where L_{eff} is the effective

channel length. The front and back Si–SiO_2 interfaces are located at x=0 and x=t_s, where t_s is the SOI film thickness. The t_{oxf} and t_{oxb} are the front and the back gate oxide thicknesses, respectively, where the applied potential to the front and back gates are V_{gf} and V_{gb}.

The sidewall Si–SiO_2 interfaces are located at z=0 and z=w. The thickness of the side wall oxide is around 1.5 times the thickness of the gate oxide because the parasitic sidewall transistor is normally oriented along the surface.

In order to analyze the structure shown in Fig. 1, we need to solve both Poisson's equation and current continuity equation. However, in the sub threshold regime, the currents are small and Poisson's equation alone is sufficient. In this paper, we consider a fully depleted (FD) SOI film. The 3-D Poisson's equation in the FD SOI film region is given by,

$$\frac{\partial^2\psi(x,y,z)}{\partial x^2}+\frac{\partial^2\psi(x,y,z)}{\partial y^2}+\frac{\partial^2\psi(x,y,z)}{\partial z^2}=\frac{qN_A}{\varepsilon_{si}} \quad (1)$$

where N_A is the doping concentration and $\psi(x,y,z)$ is the potential at a particular point (x,y,z) in the SOI film.

The boundary conditions required to solve the 3-D Poisson's equation are given as,

$$\psi(0,y,z)-\frac{t_{oxf}}{\varepsilon_{ox}}\left[\varepsilon_{si}\left|\frac{\partial\psi(x,y,z)}{\partial x}\right|_{x=0}-Q_{it}^{f}\right]=V_{gf}-V_{fb}^{f} \quad (2)$$

$$\psi(t_s,y,z)-\frac{t_{oxb}}{\varepsilon_{ox}}\left[\varepsilon_{si}\left|\frac{\partial\psi(x,y,z)}{\partial x}\right|_{x=t_s}+Q_{it}^{b}\right]=V_{gb}-V_{fb}^{b} \quad (3)$$

$$\psi(x,0,z)=V_{bi} \quad (4)$$

$$\psi(x,L_{eff},z)=V_{bi}+V_{ds} \quad (5)$$

$$\psi(x,y,0)-\frac{t_{oxw}}{\varepsilon_{ox}}\left[\varepsilon_{si}\left|\frac{\partial\psi(x,y,z)}{\partial z}\right|_{z=0}-Q_{it}^{f}\right]=V_{gf}-V_{fb}^{f} \quad (6)$$

$$\psi(x,y,W)+\frac{t_{oxw}}{\varepsilon_{ox}}\left[\varepsilon_{si}\left|\frac{\partial\psi(x,y,z)}{\partial z}\right|_{z=W}+Q_{it}^{f}\right]=V_{gf}-V_{fb}^{f} \quad (7)$$

The boundary conditions given by (2) and (3) indicate that the potential applied at the front (back) gate is the sum of the potential at the front (back) Si–SiO_2 interface and the drop across the front (back) gate oxide. In (2) and (3), V_{gf} and V_{gb} are the flat band voltages and Q_{it}^{f} and Q_{it}^{b} are the interface trapped charges associated with the front and back gates respectively, and ε_{si} and ε_{ox} are the permittivity for silicon and silicon dioxide, respectively. Equations (4) and (5) represent the boundary conditions at the source and drain ends of the channel, V_{bi} being the built-in potential of the n^+ -p junctions and V_{ds} is the drain-to-source applied voltage. Equations (6) and (7) indicate that the potential applied at the front gate is the sum of the surface potential at the edge of the transistor and the drop across the sidewall oxide.

Now to obtain the potential field profile, the 3D Poisson's Equation is numerically solved by considering the entire channel length to be divided in to large number of strips. Thus we will obtain the potential at every point in the channel.

From the potential values obtained from the numerical solution we can find out the electric field. The electric field equations in x, y and z directions are given by,

$$E_x=\frac{\psi(i+1,j,l)-\psi(i-1,j,l)}{\frac{2L}{m_x}} \quad (8)$$

$$E_y=\frac{\psi(i,j+1,l)-\psi(i,j-1,l)}{\frac{2W}{m_y}} \quad (9)$$

$$E_z=\frac{\psi(i,j,l+1)-\psi(i,j,l-1)}{\frac{2t_s}{m_z}} \quad (10)$$

Where m_x, m_y and m_z are the separation of grid line along x, y, z directions. $\psi(i,j,l)$ is the surface potential.

L, W, t_s are the gate length, device width & oxide thickness respectively.

We can find out the mobility of charge carriers from the electric field values. The mobility in x, y, z directions is given by,

$$\mu_x=E_x\varepsilon_{si}\varepsilon_{ox} \quad (11)$$

$$\mu_y=E_y\varepsilon_{si}\varepsilon_{ox} \quad (12)$$

$$\mu_z=E_z\varepsilon_{si}\,\varepsilon_{ox} \quad (13)$$

The drain – source current I_{ds} can be obtained from the continuity equation. I_{ds} is obtained as,

$$I_{ds}=\frac{\varepsilon_{ox}}{d_{ox}}Z\mu_x\left(V_{gs}-V_{th}-V(x)\right)E_x \quad (14)$$

Where ε_{ox} & d_{ox} are the permittivity & thickness of oxide layer respectively.

μ_{ox} & E_x represents the mobility & electric field along the length of channel.

V_{gs} denotes gate – source voltage.

V_{th} represents threshold voltage.

V_x is the surface potential.

3. COMPUTATIONAL TECHNIQUES

The basic 3D Poisson's equation (1) is solved using Liebmann's iterative method to determine the surface potential for fixed value of gate voltage and assumed value of the drain voltage. The numerically estimated value of the surface potential is utilized to determine the charge per unit area in the inversion region. The drain current has been calculated from equation (14). The voltage profile and the electric field distribution in the channel have been estimated for accurate calculation of the drain to source current. The voltage profile in the channel is obtained by calculating the differential change in the voltage across the channel and is assumed to be very small (1mV) at the source end and low field mobility has been used to begin the numerical computation from the source end. The field dependant mobility has been computed by estimating the electric field at any point (x, y, z). The field in the channel has been calculated by numerical simulation.

The voltage profile in the channel is obtained by dividing the channel region into several meshes and then calculating the differential change in voltage across the channel. The numerically estimated surface potential value is used to determine the electric field and mobility profile.

$$\psi(i,j,l)=\psi(i-1,j,l)+\psi(i+1,j,l)+\psi(i,j-1,l)+\psi(i,j+1,l)$$
$$+\psi(i,j,l-1)+\psi(i,j,l+1)-\left(\left(q*{}^{N_a}\!/\!_{\varepsilon_{si}}\right)/6\right) \quad (15)$$

4. RESULTS AND DISCUSSION

The device parameters used for the modeling and numerical simulation are given in the table below.

Table. 1

Parameters	Value
Gate Length L	100nm
Device Width W	80nm
Oxide Layer Thickness t_s	30nm
Intrinsic carrier concentration N_i	$1.2*10^{13}/m^3$
Acceptor concentration,N_A	$10^{21}/m^3$
Front gate oxide thickness t_{oxf}	3nm
Back gate oxide thickness t_{oxb}	400nm
Side wall oxide thickness t_{oxw}	15nm

4.1 Potential distribution along length of channel

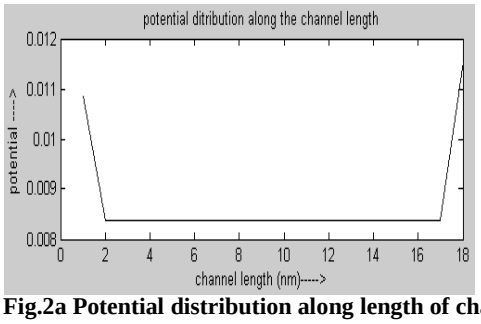
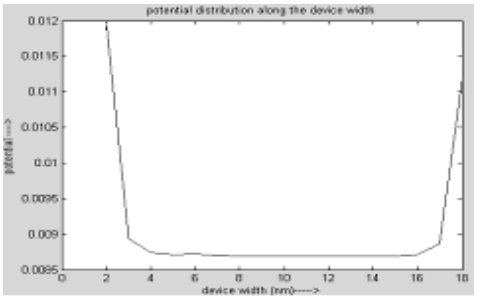


Fig.2a Potential distribution along length of channel

Figures 2a and 2b represent the typical two dimensional potential profiles along channel length and device width respectively.

From this graph we found that the surface potential decreases linearly near the source end and increases linearly near drain end. This is due the fact that the high electric field near the drain causes the conductivity rapidly. Due to this it is expected that the electric field near the drain end reaches the critical field for high drain voltage and hence causes the velocity saturation.

4.2 Potential distribution along the device width



. Fig.2b Potential distribution along the device width

4.3 Potential distribution along the channel length & device width

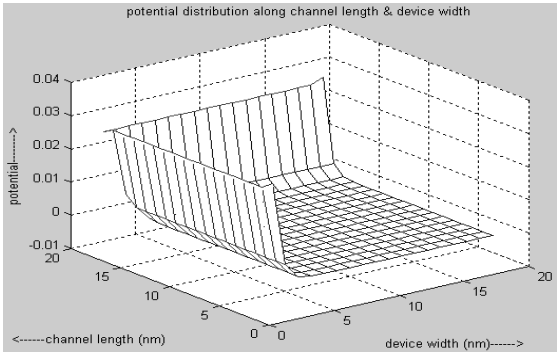


Fig. 2c Potential distribution along the channel length & device width

The potential profile along the channel length & device width in a 3 dimensional figure is shown in fig.2C. The potential increases near the drain because of the applied positive bias at the drain electrode.

4.4 Electric field along length of the channel

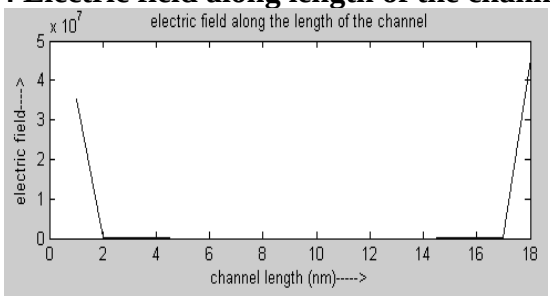


Fig.3a Electric field along length of the channel

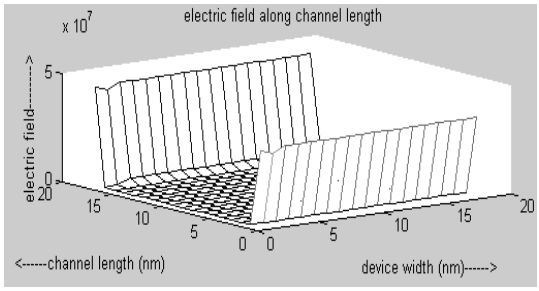


Fig.3b Electric field along length of the channel

The electric field distribution along the channel length, device width & oxide thickness is also obtained and it is shown in figures 3a, 4a & 5. The electric field along the length of the channel (E_x) is dominant over the electric along device width (E_y) and the electric field along oxide thickness (E_z). . The electric field increases rapidly near the drain end. This is due to the fact that the carrier density near the drain end experiences a rapid decrease in surface concentration which calls for a rapid increase in the electric field to maintain the constant drain current

It can be observed from the figures 4a & 5 that both E_y and E_z decrease rapidly near the drain end. This is due to the application of V_{gs} ; electrons acquire more energy to move along the length of channel. Thus E_x increases rapidly near drain end. The corresponding three dimensional models are also shown in figures 3b & 4b.

4.5 Electric field along the device width

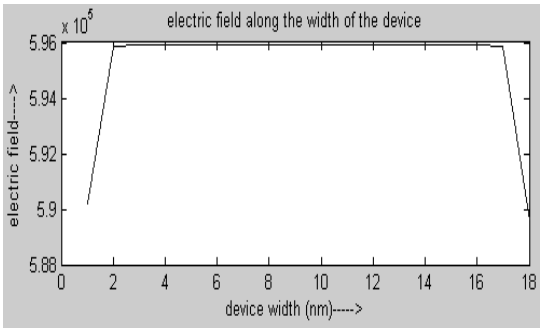


Fig.4a Electric field along the device width

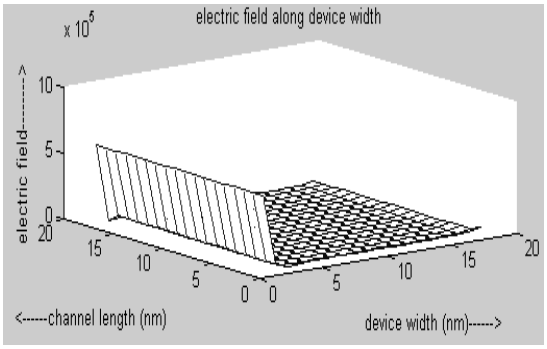


Fig.4b Electric field along the device width

4.6 Electric field along oxide thickness

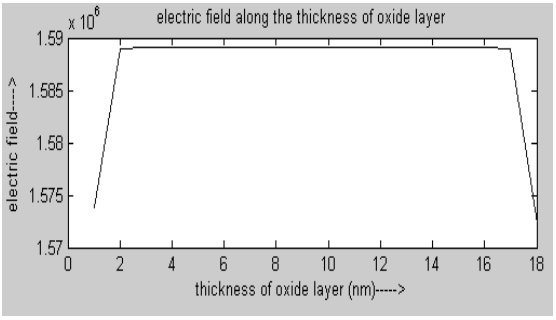


Fig.5 Electric field along oxide thickness

4.7 Mobility along channel length

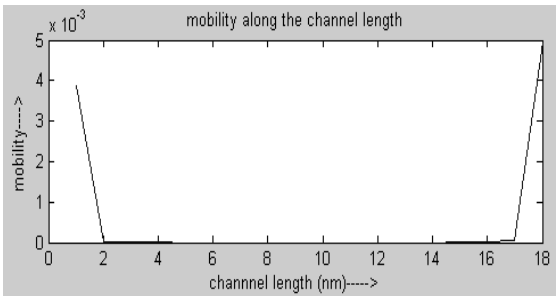


Fig. 6a Mobility along channel length

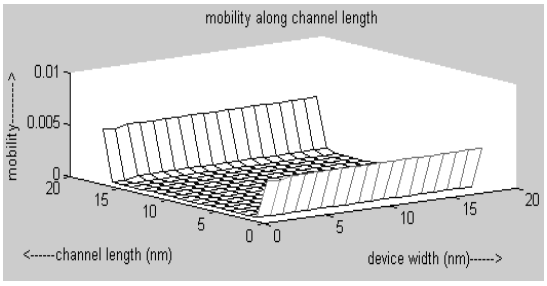


Fig. 6b Mobility along channel length

The mobility variation along the channel length is shown in figure 6a and its three dimensional plot is shown in figure 6b. We know that mobility is directly proportional to the electric field. So the shape of the mobility curve along the channel length is same as that of the electric field curve along channel length (E_x). The mobility has a drastic increase near the drain end.

4.8 Mobility along device width

The mobility variation along the device width is shown in figure 7a and its three dimensional plot is given in figure 7b. In this case also the shape of the mobility curve along device width is same as that of the electric field profile along the device width (E_y). Near the drain end there is a drastic reduction in mobility of charge carriers

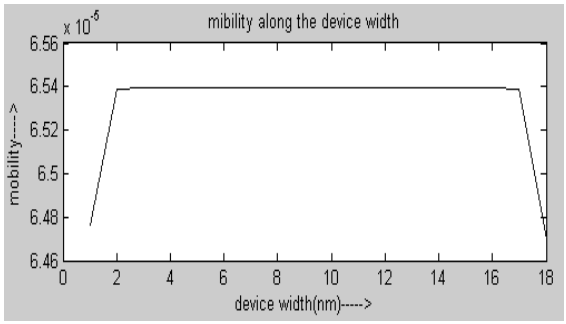


Fig. 7a Mobility along device width

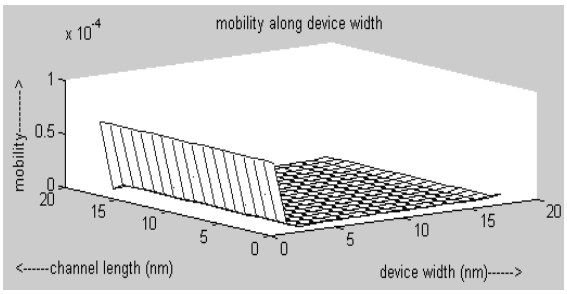


Fig. 7b Mobility along device width

The value of mobility (velocity per unit electric field) is influenced by several factors. The mechanisms of conduction through the valence and conduction bands are different, and so the mobility associated with electrons and holes are different. The value for electrons is more than twice that for holes at low values of doping. As the density of dopants increases, more scattering occurs during conduction. Mobility therefore decreases as doping increases. At low temperatures, electrons and holes gain more energy than the lattice with increasing T, therefore mobility increases. At high temperatures, lattice scattering dominates, and thus mobility falls.

4.9 Mobility along oxide thickness

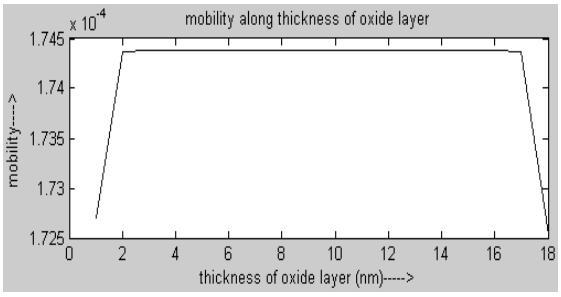


Fig.8 Mobility along oxide thickness

The mobility variation along the oxide thickness is shown in figure 8. As we explained above the shape of the characteristics will be same as that of the electric field profile along the oxide thickness (E_z). Near the drain end there is a drastic reduction in mobility of charge carriers.

4.9 Transfer characteristics

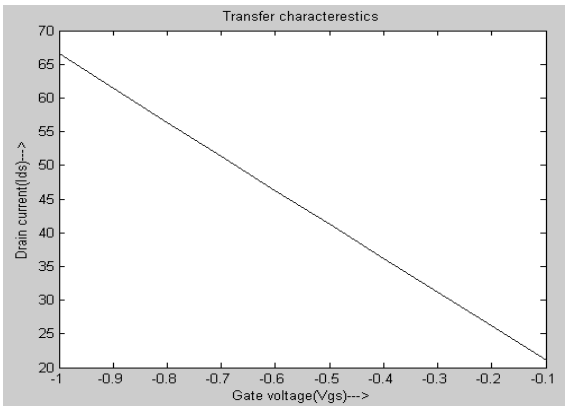


Fig. 9 Transfer characteristics

The transfer characteristics of the MOSFET are also obtained for different values of gate voltage. As the applied gate to source voltage increases, the drain current also increases for fixed drain voltage. This is due to the fact that the excess carriers generated in the channel. When the drain voltage increases, the drain current also increases rapidly. The transfer characteristic is shown in figure 8.

The linear transfer characteristics are provided by a MOSFET having a channel that operates in a linear mode and a drift region that simultaneously supports large voltages and operates in a current saturation mode. A relatively highly doped transition region is preferably provided between the channel region and the drift region. Upon depletion, this transition region provides a potential barrier that supports separate and simultaneous linear and current saturation modes.

4.10 Tran conductance Vs gate voltage

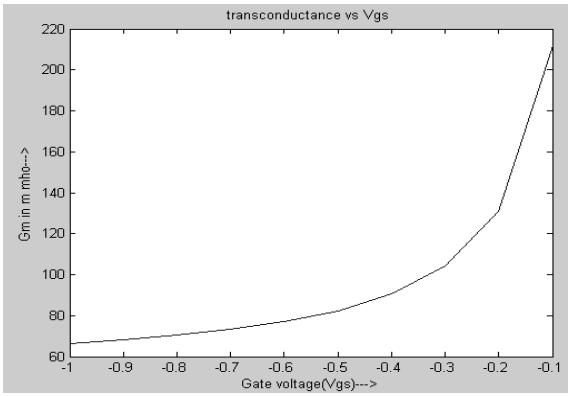


Fig. 10 Transconductance Vs gate voltage

The Trans conductance Vs a gate voltage characteristic is also obtained and is shown in figure 10. Transconductance, G_m, is a measure of the sensitivity of drain current to changes in gate-source bias. The transconductance is defined as $G_m=I_{ds}/V_{gs}$. This parameter is normally quoted for a V_{gs}

5. CONCLUSION

A threshold voltage model for mesa isolated fully depleted (FD) SOI MOSFET based on numerical solution of 3-D Poisson's equation is presented. The device can be considered as a nano device as all device dimensions are in nano meter range. The potential distribution is obtained from the numerical solution of 3D Poisson's equation. The voltage profile and electric field of the device enhance the study of various other parameters. The field dependent mobility of the carriers in the surface channel should be considered for the short channel device simulation because it drastically modifies the characteristics of the device. Various other characteristic like transfer characteristics and transconductance Vs gate voltage characteristics is also discussed in this paper.

6. REFERENCES

[1] Konard Young , Member , IEEE , " Short Channel Effect in Fully depleted SOI MOSFET's", IEEE Transactions on Electron Devices, Vol. 36, No. 2, February 1989.

[2] Guruprasad Katti , Nandita DasGupta , Amitava DasGupta , "Threshold Voltage Model for Mesa – Isolated Small Geometry Fully Depleted SOI MOSFETs Based onAnalytical Solution of three Dimensional Poisson's Equation", IEEE Transactions On Electron Devices, Vol. 51, No. 7, July 2004.

[3] Jason C. S. Woo, Kyle W. Terrill, Prahalad K. Vasudev, " Two – Dimensional Analytic Modeling of Very Thin SO1 MOSFET's ", IEEE Transactions on Electron Devices , Vol. 37. No.9. September 1990.

[4] Hans van Meer, Kristin De Meyer , "A 2-D Analytical Threshold Voltage Model for Fully-Depleted SOI MOSFETs with Halos or Pockets ", IEEE Transactions on Electron Devices, Vol. 48, No. 10, October 2001.

[5] H.K Lim, J.G.Fossum," Threshold voltage of thin film SOI MOSFETs", IEEE Transactions on electron devices, Vol. 30, Oct 1983.

[6] Francis Balestra, Mohcine Benachir, Jean Brini , Gerard Ghibaudo , Analytical Models of Sub threshold Swing and Threshold Voltage for Thin- and Ultra-Thin - Film SO1 MOSFET's , IEEE Transactions On Electron Devices. Vol 37. No II. November 1990.

[7] C.Mallikarjun, K. N . Bhat , " Numerical and Charge Sheet Models for Thin – Film SO1 MOSFET's ",IEEE Transactions On Electron Devices , Vol. 37. No. 9. September 1990.

[8] Takeshi Shima , Hisashi Yamada , Ryo Luong MoDang,"Table Look-Up Simulator MOSFET Modeling System Using a 2-D Device and MonotonicPiecewise cubic Interpolation " ,IEEE transactions on Computer Aided design of Integrated Circuits and Systems, Vol.CAD.2, No.2, April 1983.

[9] David Esseni, Antonio Abramo, Luca Selmi, Enrico Sangiorgi , " Physically Based Modeling of Low Field Electron Mobility in Ultrathin Single - and Double – Gate SOI N - MOSFETs " , IEEE Transactions On Electron Devices ,Vol. 50, No.12, December 2003.

[10] 10.S. Veeraraghavan and J. G. Fossum , " Short - channel effects in SO1 MOSFET'S " IEEE Trans. Electron Devices , vol. 36 , pp. 522-528, 1989.

[11] Z. H. Liu , C. H. Hu , J. H. Huang , T. Y. Chan , M. C. Jeng , P. K. KO, and Y. C. Cheng, "Threshold voltage model for deep- sub micrometer MOSFET 's," IEEE Trans. Electron Devices, vol. 40, pp. 86-95, 1993.

[12] Y. A. El – Mansy and A. R. Boothroyd, "A simple two - dimensional model for IGFET operation in the saturation region," IEEE Trans. Electron Devices, vol. 24, p. 254, 1977.

[13] T. Y. Chan , P. K. KO , and C. Hu , " Dependence of channel electric field on device scaling,'' IEEE Electron Devices Lett., vol. 6, p. 551, 1985.

[14] K. W. Temll , C. Hu, and P. K. KO , " An analytical model for the channel electric field in MOSFET with graded - drain structure," IEEE Electron Device Lett., vol. 5, p. 440, 1984.

[15] J. R. Pfiester , J . D. Shott, and J . D. Meindl , " Performance limits of CMOS ULSI ," IEEE Trans. Electron Devices, vol. ED- 32, pp. 333- 343, 1985.

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