Minimization of Switching Losses for Diode Clamped Multilevel Inverter

R. Pon Perumal
PG scholar
School of Electrical Engineering
VIT University
Vellore, India

W. Razia Sultana
Assistant Professor
School of Electrical Engineering
VIT University

Sarat Kumar Sahoo
Associate Professor
School of Electrical Engineering
VIT University
Vellore, India

ABSTRACT
Multilevel inverters are emerging as a most promising alternative for reducing the harmonics and to achieve high-voltage, high-power capability but switching losses are increased because of increased device count. Many modulation techniques like soft switching techniques, space vector-based PWM techniques or sinusoidal PWM-based techniques were employed to reduce the switching losses. In this paper, a carrier-based closed-loop PWM control technique has been proposed based on insertion of 'no switching' zone within each positive and negative half cycle of fundamental wave to reduce the switching losses. This method effectively reduces the switching losses of three-level inverter as it does not require any complex mathematical expressions involved in space vector based technique. Moreover, THD is found within 5% for a switching frequency of 5 kHz with proposed technique over conventional SPWM technique. Simulation results are presented to validate the proposed technique. Comparisons are made between switching losses of conventional and proposed control technique of three level diode clamped inverter.

Keywords
Multilevel inverters, Carrier based pulse width modulation, Switching losses, Total harmonic distortion.

1. INTRODUCTION
Nowadays, multilevel inverters have achieved an increasing contribution in medium and high-voltage applications. They have the advantage of producing high-voltage, high-power capability with improved voltage quality. Problems related to series–parallel connections of switching devices are also eliminated. Recent advances in power semiconductor technology by using (IGBT/MOSFET)as switches leads to the use of high frequency switching modulation techniques in power inverters to reduce the harmonic contents in output voltage. To reduce the filtering requirement in almost all the inverter topologies, switching frequency is increased which in turn increases the switching losses thus reducing the system efficiency. Since there are 12 switching devices involved in three-level inverter and more in higher level inverters, switching loss problem becomes more serious. Fig. 1 shows the structure of three phase three-level diode clamped inverter and Table 1 gives the switching sequences to generate the three-level output voltage for phase 'A'. Conventional space vector (SVPWM) and other PWM techniques just sacrifices switching losses to improve the harmonic profile of the output voltage. Voltage-source multilevel inverters, which can be divided into three categories, according to their topological modifications: neutral point clamped (NPC), flying capacitor (FLC), and cascade H-bridge [1].

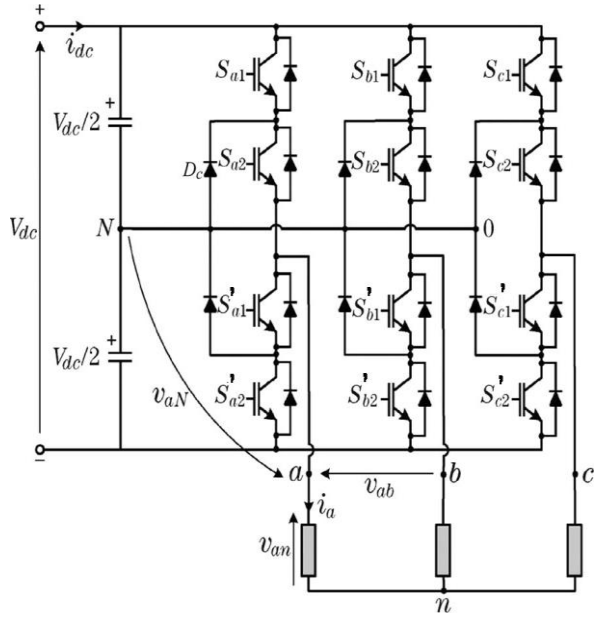


Fig. 1 Structure of three phase three level diode clamped inverter.

Among the high-power converters shown, the NPC inverter introduced 20 years ago is the most widely used in all types of industrial applications [2,3,4], in the range of 3.3 to 4.16 kV, with some applications up to 5 kV. Switching losses can be reduced by employing slight topological modifications to achieve soft switching technique [5].

For the control of power electronics converters, soft switching techniques are used to improve the performance of the system, and it also allows high-frequency operation with reduced acoustic noise and electromagnetic interference (EMI), reduced switching losses, reduced dv/dt and di/dt stress across each switch and better controllability. While working with delta modulation technique, soft switching operation restricts the modulation process at some stage such as in the case of resonant DC link topology, in which the benefits of using very high switching frequency are partially reduced

Comparison of SVPWM and SPWM techniques as applied in quasi-resonant soft switched two-level inverter is proposed in [6]. Space vector based PWM technique is proposed for reduced switching loss by using closed-loop control of induction motor [6]. However, three-level inverter provides 27 output voltage space vectors resulting in more complex control and the degree of freedom to generate the command vector also increases. Complexity increases with number of levels. A comparison of total harmonic distortion (THD) and switching losses in conventional two-level inverter with multilevel inverters (three-level and five-level) at different switching frequencies has been presented in [8]. Mostly,

research works were concentrated on the SVPWM which involves complex mathematical calculation with reduced harmonic profile, but not on the reduced switching losses.

Table 1. Switching states of three level diode clamped inverter

Sa1	Sa2	Sa1'	Sa2'	Output pole voltage Vao	Output phase voltage Vab
1	1	0	0	Vdc	Vdc/2
0	1	1	0	Vdc/2	0
0	0	1	1	0	-Vdc/2

In this paper, a closed-loop carrier-based PWM control technique has been proposed based on insertion of 'no switching' zone within each positive and negative half cycle of fundamental wave to reduce the THD and switching losses of three level inverter. The positioning of 'no switching zone' is controlled by controlling the parameters of PI regulators both used at dc and load voltage side. This method effectively reduces the switching losses of three-level inverter as it does not require any complex mathematical expressions as involved in space vector-based techniques. An improvement of THD within 5% specified limit imposed by IEEE 519-1992 standard for a switching frequency of 5 kHz is observed with proposed technique over conventional SPWM technique. Simulation results are presented to validate the proposed concept.

2. SWITCHING LOSS CALCULATIONS

Almost in various applications of inverters, total power losses can be divided into following parts: switching losses, snubber losses, conduction losses and off-state losses. Generally, switching losses depend on switching frequency of power semiconductor devices and instantaneous value of device voltage and current during switching interval.

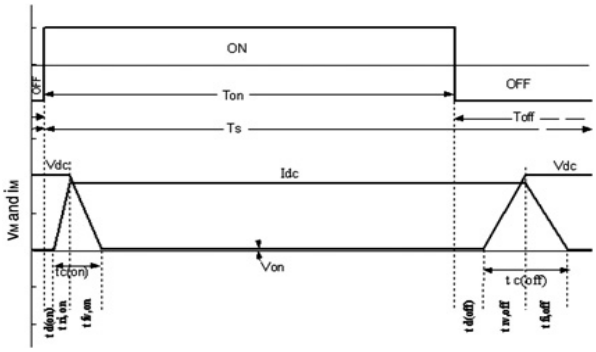


Fig. 2 Linearised switching characteristics of controllable switch (IGBT/MOSFET).

Switching losses become more dominant part of the total power loss in high switching frequency applications. Off-state losses are insignificant for normal ambient temperature. Conduction losses are directly proportional to magnitude of load current [9, 10].

Consider a single controllable switch (IGBT/MOSFET) connected across a DC voltage of value Vdc. Current through switch during ON time is considered as I_{dc}. Fig.2 shows the waveforms of voltage across and current through the switch when it is operated at a switching frequency of f_s ¼ $1/T_s$, where T_s is the switching period. To simplify the expressions, the switching waveforms are represented by linear approximations. In the figure, v_M and i_M are the voltage across and current through the MOSFET.

Instantaneous voltage and current through the switch can be expressed as

$$v(t) = V_{dc} - (V_{dc} - V_{on})\frac{t}{t_{c,on}}$$

$$i(t) = I_{dc} - \frac{t}{t_{c,on}}$$

$$P_{sw} = \frac{1}{6}(V_{dc} I_{dc} \frac{t_{c,on} + t_{c,off}}{T_S}) + \frac{1}{3}\{V_{on} I_{dc} \frac{t_{c,on} + t_{c,off}}{T_S}\}$$

Where $t_{c,on}$ is the turn on time and $t_{c,on}$ is the turn off transition time. P_{SW} shows that switching power losses in a semiconductor switch and it varies linearly with the switching frequency and switching times. Therefore with the devices having short switching times, it is possible to operate them at higher switching frequency, thus avoiding excessive switching power losses in the device [8].

3. PROPOSED CLOSED LOOP PWM CONTROL TECHNIQUE

This section presents the proposed closed loop PWM control technique to reduce THD and switching losses of the three level inverter using carrier based sinusoidal PWM strategy. Fig. 3 shows the block diagram of proposed method and Fig. 4 shows the control scheme for proposed closed loop PWM technique.

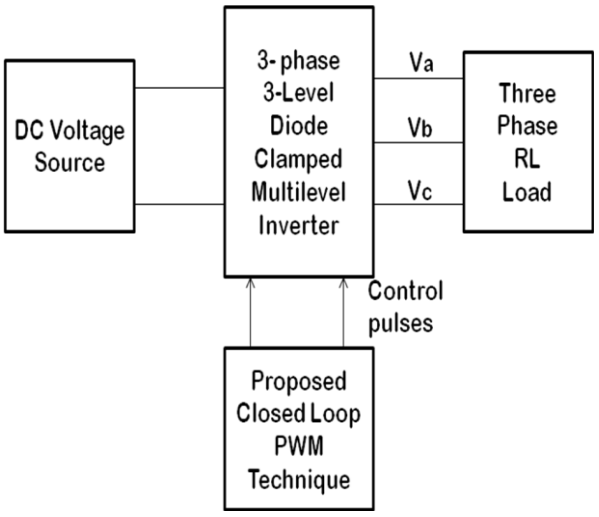


Fig. 3 Block diagram of proposed closed loop PWM technique.

Switching losses can be reduced by reducing either switching frequency or instantaneous values of voltage and current at the time of switching as indicated in (3). Fig.4. the presented technique is based on carrier based SPWM method with two PI regulators used at both dc and load voltage side as given in controlling the parameters of PI regulator at DC side and load side. The positioning of this 'no switching' zone can be controlled by these parameters to generate pulses.

At the load voltage side, three phase inverter output voltages are sensed and converted into per unit system. These per unit voltages are converted into dqo axis using following 3-phase to two-phase conversion,

$V_d = 2/3\ [V_a \sin(t) + V_b \sin(t-120^o) + V_c \sin(t-240^o)]$,

$V_q = 2/3 [V_a \cos(t) + V_b \cos(t-120^o) + V_c \cos(t-240^o)]$,
$V_0 = (V_a + V_b + V_c)/3$
These dqo voltages, Vdqo, are compared with set values of dqo voltages Vdqo*. It results in voltage error which is processed through a proportional-integral (PI) controller to generate two axis command signals Vdq. Then three phase reference voltage signal for PWM generator is synthesized using following two-to-three phase conversion,

$V_a = [V_d \sin(t) + V_q \cos(t) + Vo]$,

$V_b = [V_d \sin(t-120^o) + V_q \cos(t-120^o) + Vo]$,
$V_c = [V_d \sin(t-240^o) + V_q \cos(t-240^o) + Vo]$
and also from the DC voltage side, Vdc1 and Vdc2 voltages are sensed and added to get the error signals, then they are given to the PI regulator and processed to create appropriate offset signal. This offset signal is to be added with the actual modulating signals. In PWM generator, modulating signal is compared with the high frequency carrier signals to generate the control pulses for the diode clamped inverter.
.

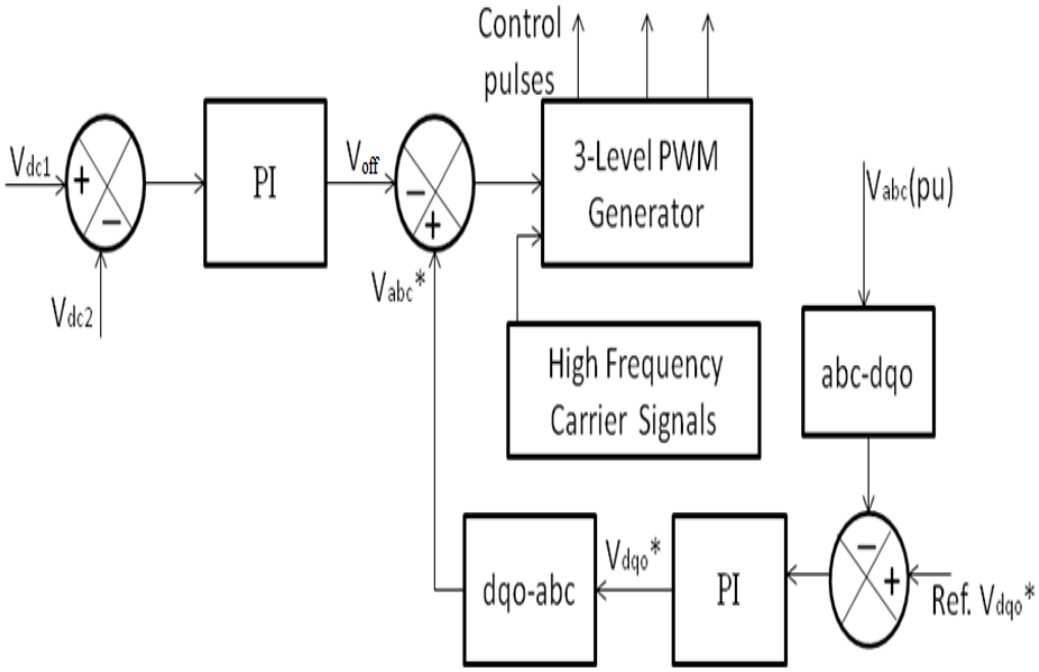


Fig.4 Control scheme for proposed closed loop PWM technique.

4. SIMULATION RESULTS

A simulation model of the proposed technique is developed in MATLAB/Simulink environment. The parameters used for simulation work are given in Table 2. Phase voltage (Van), line voltage (Vab) and Frequency spectrum of line voltage (Vab) with conventional SPWM technique is shown in Fig. 5. Load voltage and Frequency spectrums of inverter line voltage (Vab) with conventional SPWM technique after filtering are shown in Fig. 6.

Table 2. Simulation parameters

DC link voltage	680 V
DC link capacitor	2200 µF
Filter inductance	0.1mH
Filter capacitance	1400µF
Frequency	50Hz
Load resistance	100ohm
Load inductance	0.1mH
Switching frequency	5KHz

Phase voltage (Van) and line voltage (Vab) with proposed closed loop PWM control technique are shown in Fig .7.
Inverter line voltage (Vab) and Frequency spectrum of inverter line voltage with closed loop PWM control technique after filtering are shown in Fig. 8.

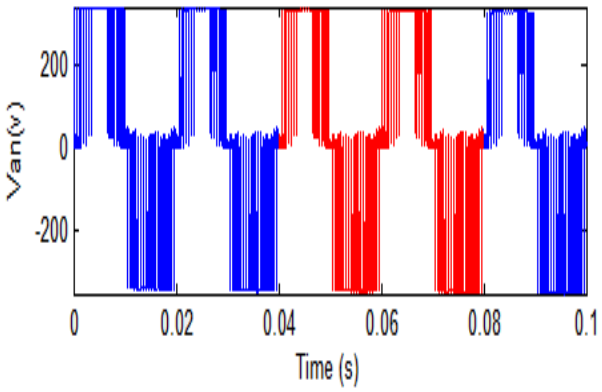
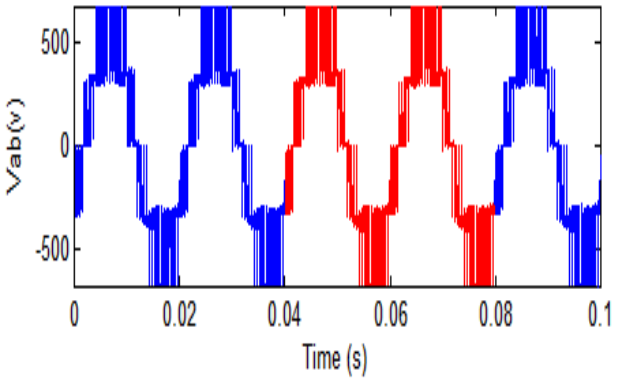
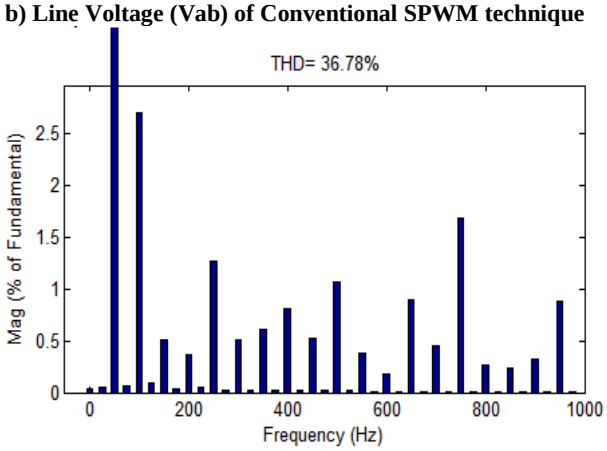


Fig. 5 a) Phase voltage (Van) of conventional SPWM technique.



b) Line Voltage (Vab) of Conventional SPWM technique



c) Frequency spectrum of inverter line voltage of conventional SPWM technique.

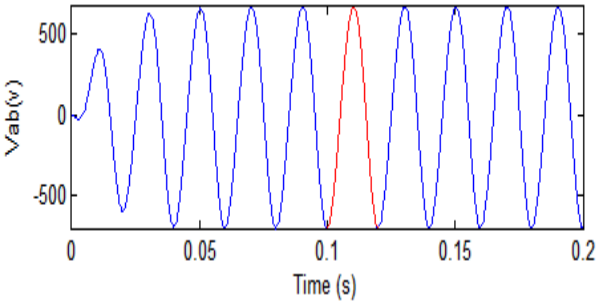
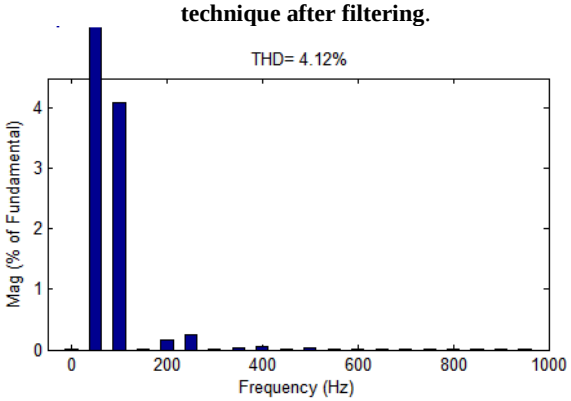


Fig. 6 a) Load voltage (Vab) of conventional SPWM technique after filtering.



b) Frequency spectrum of Inverter line voltage with conventional SPWM technique after filtering.

It is clear that, based on controlling the parameters of PI regulators at dc side and load voltage side, this technique effectively reduces the THD and switching losses for the same switching frequency. Load voltage (after filter) is almost same in both the cases in terms of its magnitude and THD. Both load voltages, THD's are found within 5% limit imposed by IEEE 519-1992 standard.

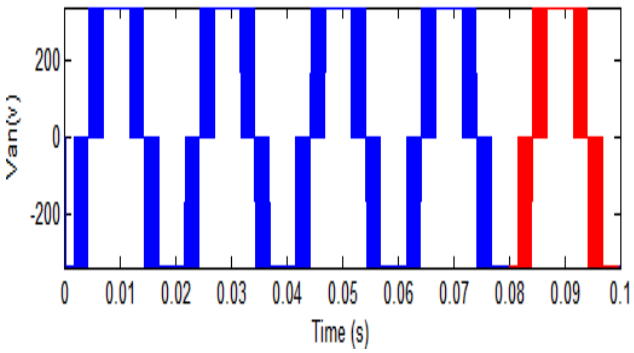
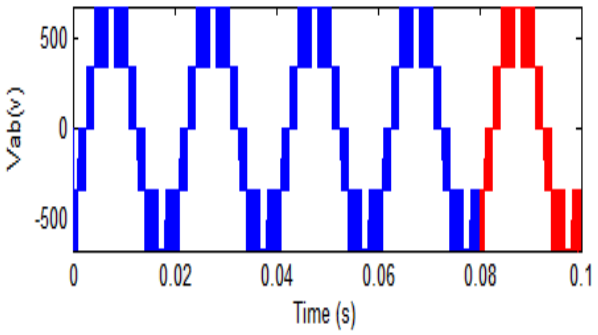
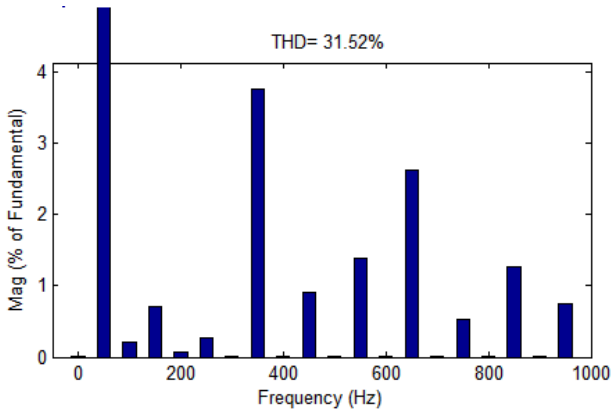


Fig. 7 a) Phase voltage (Van) of proposed control PWM technique.



b) Line voltage (Vab) of proposed control technique



c) Frequency spectrum of inverter line voltage with proposed control scheme.

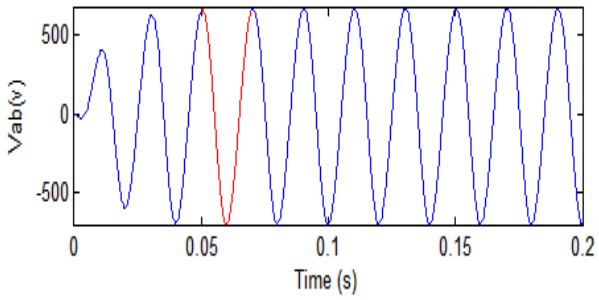
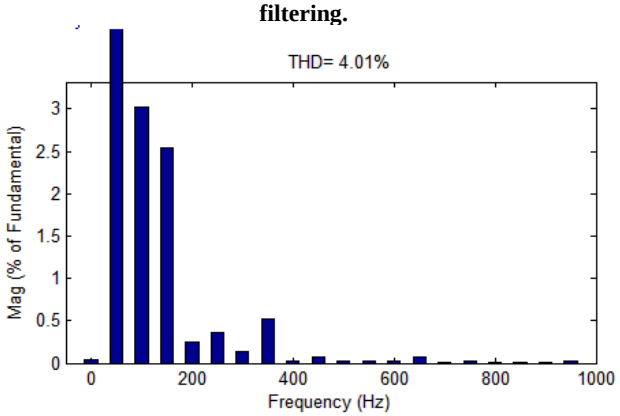


Fig. 8 a) Load voltage (Vab) of proposed technique after filtering.



b) Frequency spectrum of inverter line voltage with proposed control scheme after filtering.

Comparison of switching losses of conventional and proposed technique of three level inverter are made based on various carrier frequencies which prove that the proposed closed loop control technique effectively reduces the switching losses of three level diode clamped inverter. Table .3 shows the switching losses of conventional and proposed technique based on various carrier frequencies.Table.4 shows the comparative analysis of proposed carrier based PWM technique and SVPWM technique

Table 3. Switching losses of conventional and proposed technique based on various carrier frequencies

Carrier frequency (Hz)	Switching loss P_{sw} (w) – conventional Method	Switching loss P_{sw} (w) – proposed method
1000	144.5	125.23
2000	158.95	138.12
3000	170.9	154.7
4000	183	167.5
5000	202.3	176.8

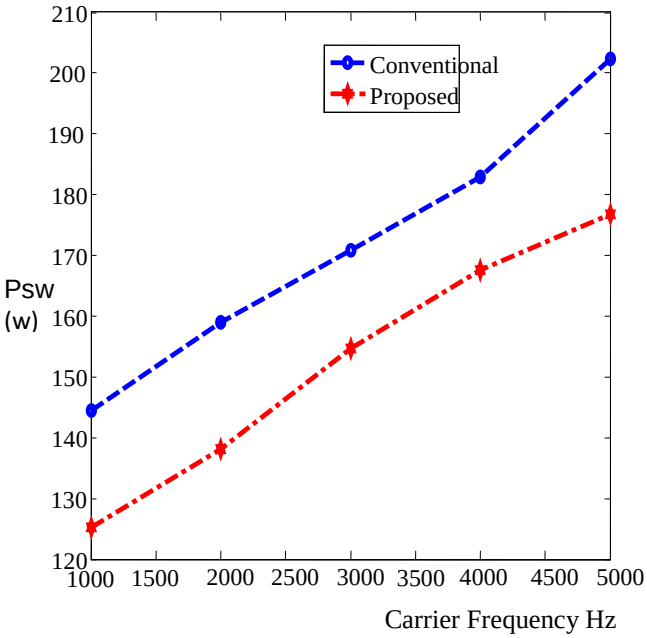


Fig. 9 Variation of switching loss Psw versus carrier frequency

From the graph, it is clear that switching losses of proposed closed loop control technique are minimized when compared to the conventional SPWM technique for various carrier frequencies. This effectively validates the minimization of switching loss of the proposed technique.

Table 4. Comparative analysis between proposed carrier based PWM techniqueand space vector PWM technique

Parameters	Proposed carrier based PWM technique	Space vector based PWM
Controlling common mode voltage	Controllable	Complicated
Compensation of unbalanced dc sources	Compensated	Uncompensated
Implementation	Simple	Complex
Controlling more number of levels	Applicable to any number of levels	Complexity increases with more number of levels
Total harmonic Distortion(THD)	Less compared to SVPWM technique	More
Switching losses	Less	More

5. CONCLUSION

A carrier based closed loop PWM technique has been proposed using SPWM technique, based on stopping the switching pulses for some duration within each positive and negative half cycle of voltage wave to further reduce the THD and switching losses. Simulated results have been presented to validate the effectiveness of the proposed technique. THD contents in inverter output voltages are also found within 5% specified limit imposed by IEEE 519-1992 standard in simulation results. Graph clearly shows the minimization of switching losses based on proposed control technique compared to conventional SPWM technique. The obtained results are comparable with the space vector PWM-based switching loss reduction technique [7] without any complex calculations involved in switching state estimation.

6. FUTURE WORK

The future work of this paper can be extended for balancing the neutral point potential (NPP) in diode clamped multilevel inverter by using the same carrier based PWM technique and can also be extended for drives and renewable energy applications.

7. REFERENCES

[1] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point clamped PWM inverter," IEEE Trans. Ind. Applicat., vol. IA- 17, pp. 518–523, Sept./Oct. 1981.

[2] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: " A survey of topologies, controls, and applications," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 724–738, Aug. 2002.

[3] Leon M. Tolbert, Fang Zheng Peng, and Thomas G.Habetler, " Multilevel Converters for Large Electric Drives" , IEEE Trans. Ind. Electron., VOL. 35, NO. 1, jan/feb. 1999.

[4] Jose Rodriguez, Steffen Bernet , Peter K. Steimer and Ignacio E. Lizama, "A Survey on Neutral-Point-Clamped Inverters", IEEE Trans. Ind. Electron, vol. 57, no. 7, pp. 2219-2230, july 2010.

[5] Peter, K., Lenke, R.U., Schroder, S., Doncker, R.W.D. "Design of a flexible control platform for soft-switching multilevel inverters", IEEE Trans. Power Electron,vol. 2, no.5, pp. 1778– 178, 2007.

[6] Luigi, M., Paolo, T., Toigo, V.: "Space vector control and current harmonics in quasi-resonant soft-switching PWM conversion", IEEE Trans. Ind. Appl.,vol. 32, no. 2, pp. 269–278, 1996.

[7] Lei, L., Yunping, Z., Jie, Z., Xudong, Z.:" Digital implementation of diode clamped three level SVPWM inverter". Proc. PEDS, vol. 2, pp 1413–1417, November 2003.

[8] Chaturvedi, P.K.,Jain, S., Agarwal, P.: 'Switching losses and harmonic investigations in multilevel inverters', IETE J. Res., vol. 54, no.4, pp. 295–305, 2008.

[9] Ned, M., Undeland, T.M.,Robbins,WP:"Power electronics converters, applications and design" (John Willey & Sons, 2001, 3rd edn.)

[10] Rashid, M.H.:"Power electronics handbook" (Academic Press, New York, 2001, 3 rd edn.)

[11] Paul C. Krause, Oleg Wasynczuk, Scott. Sudhoff, 'Analysis of Electric machinery and Drive (Wiley & sons , 2002, 2nd edn).