# Single Electron 2-Bit Multiplier

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## ABSTRACT
A Single Electron 2 bit multiplier is presented in this paper. Modern techniques of lithography make it possible to confine electrons to sufficiently small dimensions that the quantization of both their charge and their energy are easily observable. When such confined electrons are allowed to tunnel to metallic leads a single electron transistor (SET) is created. This transistor turns on and off again every time one electron is added to the isolated region 2 bit multiplier performs multiplication through a series of additions. For example, suppose we want to multiply 2 * 1. Instead of building a multiplier circuit, we can instead use an adder and perform 2 * 1 by adding 1 + 1. The first number indicates how many times the second number is added to itself. The adder which is used to build the 2 bit multiplier circuit is designed using single electron transistor. The logic operation of 2 bit multiplier is verified using simulation software "SIMON2.0".

**Keywords** - single electron transistor; half adder; quantum dot; tunnel junction; Coulomb blockade.

## 1. INTRODUCTION
Multipliers have an important effect in designing arithmetic processors. The Single Electron Tunnelling (SET) technology is the most promising future technology generations to meet the required increase in density and performance and decrease in power dissipation [1]. The main device of the SET circuits is the tunnel junction through which individual electrons can move in a controlled manner [2]. In this paper, we first briefly discuss the basic physics of SET. We review some of the Single Electron Circuit basic building blocks that were introduced in the literature. The full design and simulation results (using the famous simulator SIMON 2) are included. A novel XOR SEC is introduced. The full design and SIMON simulation results of the developed XOR SEC are presented. It is worth noting here that the developed XOR SEC can be used as a half-adder SEC [3-6].

Single electron based logic gates have already been constructed with binary decision diagram (BDD) with clock pulses of 1ns each. The technique of tunnelling of an electron is utilized for those gates. This technique is used to design the complex logical circuit 2 bit binary multiplier**.** For easily understanding the operation of some of the single electronic gates having different number of inputs has been depicted. Single Electron Tunnelling devices exploit effects that arise due to the quantized nature of charge. These effects have been observed in systems of small metal structures in semiconductors structures and in structures made from conducting polymers. Because these effects are omnipresent in small structures, they are likely to have an impact on any future Nano-scale electronic circuits. These devices are able to use in low power circuits as only a few electron is needed for carrying information the logic circuit of the 2 bit binary multiplier which is designed using the Single electron Transistor is depicted here.

## 2. THE BASIC PHYSICS OF SET
The main component of SEC is the tunnel junction that can be implemented using silicon or metal-insulator-metal structures, GaAs quantum dots, etc. The tunnel junction can be thought of as a leaky capacitor [7].For very small tunnel junctions (hence, very small capacitance $\mathbf{C_J}$), the movement of only one electron, from one side of the tunnel junction to the other, may produce a noticeable change e/C of the voltage across the tunnel junction. Note that the above $C = C_J + C_6$ where $C_6$ is the equivalent capacitance of the remainder of the circuit, as viewed from the tunnel junction's perspective [8-10].

## 3. 2-BIT MULTIPLIER
In this section you will build a 2-bit multiplier circuit that performs multiplication through a series of additions. For example, suppose we want to multiply 2 * 1. Instead of building a multiplier circuit, we can instead use an adder and perform 2 * 1 by adding 1 + 1. The first number indicates how many times the second number is added to itself. Alternatively, suppose we want to perform 3 * 3, this multiplication can again be computed by adding 3 + 3 + 3.

### 3.1 Binary Implementation of Two Bit Multiplier

```
   10   (this is 2 in binary)
 X 11   (this is 3 in binary)
 ======
   10   (this is 10 x 1)
+ 10    (this is 10 x 1, shifted one position to the left)
=========
  110   (this is 6 in binary)     (see Figure 1)
```

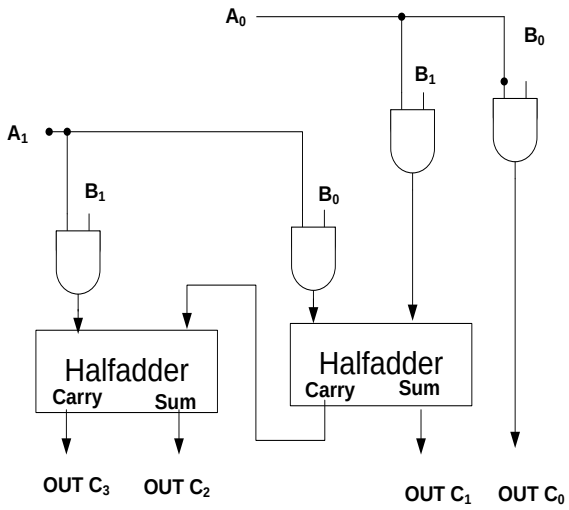



**Fig 1: 2-bit multiplier Logic Diagram**

# 4 BASIC ELEMENTS OF 2 BIT MULTIPLIER

- AND Gate
- OR Gate
- HALF ADDER

## 4.1 AND Gate

The AND gate is a digital logic gate that implements logical conjunction - it behaves according to the truth table to the right. A HIGH output (1) results only if both the inputs to the AND gate are HIGH (1). If neither or only one input to the AND gate is HIGH, a LOW output results. In another sense, the function of AND effectively finds the minimum between two binary digits, just as the OR function finds the maximum. The Single electron AND gate is shown in Fig.1. The circuit comprises eight islands bounded by five tunnel junctions.

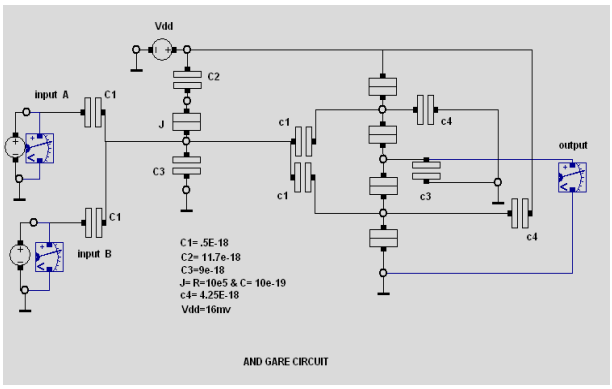



**Fig 2: AND Gate**

## 4.2 OR Gate

The OR gate is a digital logic gate that implements logical disjunction - it behaves according to the truth table to the right. A HIGH output (1) results if one or both the inputs to the gate are HIGH (1). If neither input is HIGH, a LOW output (0) results. In another sense, the function of OR effectively finds the maximum between two binary digits, just as the complementary AND function finds the minimum. The Single electron OR gate is shown in Fig.2. The circuit comprises eight islands bounded by five tunnel junctions.

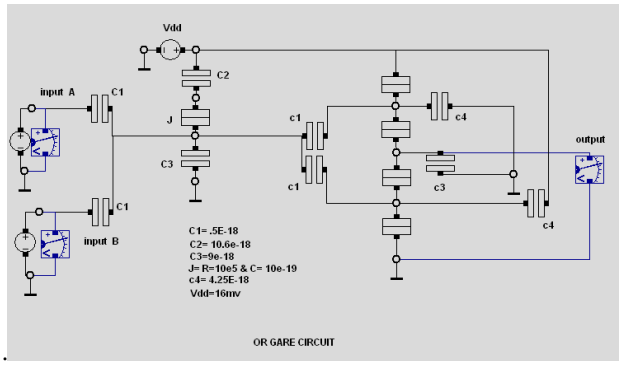



**Fig 3: OR Gate**

## 4.3 HALF ADDER

A half adder is a logical circuit that performs an addition operation on two one-bit binary numbers often written as *A* and *B*. The half adder output is a sum of the two inputs usually represented with the signals $C_{out}$ and *S* where, Sum=2*$C_{out}$ +S
Half-adder circuit is combination of AND gate and OR gate, is shown in Fig. 3.The Single electron half-adder circuit comprises ten islands bounded by six tunnel junctions.

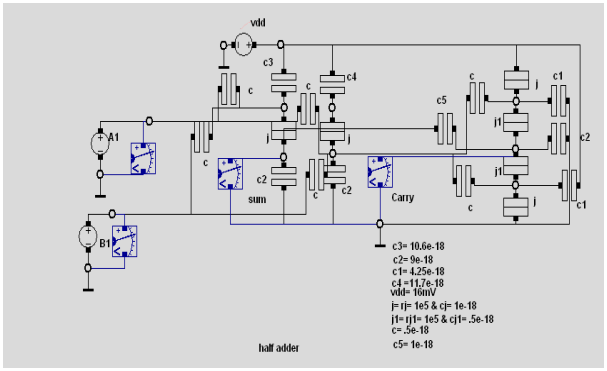



**Fig 4: Half Adder**

# 5. SINGLE ELECTRON 2-BIT MULTIPLIER

The single electron 2 bit multiplier is shown in Fig. 5. The circuit comprises of 28 islands $N_1$, $N_2$, $N_3$….$N_{28}$ bounded by 16 tunnel junctions. The capacitance of J junctions is $0.1x10^{-18}$F and their resistances are $1x10^5$ Ohm. The capacitance of $J_2$ Junctions is $0.5x10^{-18}$F and their resistance is $1x10^5$ Ohm. The voltage $V_{dd}$ is constant and its value 16 mV.

As shown in Table 1.The voltage sources $A_0$ $A_1$ $B_0$ $B_1$ are the inputs of 2 bit multiplier and can take only two values. 0V corresponds to logic '0' and 15mV which corresponds to logic '1'. The input value $A_1$ is applied to nodes $N_5$ and $N_8$ through capacitors C ie. $0.5x10^{-18}$F, the input value $A_0$ is applied to nodes $N_1$ and $N_3$ through capacitors C ie. $0.5x10^{-18}$F, the input value $B_1$ is applied to nodes $N_3$ and $N_7$ through capacitors C.

$0.5x10^{-18}$F and the input voltage $B_0$ applied to the nodes $N_1$ and $N_5$ through capacitors C ie. $0.5x10^{-18}$F. The output signals of the 2 bit multiplier are taken from nodes $N_2$, $N_{20}$, $N_{22}$ and $N_{17}$ whose product values are $C_0$, $C_1$, $C_2$ and $C_3$ respectively .The presence of positive charge corresponds to logic '1' and no charge corresponds to logic '0'.Input and Output is shown in Fig.6 &Fig.7 respectively.

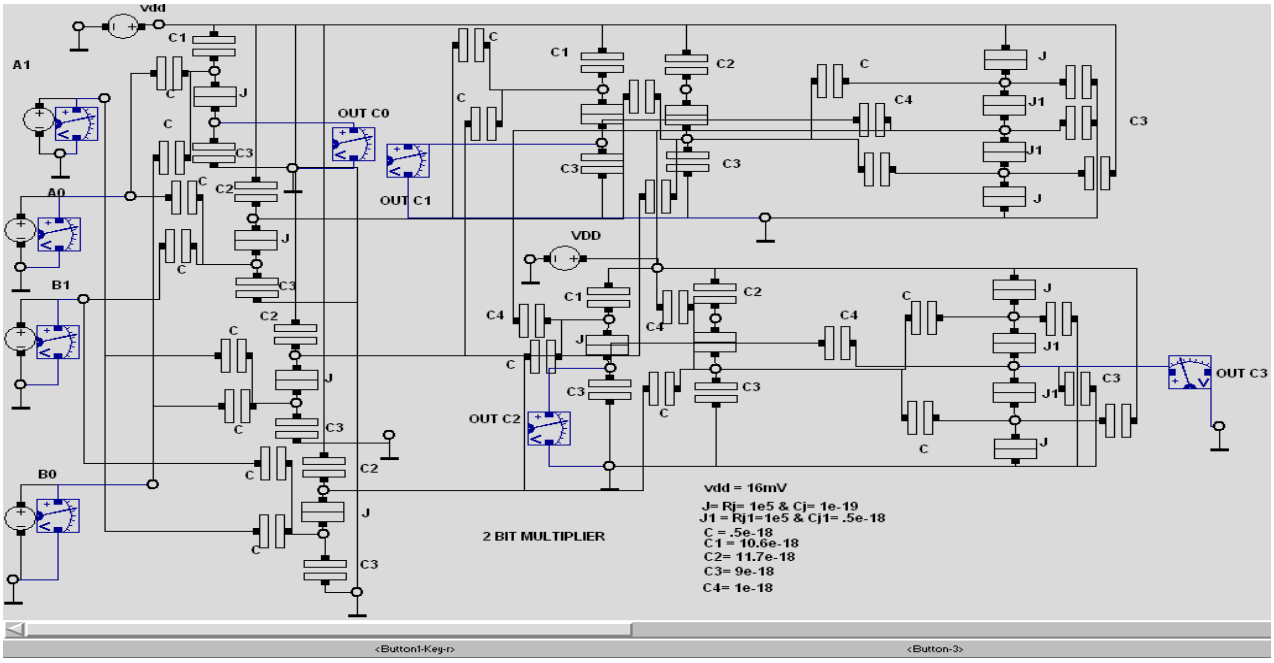
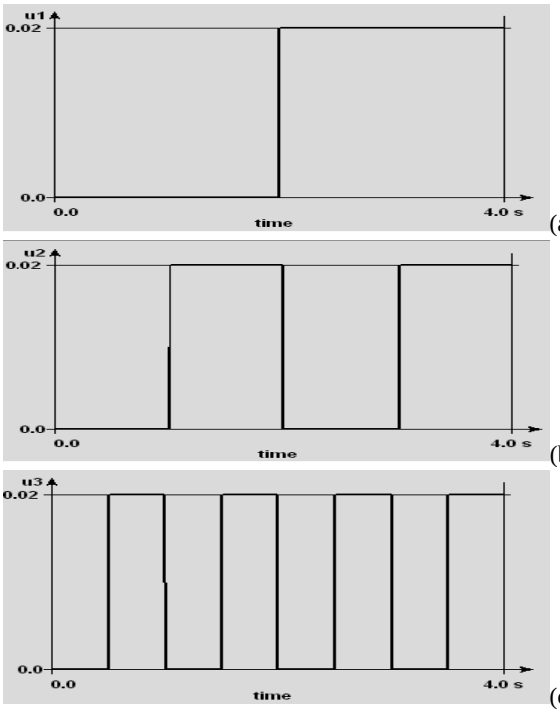
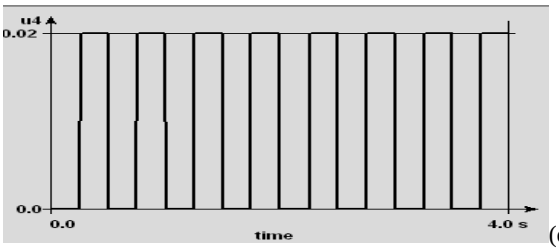



**Fig 5: Internal Circuit of 2 Bit Multiplier**

**Table 1. Truth Table**

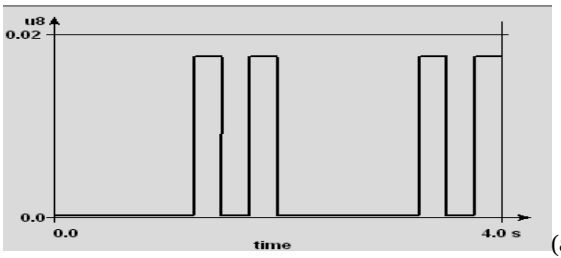
| INPUT A | | INPUT B | | OUTPUT | | | |
|---|---|---|---|---|---|---|---|
| $A_1$ | $A_0$ | $B_1$ | $B_0$ | $C_3$ | $C_2$ | $C_1$ | $C_0$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |



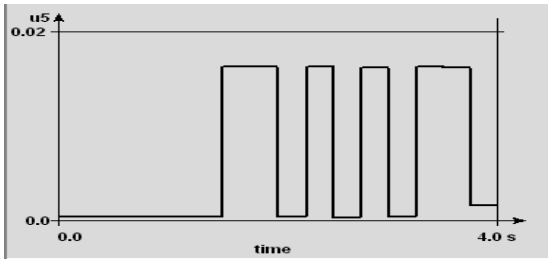



(d)

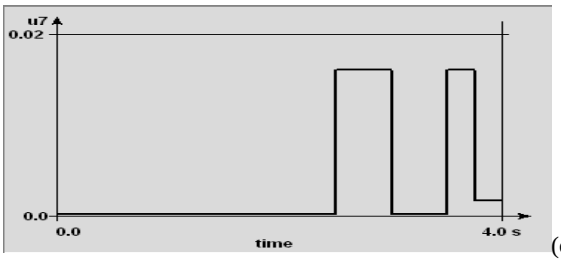
**Fig 6: Simulated input (a) $A_1$ voltage versus time (b) $A_0$ voltage versus time (c) $B_1$ voltage versus time (d) $B_0$ voltage versus time**



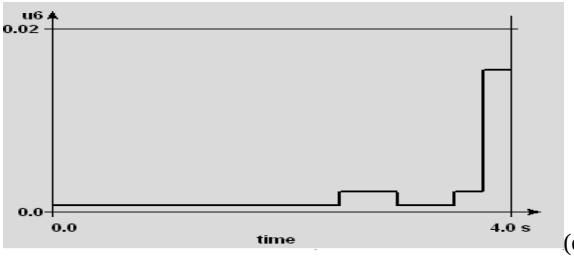

(a)




(b)




(c)




(d)

**Fig 7: Simulated output (a) OUT $C_0$ voltage versus time (b) OUT $C_1$ voltage versus time (c) OUT $C_2$ voltage versus time (d) OUT $C_3$ voltage versus time**

## 6. CONCLUSION

The design and simulation of the single electron 2 bit multiplier was presented in this document .The circuit multiplies a pair of 2 bit inputs and produces their product OUT $C_0$ , OUT $C_1$ , OUT $C_2$ and OUT $C_3$ .The circuit comprises 16 tunnel junctions , forty two capacitors and twenty two islands .each output is an island and the presence of positive charge on it corresponds to the logic '1', whereas the absence of charge corresponds to the logic 0 . The energy history diagram and stability plot showed that the circuit operates in stable regions. Further this multiplier can be implemented in filters for image processing applications. Due to the increase in speed of multiplier and high reduction in power dissipation it can be used for DSP applications.

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