Biphase Amplifier based Precision Rectifiers using Current Conveyors

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ABSTRACT
A novel and simple circuit for precision rectifier using second-generation current conveyor (CCII) is presented in this article. The circuit basically uses a CCII-based voltage mode bi-phase amplifier, which has been used as full-wave and half-wave rectifiers. To switch the bi-phase amplifier from non-inverting to inverting mode, a MOSFET and a CCII-based comparator has been used. The circuit exhibits precision rectification over a wide range of operation and can also be implemented using commercially available ICs such as the AD844. The proposed circuits have been simulated using CMOS implementation of current conveyor with effective results.

General Terms
Analog Signal Processing, Electronic Circuits

Keywords
Current conveyors, bi-phase amplifier, precision rectifiers, DVCC

1. INTRODUCTION
Precision rectifiers form an important building block in non linear analog processing systems. In such rectifiers, the threshold voltages associated with diodes are overcome and hence enable the rectification at relatively low signal levels required for signal processing applications. With the advent of current conveyors, which offer a number of advantages over other devices, many precision rectifiers using current conveyors have been recently reported in literature [1-16]. However, many of them use a complex circuitry [6-9]. In this paper, novel precision rectifiers using Second-Generation Current Conveyor (CCII) and Differential Voltage Current Conveyor (DVCC) based bi-phase amplifier are presented. The bi-phase mode of the amplifier is controlled with the help of an additional voltage controlled switch and a comparator to achieve half-wave and full-wave rectification. The proposed precision rectifier offer features such as simpler hardware and a wide frequency range of operation. Non-ideal and parasitic study of the proposed circuits is also performed. The circuit proposed is designed and verified using PSPICE.

2. CIRCUIT DESCRIPTION
The second-generation current conveyor (CCII) symbol is shown in Fig.1, which is characterized by

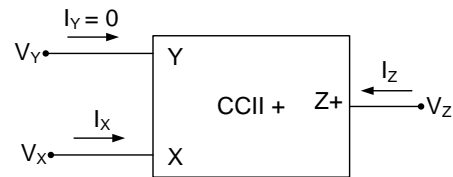$$V_X = V_Y \ , \quad I_Y = 0 \quad , \quad I_{Z+} = I_X \qquad (1)$$

Fig 1: The symbol of CCII

The CMOS implementation of the CCII along with a buffer is given in Fig. 2, while the realized bi-phase amplifier is shown in Fig. 3.
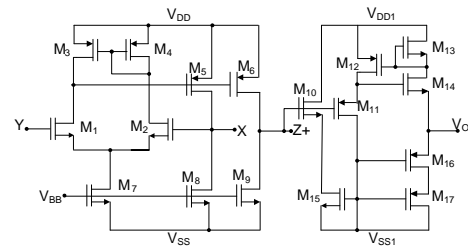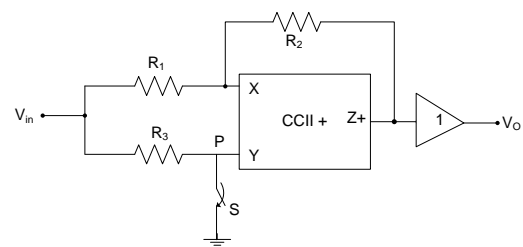

Fig 2: The CMOS structure of the CCII with buffer

Fig 3: CCII based bi-phase amplifier

The amplifier uses a voltage-controlled switch *S*. When *S* is open, the output voltage V_0 can be expressed as:

$$V_O = V_{in} \qquad (2)$$

When *S* is closed, the voltage at node *P* is zero. Now by selecting $R_2=2R_1$ the output voltage becomes:

$$V_O = -V_{in} \qquad (3)$$

Thus from equations (2) and (3), it is clear that the circuit of Fig.2 realizes a bi-phase amplifier. To realize a precision rectifier, the switch *S* of the bi-phase amplifier has been

realized with a P-MOS transistor along with CCII+ based non-inverting comparator as shown in Fig. 4.
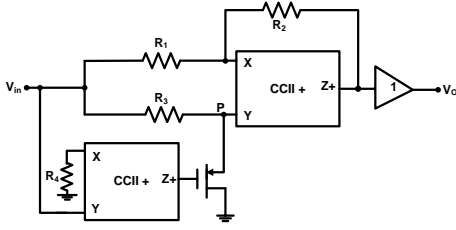

Fig 4: Proposed precision rectifier circuit-I

2.1 Additional precision rectifier circuit

The circuit presented in this section is a modified form of the circuit shown in Fig. 3. This modified circuit employs a DVCC-based biphase amplifier. Further, the switch of the biphase amplifier is also realized using a DVCC-based comparator and a NMOS transistor. The symbol of a DVCC with only a Z+ output is shown in Fig. 5 [17], which is characterized by the following port relationship.

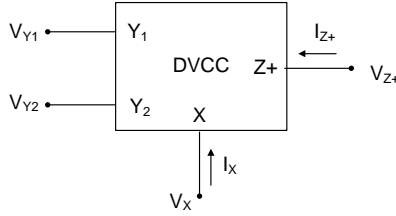$$V_X = V_{Y1} - V_{Y2} \ , \quad I_Y = 0 \ , \quad I_{Z+} = I_X \qquad (4)$$

Fig 5: Symbol of DVCC

The DVCC-based precision rectifier is shown in Fig.6. Here, DVCC ② is used as a comparator [17]. During the positive half of the cycle, the comparator output is low and the switch is open thus leading to $V_0 = V_{in}$. During the negative half of the cycle, the comparator output is high; the switch is closed, and thus the bi-phase amplifier behaves in an inverting mode resulting in $V_0 = -V_{in}$. As a result, full-wave rectification is achieved. The advantage of this circuit over the previous circuit (shown in Fig. 4) is that one passive resistance R_4 is eliminated and the PMOS transistor is replaced by an NMOS transistor which is suitable for IC fabrication in terms of area.
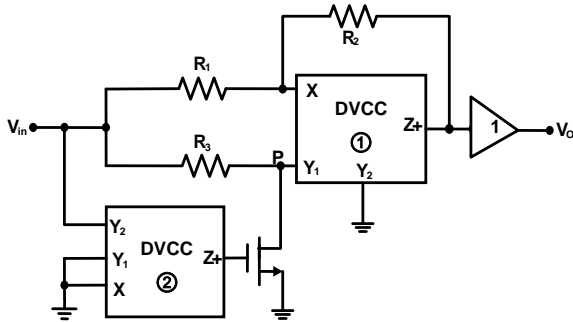

Fig 6: Proposed precision rectifier circuit-II

3. NON-IDEAL ANALYSIS

3.1 Effect of transfer gain

A non-ideal CCII is characterised by

$$V_X = \beta V_Y \ , \quad I_Y = 0 \ , \quad I_{Z+} = \alpha I_X \qquad (5)$$

where β is the voltage transfer gain from Y to X and α is the current transfer gain from X to Z+. Re-analysis of the first proposed circuit of Fig. 4 using equation (5) yields the following relation:

During the positive half cycle:

$$\frac{V_{0,n}}{V_i} = \frac{R_2}{2R_1}\left[\frac{\beta_{11} + 3\beta_{11}\alpha_{11} - 2\alpha_1}{1 + \alpha_1}\right] \qquad (6)$$

During the negative half cycle:

$$\frac{V_{0,n}}{V_i} = -\frac{R_2}{R_1}\left(\frac{\alpha_1}{1 + \alpha_1}\right) \qquad (7)$$

Selecting $R_2 = 2R_1$, equations (6) and (7) reduce to:

$$\frac{V_{0,n}}{V_i} = \left[\frac{\beta_{11} + 3\beta_{11}\alpha_{11} - 2\alpha_1}{1 + \alpha_1}\right] \qquad (8)$$

$$\frac{V_{0,n}}{V_i} = -2\left(\frac{\alpha_1}{1 + \alpha_1}\right) \qquad (9)$$

It is to be further noted that equations (8) and (9) reduce to equations (2) and (3) respectively for $\alpha_1 = \beta_{11} = 1$.

3.2 Effect of Parasitics

A CCII is characterised by the following parasitic port impedances: The parasitics are R_X, $R_Y//C_Y$ and $R_Z//C_Z$ for X- ,Y- and Z ports respectively. Considering the X- and Y-terminal parasitics, the output voltage during the positive half cycle can be expressed as:

$$\frac{V_0^{'}}{V_i} = -\frac{R_2 - R_X}{(2R_1 + R_X)}\frac{\left[s + \dfrac{1}{C_Y R_Y} - \dfrac{(2R_1 + R_X)}{C_Y R_3(R_2 - R_X)}\right]}{s + \dfrac{R_3 + R_Y}{C_Y R_3 R_Y}} \qquad (10)$$

For a typical design $R_3 << R_Y$ thus $R_3//R_Y \simeq R_3$. By selecting $R_2 = 2R_1$, equation (10) reduces to:

$$\frac{V_0^{'}}{V_i} = -\frac{(2R_1 - R_X)}{(2R_1 + R_X)}\frac{\left[s + \dfrac{1}{C_Y R_Y} - \dfrac{(2R_1 + R_X)}{C_Y R_3(2R_1 - R_X)}\right]}{s + \dfrac{1}{C_Y R_3}} \qquad (11)$$

During the negative half of the cycle the output voltage can be expressed as:

$$\frac{V_0^{'}}{V_i} = -\frac{(2R_1 - R_X)}{(2R_1 + R_X)}\frac{\left[s + \dfrac{1}{C_Y r_{on}} - \dfrac{(2R_1 + R_X)}{C_Y R_3(R_2 - R_X)}\right]}{s + \dfrac{R_3 + r_{on}}{C_Y R_3 r_{on}}} \qquad (12)$$

where r_{on} is the ON resistance of MOSFET.

Again, in equation (12) $r_{on} << R_3$ thus $r_{on}//R_3 \simeq r_{on}$. By selecting $R_2 = 2R_1$, equation (12) reduces to:

$$\frac{V_0^{'}}{V_i} = -\frac{(2R_1 - R_X)}{(2R_1 + R_X)}\frac{\left[s + \dfrac{1}{C_Y r_{on}} - \dfrac{(2R_1 + R_X)}{C_Y R_3(2R_1 - R_X)}\right]}{s + \dfrac{1}{C_Y r_{on}}} \qquad (13)$$

Closer inspection of equations (11) and (13) for a typical design shows that the gain of the rectified output is not affected. The pole and zero introduced due to parasitics are found to be symmetrical and approximately equal in magnitude, thus they may be the cause for certain phase errors. It is also to be noted that for open-switch as well as for closed-switch conditions (equation (11) and (13)), the path from port Y to ground will contain R_Y or $R_Y//r_{ON}$ respectively. Therefore both equations (11) and (13) show a 'minus' sign.

4. DESIGN AND VERIFICATION

To verify the proposed theory, the precision rectifier of Fig. 4 is designed and simulated using PSPICE. The model parameters for the CMOS CCII are taken from MIETEC 0.5 µm CMOS process [18]. The PMOS switch is implemented with the *W/L* ratio as 7 µm /0.35 µm. For a bi-phase amplifier, selecting $R_1 = 1K\Omega$ leads to $R_2 = 2K\Omega$. R_3 and R_4 are selected as 150KΩ and 400Ω respectively. The supply voltages are taken as $V_{DD} = - V_{SS} = 2.5V$ and $V_{BB} = -1.96V$. The MOS transistors aspect ratios for the CMOS CCII are given in Table 1. The resulting DC transfer characteristics of the proposed precision rectifier are shown in Fig.7. Its performance is also verified with a sinusoidal input of 20mV peaks at 10 KHz, 100 KHz and 1 MHz, the results of which are depicted in Fig.8-10.

The proposed circuit of Fig. 6 is designed with $R_1 = 2K\Omega$, $R_2 = 4K\Omega$ and $R_3 = 40K\Omega$. The supply voltages are kept as before. The NMOS transistor aspect ratio is 10 µm /0.35 µm. The full-wave rectified output at 20mV peaks and at 1 MHz are shown in Fig. 11.

The distortions visible during the clock switching edge at increasing frequencies are mainly due to the switching limitation of the transistor. These may be reduced by employing high frequency transistors.

Table 1. Dimensions of the transistors used in CCII

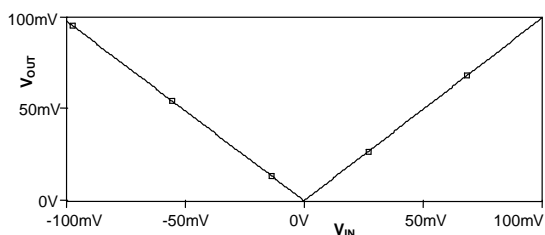| Transistor	W (µm)	L (µm)
M_1, M_2	0.8	0.5
M_3, M_4	4	0.5
M_5, M_6	10	0.5
M_7	14.4	0.5
M_8, M_9	45	0.5

Fig 7: DC transfer characteristics of the precision rectifier
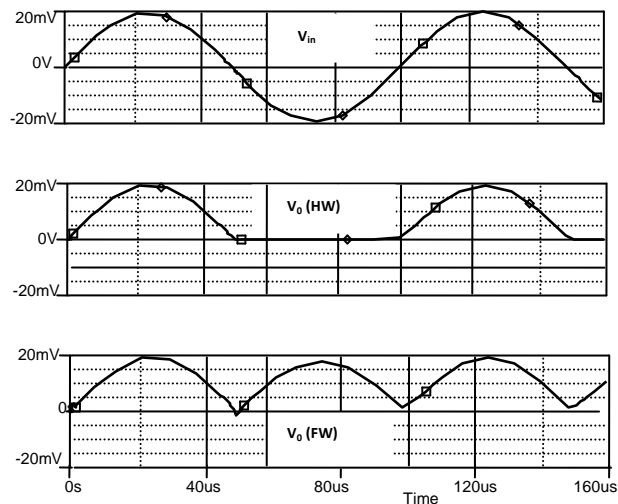

Fig 8: Input and output waveforms at 10KHz of the of the precision rectifier shown in Fig 4.
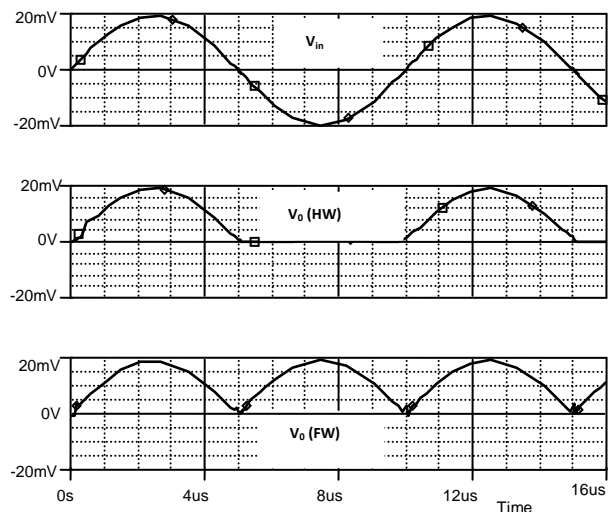

Fig 9: Input and output waveforms at 100KHz of the precision rectifier shown in Fig 4.
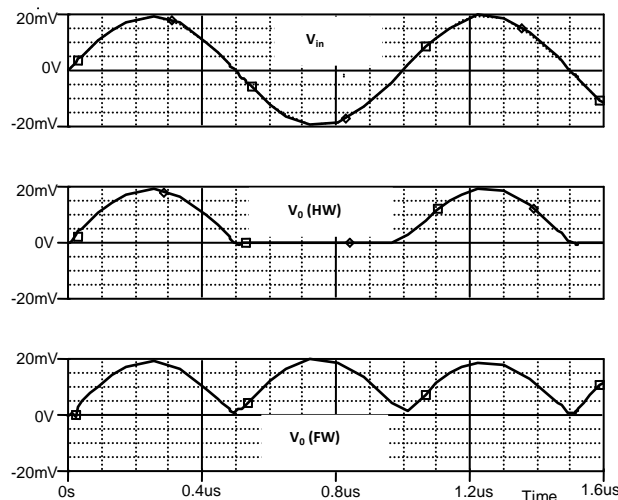

Fig 10: Input and output waveforms at 1MHz of the precision rectifier shown in Fig 4.
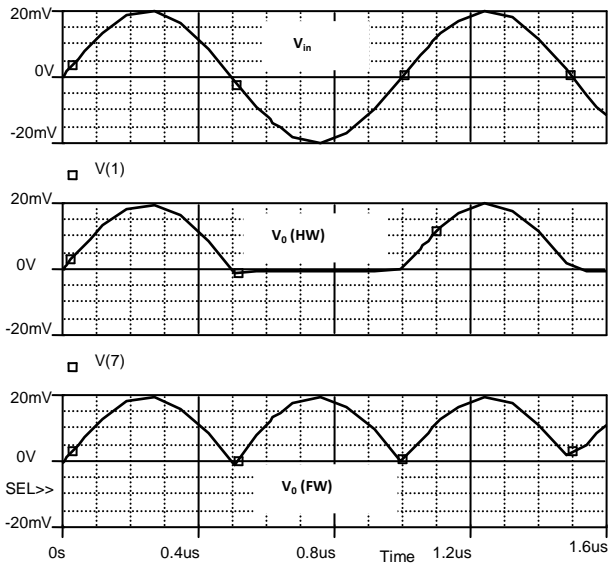
Fig 11: Input and output waveforms at 1MHz of the precision rectifier shown in Fig. 6

5. COMPARATIVE STUDY

The circuits proposed in this work were compared to similar circuits reported in literature. The different parameters used for comparison were:

i. Type of active building blocks used
ii. Number of diodes
iii. Number of resistors
iv. Half-wave and/or full wave capability
v. Operating frequency
vi. Signal (voltage or current) amplitude range

The results are depicted in Table 2. It may be noted that most of the available circuits are based on two current conveyors. There are some works which benefit from using only a single current conveyor or OTA [4, 9, 10, 16]. However one of these [9] exhibits only half-wave rectification. As far as the frequency range is concerned, the circuit proposed by [9] with half wave capability is quite attractive. Similarly the work proposed by [6] also exhibits good frequency performance but employs a number of diodes.

The circuits proposed by [10, 12] exhibit good precision. However the operating frequency for the latter is limited as compared to the former, though it may not be entirely fair to compare these circuits since they fall in the class of tunable precision rectifiers. However, as can be seen, the circuits proposed in this work benefit from a good precision, half wave as well as full-wave operation and a moderate to good operating frequency. Moreover, the new proposed circuits are a novel addition to the already vast literature on the subject

6. CONCLUSION

In this work, a novel precision rectifier using second generation current conveyor is realized. The realized precision rectifier uses a CCII-based voltage mode bi-phase amplifier. To switch the bi-phase amplifier from non-inverting to inverting mode, a MOSFET switch and a CCII based comparator has been used. A DVCC based precision rectifier circuit is further introduced. Non-ideal and parasitic study is also given. The rectifier was designed and verified using PSPICE simulation. The results prove that the circuit achieves half-wave as well as full-wave precision rectification The simulated precision rectifier also exhibits a wide frequency range of operation and uses simple hardware. Improving the performance and high precision capability of the circuit is an area open for further research.

Table 2. Comparison of proposed and existing circuits

Reference No.	Feature					
	(i)	(ii)	(iii)	(iv)	(v)	(vi)
[2]	2 CCII, 2OPAMP	4	2	N/Y	100KHz	± 500mV
[4]	1 FDIO-OTA	4	1	Y/Y	500MHz	±500mV
[6]	2 CCII	4	2	-	30MHz	-
[7]	2CCII	4	2	N/Y	100KHz	±100mV
[8]	1 CCII, 2 OPAMP	2	3	N/Y	100MHz	±1V
[9]	CCII-	-	1	Y/N	100MHz	±25mV
[10]	1 CCII, 2 MOS	-	1 or 0	Y/Y	100KHz	±10mV
[11]	CDTA	4	2	N/Y	5MHz	±50μA
[12]	2 CCII, 2 MOS	-	2	N/Y	20KHz	±20mV
[13]	3 CCCII	-	-	N/Y	100KHz	-
[14]	3 CCII	-	-	N/Y	1MHz	±80μA
[15]	2 CCII, 3 MOS	-	-	-	250KHz	±50mV
[16]	DXCCII, 3MOS	-	-	N/Y	1MHz	±150mV
Proposed (Fig.4)	2 CCII, 1 MOS	-	4	Y/Y	1MHz	±20mV
Proposed (Fig.6)	2 DVCC, 1 MOS	-	3	Y/Y	1MHZ	±20mV

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