FPGA Implementation of Low Complexity VLSI Architecture for DS-CDMA Communication System

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ABSTRACT
The principal goal of this research work is focused on designing and then testing the performance of source and channel coding and decoding circuits implemented on FPGA for Code Division Multiple Access (CDMA) Transceiver using extremely simple circuit concepts. The paper also describes modulation and demodulation circuits for CDMA. The latest technology advancement in cellular mobile communication systems has become more demanding for better quality of service. It requires broad bandwidth for huge quanta of data transfer. CDMA communication system easily meets these requirements of cellular communications. The design of the relevant circuits is based on CDMA approach of direct sequence spread spectrum technology. The functional performance of designed circuits is tested by carrying out simulations using Field Programmable Gate Arrays (FPGA) and Very High Speed Integrated Circuits Hardware Description Language (VHDL) on XILINX ISE® and MATLAB® platforms. The simulated results subsequently have shown quite improved and optimized circuit performance. The performance parameter is mainly based on the number of gates used by CDMA sub-circuits and systems on FPGA implementation.

General Terms
Communication System, VLSI Design, Electronic Circuits Computer and Communication.

Keywords
FPGA, CDMA, Cellular Networks, Quality of Service, Mobile Communication, Direct Sequence Spread Spectrum, VHDL, FPGA.

1. INTRODUCTION
Due to inherent property of better noise immunity and other advantages, the signal processing for communication systems is performed in modern times almost entirely in digital domain which requires high throughput. One such example is CDMA communication system. It requires an efficient design and testing of its subsystems of PN-sequence generator, spectrum spreading and de-spreading digital circuits and digital modulator and demodulator modules which give high throughput. Keeping high processing speed is another big challenge for developing such a system. Such a design of multistage detector and low complexity multistage detectors is particularly useful [1]. Simpler and dedicated hardware circuits can only provide the high speed processing capability to meet these contrasting requirements [2]. The parallel processing capability of FPGA based Programmable Logic Devices (PLDs) makes them ideally suitable for baseband / Radio Frequency (RF) digital signal processing in CDMA applications [3]. The choice of CDMA is based on the fact that allocating channel resources using spread spectrum techniques have number of advantages compared to Frequency Division Multiple Access (FDMA) or Time Division Multiple Access (TDMA) schemes [4]. By spreading the spectrum of the data to be transmitted with orthogonal codes, the receiver can decode each user's data uniquely, even though many users share the same spectral and temporal channel resources [5].

The problem is, therefore, to design hardware based CDMA communication system which works on the principles of direct sequence spread spectrum technology. The design must be easy to use, better in performance and highly efficient. The high speed and simplicity of circuits are always desirable in digital systems [6]. This makes them suitable for low power applications and has simpler and smaller circuit size. The design solution should also provide high throughput and high speed data transfer which can be directly used for providing quality of service to cellular mobile communication [7]. A design modeled by using VHDL and FPGA often has both speed and area advantages over a functionally equivalent software based designs that does not use actual hardware for experiments and tests. It, therefore, is very important to further implement on FPGA during research period of such designs for above mentioned digital systems and circuits [8]. Also, the same design may be implemented for low power applications with different approach but same concept through scalable technology for Ultra Wide Band (UWB).

2. CDMA COMMUNICATION SYSTEM
A cellular communication system in which the bandwidth is shared by all subscribers, each with a different spreading code, is called Code Division Multiple Access (CDMA) system. In other words, a large number of users share a common pool of radio channels and any user can get access to any channel. Different types of cellular systems employ various schemes to achieve this multiple access. The traditional analog cellular systems use Frequency Division Multiple Access (FDMA) and Time Division Multiple Access (TDMA). TDMA and FDMA systems divides each carrier into time slots and frequency slots (channels) and then only one subscriber at a time is assigned to each time slot or channel respectively [9]. On the other hand, CDMA system uses unique digital codes rather than separate RF frequencies

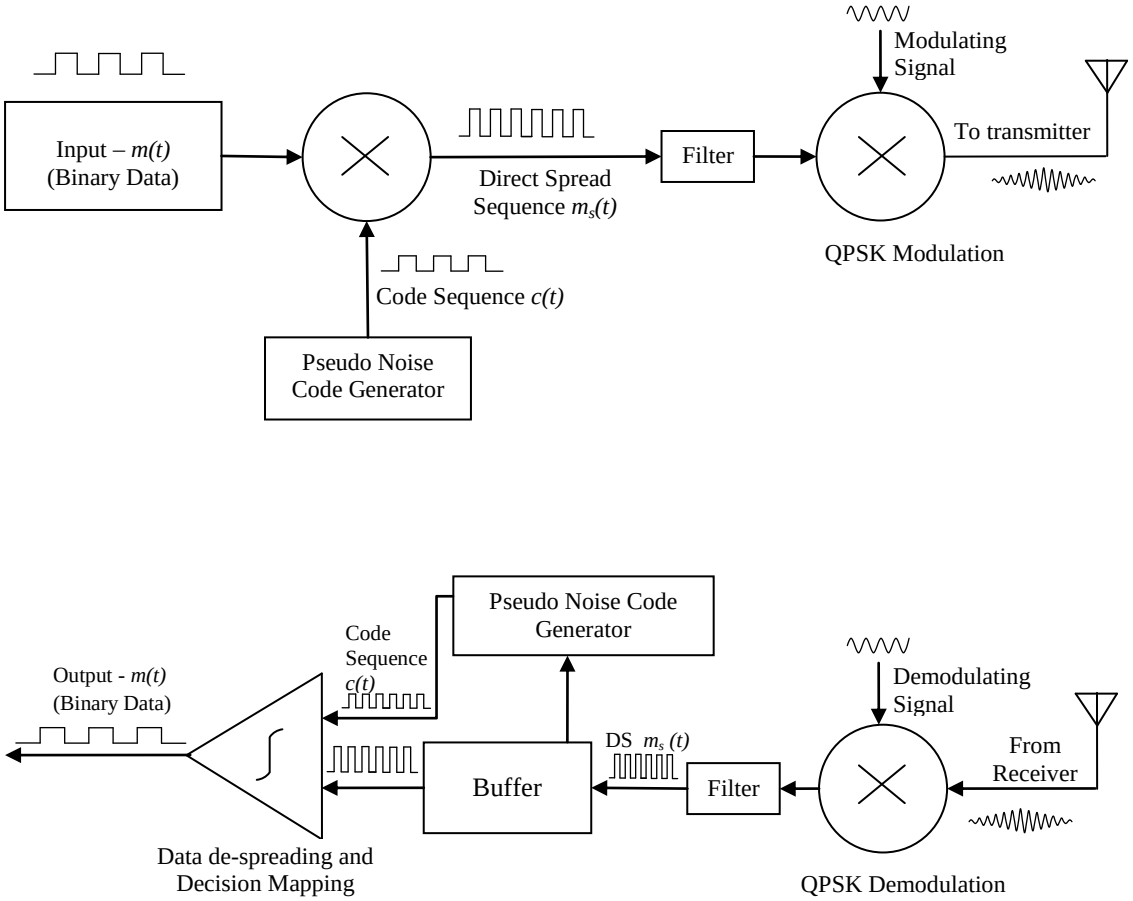

Fig 1: Representative Architecture of CDMA communication transceiver system

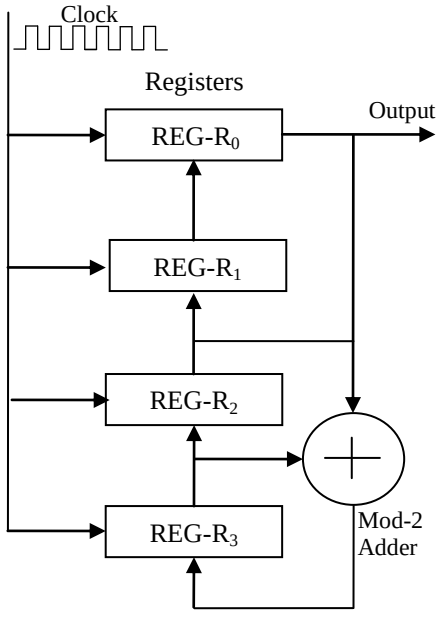

Fig 2: Pseudo noise sequence generator

or channels to differentiate subscribers. The codes are shared by both the mobile station (user) and the base station. These codes are called "Pseudo-Random Code Sequences". All the users share the same range of radio spectrum.

Originally the CDMA was used to jam the communications or to hide the fact that communication is even taking place. This is achieved by spreading the information contained in a particular signal over a much wider bandwidth. In recent times, CDMA has gained widespread international acceptance by cellular radio system operators since it is considered as an advancement and breakthrough in communication technology that has increased both system capacity and service quality.

A CDMA system typically begins with a standard rate of 9. 60 kbps and then it is spread to a typical transmitting rate of 1.23 mbps. Spreading is done by adding a digital code, normally called Pseudo-Noise (PN) sequence, to the data bits associated with users in a cell. At the receiver, the pseudo codes are removed from received signals and a call is received at the rate of 9.60 kbps. Due to wide bandwidth of spread spectrum signal, the possibility of any interference, detection or jamming is greatly reduced. The CDMA, therefore, increases the level of privacy and security. Spreading is the key to increasing the security level in communication systems, as the code of information can be spread over the entire carrier,

which is very hard to detect or intercept [10]. The CDMA systems have merits and demerits as usual with any other

Quadrature Phase Shift Keying (QPSK) and RF carrier signal. The signal is then transmitted through channel where it may

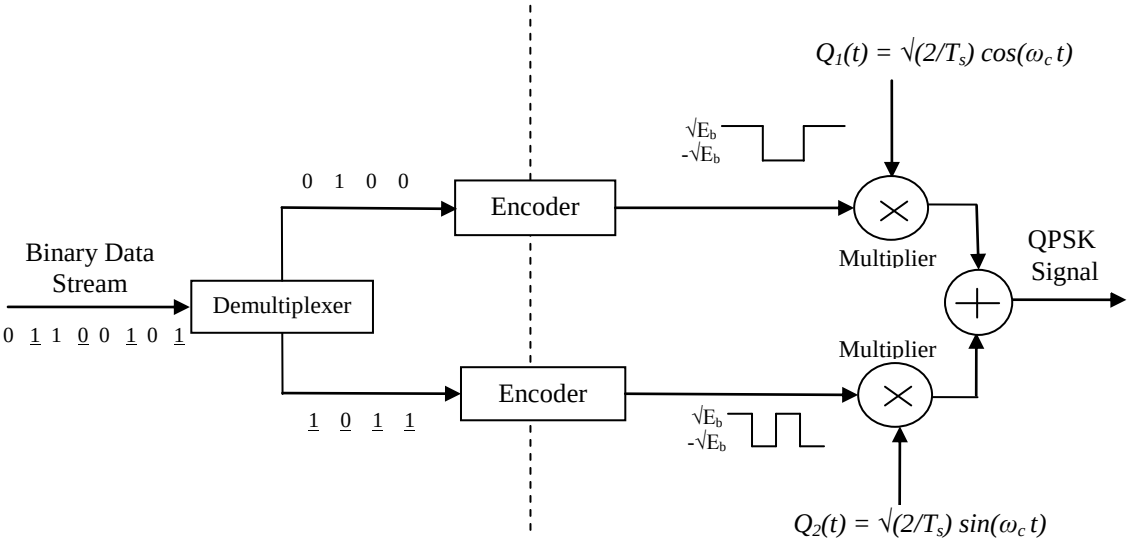

Fig 3: QPSK modulator for direct sequence spread spectrum CDMA

system. These include higher capacity by a factor of 8 to 10 compared to other systems, improved call quality with a better and more consistent performances, simple system planning through the use of the same frequency in every sector, enhanced privacy, coverage area, talk time duration and bandwidth utility. CDMA system, like any other real time system, has limitations as well. These may include that there is a need for very efficient power control to ensure uniform signal strength at the receiving antenna. Failure to this may result in one user swamping all others. Channel pollution may occur when equally dominant signals from many base stations are present at receiving antenna [11]. Hurdles and multiple reflections caused by tall buildings and hills etc.

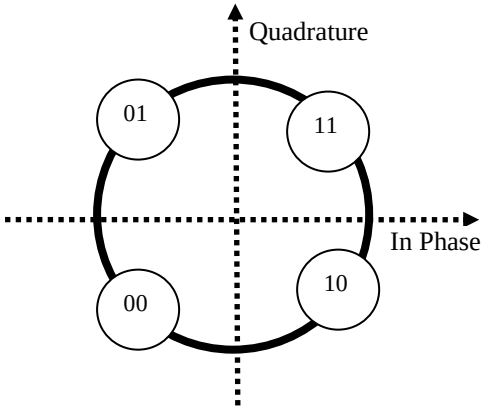

Fig 4: Constellation diagram of QPSK using Gray Coding technique

2.1 Architecture of CDMA Transceiver

A typical block diagram of CDMA transceiver communication system is illustrated in Figure 1. The digital data is first spread by means of PN sequence and then modulated using digital modulation schemes such as

have noise attenuation and other distortions. A distorted signal is then received at receiver. At receiver the signal is first demodulated and then de-spread by using PN codes. Finally original and undistorted signal is reconstructed and received. QPSK has a scheme of self cancellation of inter-carrier-interference, which makes it very robust against noise related distortion in the channel [12].

2.2 PN Sequence for Spread Spectrum

Pseudo Noise (PN) random code sequence is essentially a random sequence of binary numbers. Word 'random' refers to the fact that a bit in the sequence is independent of any of the other bits. The word 'pseudo' refers to that the sequence is deterministic and after *N* elements it repeats itself. The code generator consists of essentially three elements - delay elements, linear combining elements and feedback loop elements.

The delay elements are connected in series. These elements are normally D-flip flops. Some of the outputs of the delay elements are combined in linear combining elements with the outputs of other delay elements and fed back to the input of the first delay element in the series. The implementation of PN sequence generator is usually made up of the linear feedback shift register, which consists of '*n*' master slave D flip-flops. The PN sequence generator produces a predefined sequence of *1's* and *0's*, with *1* and *0* occurring with the same probability. Figure 2 shows one such circuit for generating PN sequence. A non converging condition may arise in the case when the initial input into the first register and the output of the XOR gate are all *0*'s.Under this condition the output of all the register of the PN generator remains as *0* at all instants of time. Therefore it is necessary that the initial input to the PN generator be equal to 1 which is the output of modulo 2 adder. The sequence is generated from Figure 2 using minimal polynomial

$$F(x) = x^3 + x^2 + 1 \qquad (1).$$

2.3 Direct Sequence Spread Spectrum

The bandwidth expansion in spread spectrum is acquired through a coding process, e.g. generation of PN sequence codes, that is independent of the message being sent or the modulation scheme being used. For example, suppose that a digital signal transmission over a Gaussian channel occupy a bandwidth *B* with *SNR = 20 dB* (i.e. 100 in ratio). A channel coding scheme can be used to receive data with small error probability if transmission is carried out at a bit rate less or equal to the channel capacity *C* defined by the Shannon's theorem as given below.

$$C = B \times \log_2(1 + SNR) \qquad (2)$$

Substituting for *SNR* = 20 dB (i.e. 100 in ratio) in equation (2), gives the ratio of bit rate to bandwidth as shown in (3).

$$\frac{C}{B} = \log_2(1+100) = 6.6582 \qquad (3)$$

Now if SNR is reduce to *10 dB* (i.e. 10 in ratio), then referring to the bandwidth-efficiency diagram, the reliable transmission is still possible at the same bit rate but with expanded bandwidth *B'* is given by:

$$\frac{C}{B'} = \log_2(1+10) = 3.4594 \qquad (4)$$

Now consider $B' = \frac{C}{3.4594}$ *and* $B = \frac{C}{6.6582}$ so that the expansion in the bandwidth is given by

$$\frac{B'}{B} = \frac{6.6582}{3.4594} = 1.9246 \qquad thus \;\; B' = 1.9246B$$

The original bandwidth has to be expanded by a factor of about 1.9246 to compensate for the reduction in the channel *SNR*. It can be noted that increasing the transmission bandwidth will increase the amount of the input noise power in a wideband receiver. This is normally countered by using a narrowband receiver to limit input noise.

The spread-spectrum concept has developed from the principle of Shannon's theorem. If data is transmitted at the rate of R_b over a channel occupying a bandwidth much greater than R_b, Shannon's theorem indicates that the reliable communication can be achieved at reduced *SNR*. The spreading of the energy is achieved by phase modulating the input data with the user code sequence. The modulation reduces the high power density of the original data to a low level.

For example, assuming that data is given by *m (t) = [1 0 1 0]* and 15-chip code PN sequence is given by *C(t) = [0010 0011 1101 011]* then baseband spread spectrum data $m_s(t)$ is given by $m_s(t) = m(t) \; \Theta \; C(t)$ = *[0010 0011 1101 011, 1101 1100 0010 100, 0010 0011 1101 011, 1101 1100 0010 100]*. This is simple *XNOR* logical operation between *m(t)* and *C(t)*.

The received signal has to be converted into the original narrowband to limit the amount of input noise accompanying the wideband reception. The conversion is performed at the receiver with the aid of a locally generated PN code sequence causing the spread spectrum to get compressed to original

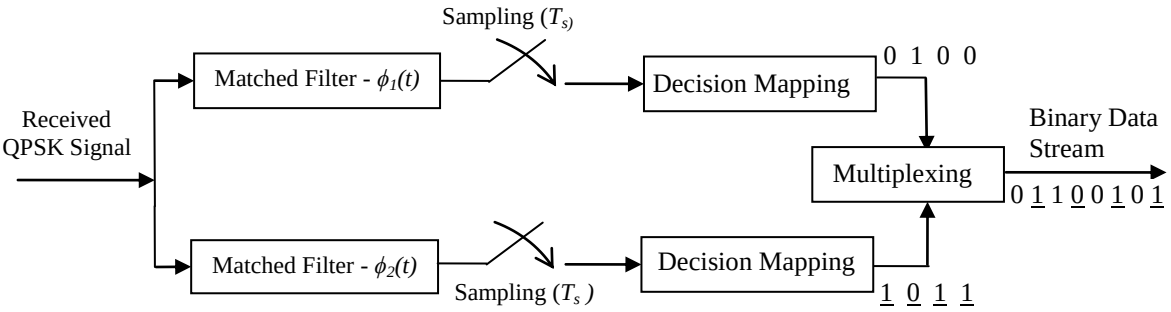

Fig 5: QPSK Demodulator for DS- Spread Spectrum CDMA communication

length. In the receiver, the received signal is multiplied again by the same (synchronized) PN code. This operation completely removes the code from the signal and the original data-signal is recovered. This implies that the despread operation is the same as the spread operation. Space Time Block Codes (ST-BC) have also been used for DS-CDMA system for producing hybrid sequence [13]. These schemes are used for user verification and signature purposes. Frequency Hoping CDMA systems are good for band jamming purposes [14].

2.4 QPSK Modulator for DS-CDMA

The Quadrature Phase-shift keying (QPSK) is a digital modulation scheme that transmits data by changing or modulating the phase of a carrier signal. QPSK uses a finite (four) number of phases each assigned a unique pattern of binary digits. Each pattern of bits forms the symbol that is represented by the particular phase. QPSK uses four points on the constellation diagram, equally spaced around a circle. With four phases, QPSK can encode two bits per symbol, as shown in Figure 4 with gray coding to minimize the Bit Error Rate (BER).

It can be shown mathematically that QPSK can be used either to double the data rate compared to Binary Phase Shift Keying (BPSK) or can reduce the bandwidth by 50 % by keeping the same data rate. This implies that QPSK transmits twice the data rate in a given bandwidth compared to BPSK at the same BER. QPSK, however, is more complex to implement. The

functioning and structural concept of QPSK modulator at transmitter is illustrated in Figure 3. The binary data stream is split into two components - the in-phase and Quadrature-phase components. These are then separately modulated onto two orthogonal basis functions. In this implementation, two sinusoids are used. Afterwards, the two signals are superimposed, and the resulting signal is the QPSK signal. Source encoding is chosen as polar Non-Return-to-Zero (NRZ). These encoders can be placed before for binary data source, but have been placed after to illustrate the conceptual difference between digital and analogue signals involved with digital modulation

2.5 QPSK Demodulator for DS-CDMA

The demodulator, which is designed specifically for the same symbol-set used by the modulator, determines the phase of the received signal and maps it to the symbol it represents. Thus the original data is recovered. This requires the receiver to be able to compare the phase of the received signal to a reference signal. Such a system is termed coherent system. Conversely, demodulator can just check for the phase changes alone to determine the bit received. In that case there is no need for local reference carrier signal but results in increased BER The typical structure of QPSK demodulator / receiver is shown in Figure 5. The matched filters can be replaced with correlators. Each detection device uses a reference threshold value to determine whether a 1 or 0 is detected

3. IMPLEMENTATION OF DS-CDMA

3.1 DS-Spread Spectrum

Figure 6 shows the simulated results in the form of wave diagrams of timing events of Spread Stream digital sequence ready for transmission. The main parameters are chosen as follows: *clk* with clock period = *1 millisecond*, *rst* is set to *0.* It can be easily explained with the help of one such experimental result that how it works. Consider one of the inputs as *1010,* and corresponding PN sequence from Figure 6 can be found to be *0010 0011 1101 011.* The combination is then simulated. This results in de-spreading data sequence of 60 bit length. The spread sequence in this example is found to be *0010 0011 1101 011 1101 1100 0010 100 0010 0011 1101 011 1101 1100 0010 100* which is represented by tag named *spread_data (59:0).* This is the final spread data to be modulated by using QPSK modulation scheme and then to be transmitted. The QPSK scheme required an even number of bits in the spread sequence. It will then take a pair of bits and map the pair with one of the four quadrants according to the values of the bits for gray code scheme as shown in the figure 4. This is called symbol mapping. The mapped symbols are transmitted further to the channel which may have noise.

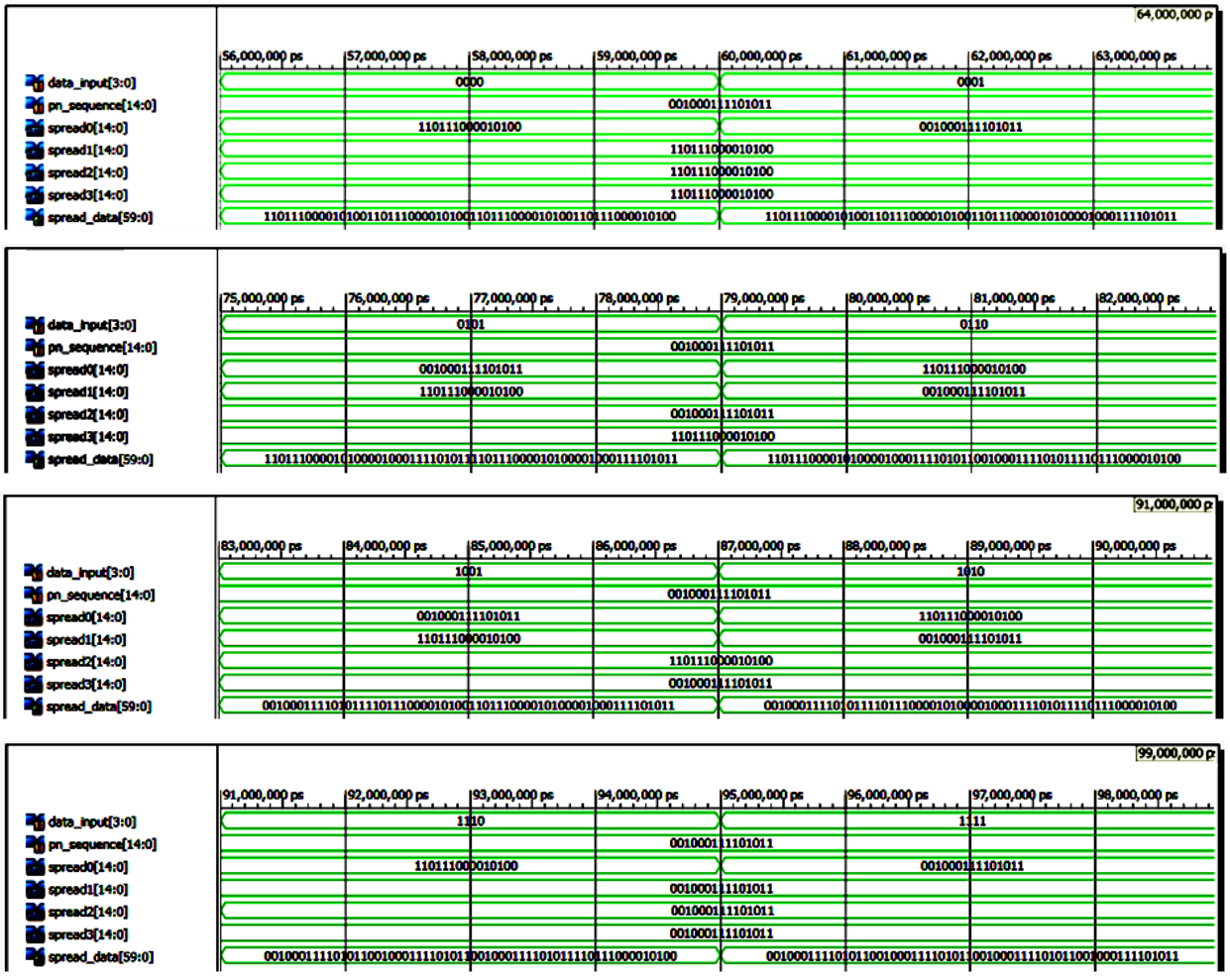

Fig 6: DS-Spread Stream results on XILINX FPGA

Time in ps	9,000,000 ps	9,500,000 ps	10,000,000 ps	10,500,000 ps
spread_data_input [59:0]	11011100001010011011100001010011011100001010011011100001010	011011100001010011011100001010011011100001010000100011110101		
receiver_pn_sequence [14:0]	001000111101011			
received_spared0 [14:0]	110111000010100		001000111101011	
received_spared1 [14:0]	110111000010100			
received_spared2 [14:0]	110111000010100			
received_spared3 [14:0]	110111000010100			
de_spread_data [3:0]	0000		0001	

Time in ps	15,000,000 ps	15,500,000 ps	16,000,000 ps	16,500,000 ps
spread_data_input [59:0]	11011100001010000100011110101110111000010100001000111101011		11011100001010000100011110101100100011110101111011000010100	
receiver_pn_sequence [14:0]	001000111101011			
received_spared0 [14:0]	001000111101011		110111000010100	
received_spared1 [14:0]	110111000010100		001000111101011	
received_spared2 [14:0]	001000111101011			
received_spared3 [14:0]	110111000010100			
de_spread_data [3:0]	0101		0110	

Time in ps	21,000,000 ps	21,500,000 ps	22,000,000 ps	22,500,000 ps
spread_data_input [59:0]	00100011110101111011100001010011011100001010000100011110101		00100011110101111011100001010000100011110101111011000010100	
receiver_pn_sequence [14:0]	001000111101011			
received_spared0 [14:0]	001000111101011		110111000010100	
received_spared1 [14:0]	110111000010100		001000111101011	
received_spared2 [14:0]	110111000010100			
received_spared3 [14:0]	001000111101011			
de_spread_data [3:0]	1001		1010	

Time in ps	9,000,000 ps	9,500,000 ps	10,000,000 ps	10,500,000 ps
spread_data_input [59:0]	00100011110101100100011110101100100011110101111011000010100		00100011110101100100011110101100100011110101100100011110101	
receiver_pn_sequence [14:0]	001000111101011			
received_spared0 [14:0]	110111000010100		001000111101011	
received_spared1 [14:0]	001000111101011			
received_spared2 [14:0]	001000111101011			
received_spared3 [14:0]	001000111101011			
de_spread_data [3:0]	1110		1111	

Fig 7: Receiver results after de-spreading and demodulating received data from a noisy channel

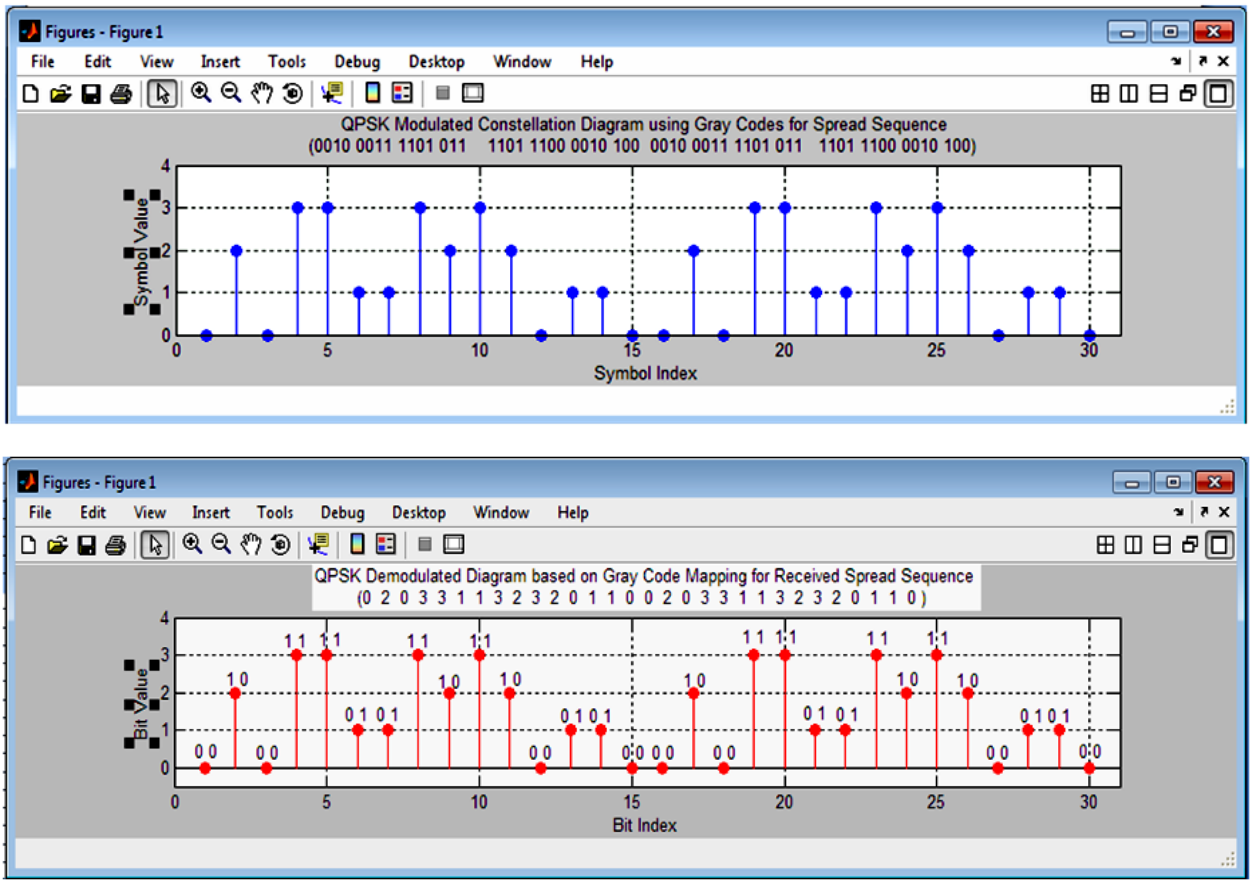

Fig 8 – Mapping of spread message data into QPSK symbols while transmitting and de-mapping at receiver

3.2 DS-De-Spread Sequence

De-spreading is reverse process of spreading. This implies that from de-spreading sequence, the original message bits are to be extracted. Figure 7 shows the simulated results in the form of waveforms of timing diagram for de-spreading digital sequence stream received at receiver by using locally generated PN-sequence and de-spreading algorithm. The main parameters are chosen as follows: *clk* with clock period = *1 millisecond*, *rst* is set to *0*. The output is the original message data recovered. To explain the working of the receiver for de-spreading operation an experimental result may be illustrated. Assuming that a 60 bit long input spread sequence received by receiver is *0010 0011 1101 011 0010 0011 1101 011 0010 0011 1101 011 1101 1100 0010 100.* This sequence is operated upon by locally generated PN sequence, in this example is *0010 0011 1101 011,* which was also used at transmitter for spreading. After simulation, the extracted message data is found to be *1110*, clearly as shown in Figure 7. Similarly further, additional tests are carried out to check the effectiveness of implemented de-spreading algorithm circuit for message data of *0000, 0001, 0101, 0110, 1001, 1010, 1110* and *1111*. All of these message data spreading and de-spreading are clearly illustrated by Figure 7. This verifies that any binary spread spectrum communication system can be implemented by scaling up the procedure explained in this paper. The experimental results can be verified as shown in the table 1, that this is very simple and less complex design as a very few gates and logic slices are used by circuit when implemented on FPGA chip.

Table 1. Summary of logic device utilization on FPGA

Slice Logic Utilization	Used	Available	Utilization
Number of Slice Registers	6	93,120	1%
Number used as Flip Flops	6		
Number of Slice LUTs	3	46,560	1%
Number used as logic	1	46,560	1%
Number using O6 output only	1		
Number used exclusively as route-thrust	2		
Number with same-slice register load	2		
Number of occupied Slices	3	11,640	1%
Number of LUT Flip Flop pairs used	4		
Number with an unused LUT	1	4	25%
Number of fully used LUT-FF pairs	3	4	75%
Number of unique control sets	2		
Number of slice register sites lost to control set restrictions	10	93,120	1%
Number of bonded IOBs	7	240	2%
Number of BUFG/BUFGCTRLs	1	32	3%
Number used as BUFGs	1		
Number of STARTUPs	1	1	100%
Average Fan-out of Non-Clock Nets	4.67		

4. RESULT ANALYSIS

The results of QPSK modulation implemented on MATLAB Communication Tool box are shown in Figure 8. The input sequence is [*0010 0011 1101 011 1101 1100 0010 100 0010 0011 1101 011 1101 1100 0010 100*]. The modulated binary bit pairs are converted into 4 symbols as shown in *y*-axis. 60 bit long message data stream is converted into 30 symbols of information by QPSK. The results of QPSK demodulation implemented on MATLAB Communication Tool box are also shown in Figure 8. The input sequence is firstly assumed to be noise free or ideal and then it is QPSK demodulated using MATLAB and C codes. Results at receiver verify mapping of the same sequence which was transmitted. The recovered sequence is [*0010 0011 1101 011 1101 1100 0010 100 0010 0011 1101 011 1101 1100 0010 100*], as shown in Figure 8. This is the same sequence which was transmitted. The two binary bits (*a pair*) are converted into one of the 4 symbols. Figure 8 shows the constellation diagram for QPSK demodulator while considering that there was no noise in the channel which is ideal case and for which there is no observed phase distortion. The recovered data at receiver is interpreted as *1010* as shown in figure 7. The performance of the implemented sub- systems of proposed DS-CDMA communication system is analyzed based on the number of gates or devices utilized. The summary is presented as shown in Table 1. Implementation is carried out on XILINX FPGA chip type xc6vlx75t-3ff484 and simulation is executed using ISE 12.1 version software EDA tool from XILINX.

5. CONCLUSION

The fundamental concept used for transmitter and receiver hardware of cellular communication system is implemented for CDMA scheme. Transceiver is realized by developing VHDL codes and testing the same for a wide range of input conditions. The logic implemented is very simple and faster. A 15-bit chip rate (PN sequence – *1001 0001 1110 101*) is realized by shifting the input through the D-flip flops. A minimal polynomial property is made compulsory so that PN sequence repeats after a cycle of chip code length (15 in this case). The PN sequence is achieved by providing feedback from the outputs of some of the registers (called taps) according to minimal polynomial used. The feedback is then fed back into the most significant register after passing them through a modulo-2 adder circuit. The process of realizing LFSR is carried out by first developing the VHDL code for a D-flip flop. The same D- flip flop code is then called 4 times in the main VHDL program to realize the required LFSR. In the implementation part of PN sequence, tapings are taken from 1^{st}, 3^{rd} and 4^{th} positions of LFSR so as to obtain the maximum length of binary digits produced before they are being repeated. A dead lock condition is observed in the case when the initial input into the first register and output of the XOR gate are all 0's. Under this condition the output of all the register of the LFSR PN generator remains as *0* at all instants of time. Therefore it is necessary that the initial input to the PN generator must be equal to *1* which is also the output of the modulo-2 circuit. The VHDL code for implementing all subsystem circuits of transceiver are simulated on XILINX ISim and ModelSim and hence, the results were generated and tested successfully for a wide variety of message data selected randomly. Implementation was done using XILINX FPGA with clock frequency of 100 MHz range.

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7. REFERENCES

[1] Cottatellucci L., Muller R. R. and Debbah M, 2010, Asynchronous CDMA System with Random Spreading – Part I : Fundamental Limits, IEEE Transactions on Information Theory, Volume : 56, Issue : 4, Pages 1477-1497

[2] Do G. L. and Feher K., 1996, Efficient Filter Design for IS-95 CDMA Systems, IEEE Transactions on Consumer Electronics, Volume: 42, Issue: 4 Pages 1011 – 1020.

[3] Boukadourn M., Tabari K., Bensaoula A., Starikov D. and Aboulhanid E. M., 2005, FPGA Implementation of a CDMA Source Coding and Modulation Subsystem for a Multiband Fluorometer with Pattern Recognition Capabilities, IEEE International Symposium on Circuits and Systems, Volume : 5, Pages 4767 – 4770.

[4] Clarke P. and de Lamare R. C., 2011, Low-Complexity Reduced-Rank Linear Interference Suppression Based on Set-Membership Joint Iterative Optimization for DS-CDMA Systems, IEEE Transactions on Vehicular Technology, Volume : 60, Issue : 9, Pages 4324 – 4337.

[5] Vishwas Sundaramurthy and Joseph Cavallaro, 1999, A Software Simulation Testbed for Third Generation CDMA Wireless Systems, Proc. 33rd Asilomar Conf. on Signals, Systems and Computers, Pacific Grove C. A.

[6] Uuanbin Guo, Dennis McCain and Joseph R Cavallaro, 2004, Low Complexity System-on-Chip Architecture of Parallel- Residue-Compensation in CDMA Systems, ISCAS, Pages : IV 77 - 80

[7] Neiyer S. Correal, Michael Buehrer R. and Brian D. Woerner, 1999, A DSP-Based DS-CDMA Multiuser Receiver Employing Partial Parallel Inference Cancellation, IEEE Journal on Selected Areas in Communications Volume: 17 No. 4, Pages 613-630.

[8] Tomaso Erseghe and Antonio Maria Cipriano, 2011, Maximum Likelihood Frequency Offset Estimation in Multiple Access Time- Hopping UWB, IEEE Transactions on Wireless Communications, Volume: 10, No. 7, Pages 2040 – 2045.

[9] Theodore S. Rappaport, 2010, "Wireless Communication - Principles and Practices", 2ND Edition, Pearson Education, Dorling Kindersley (India) Pvt. Ltd.

[10] Min Shi D'Amours, C. Yongacoglu, A. 2010, Design of spreading permutations for MIMO-CDMA based on space-time block codes, Communications Letters, IEEE, Volume: 14 Issue: 1, Pages: 36 – 38.

[11] Magaa, M.E., Rajatasereekul, T., Hank, D. and Hsiao-Hwa Chen, 2007, Design of an MC-CDMA System That Uses Complete Complementary Orthogonal Spreading Codes", IEEE Transactions on Vehicular Technology, Volume: 56, Issue: 5, Pages: 2976 – 2989.

[12] Alaka Barik and Asutosh Kar, 2011, ICI Self-Cancellation Method of BPSK OFDM, IJCA Proceedings on International Conference on VLSI, Communications and Instrumentation (ICVCI) (15), Published by Foundation of Computer Science, Pages 12-14.

[13] Shiunn-Jang Chern and Ming-Kai Cheng, 2010, New ST-BC MIMO-CDMA transceiver with augmented user signatures, Intelligent Signal Processing and Communication Systems (ISPACS), IEEE International Symposium on, Pages: 1-4, DOI: 10.1109/ISPACS.2010.5704632

[14] Haichang Sui and Zeidler J.R., A Robust Coded MIMO FH-CDMA Transceiver for Mobile Ad Hoc Networks, 2007, IEEE Journal on Selected Areas in Communication Volume: 25 Issue: 7, Pages: 1413 – 1423, DOI: 10.1109/JSAC.2007.070914