PMOS based 1-Bit Full Adder Cell

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ABSTRACT
This paper presents post layout simulations of a new 8T full adder cell using a new 3T XOR gate implemented by pMOS transistors only. This proposed design operates efficiently in super threshold region to achieve ultra low power and hence reduced power-delay product (PDP). The proposed design demonstrates its superiority against existing adder in terms of power–delay product, temperature sustainability and noise immunity. It also shows remarkable improvement in threshold loss as compared to existing 8T full adder for certain input combinations. Therefore, the proposed design outperforms the existing adder and proves to be an optimal option for low power and energy efficient applications. All the post-layout simulations have been performed at 45nm technology on Tanner EDA tool version 13.0.

Keywords
3T, 8T, full adder, PDP and XOR.

1. INTRODUCTION
Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift where power dissipation has become as important a consideration as performance and area [1] and [2]. Addition is one of the fundamental arithmetic operations. It is used extensively in many VLSI systems such DSP architectures, microprocessors, etc. In addition to its main task which is adding two binary numbers, it is the nucleus of many other useful operations such as subtraction, multiplication, division, etc. So, it is very important to choose the adder topology that would yield the desired performance. That's why, building low-power, high performance adder cells are of great interest and any modifications made to the full adder would affect the system as a whole.

IC Layout or mask design is the representation of an integrated circuit in terms of planar geometric shapes which correspond to the patterns of metal, oxide, or semiconductor layers that make up the components of the integrated circuit. In other words, Layout is the process by which a circuit specification is converted to a physical implementation with enough information to deduce all the relevant physical parameters of the circuit.

The paper is organized as follows: Section 2 describes an existing 8T full adder cell as reported in the literature. Section 3 introduces the proposed 3t XOR cell and 8T full adder design. Simulation results and their comparisons are included in Section 4 and finally Section 5 concluded the paper.

2. PREVIOUS WORK
The full adder operation can be stated as follows: Given the three 1-bit inputs A, B, and Cin, it is desired to calculate the two 1-bit outputs Sum and Carry, where

$$Sum = (A \oplus B) \oplus Cin \quad (1)$$
$$Cout = AB + Cin\,(A \oplus B) \quad (2)$$

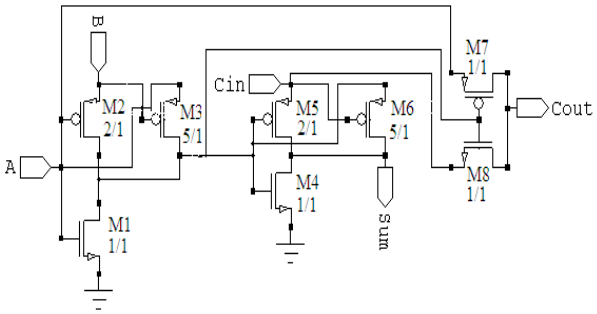

Fig 1: Schematic of 1-bit 8T Full Adder

Fig. 1 shows the schematic of eight transistor (8T) 1-bit full adder cell. The Sum output is basically obtained by a cascaded exclusive ORing using 3T XOR gate [3] of the three inputs. Cout is implemented using 2T multiplexer. Fig. 2 shows the layout design of 1-bit 8T full adder.

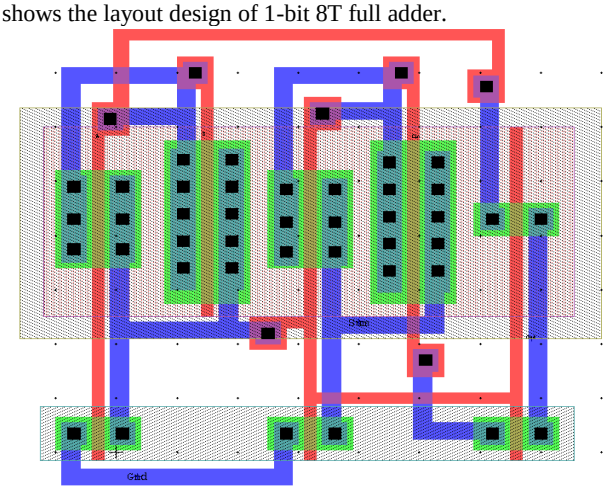

Fig 2: Layout of 1-bit 8T Full Adder

In the design of Fig.1 two stage delays are required to obtain the Sum output and at most two stage delays are required to obtain the carry output Cout[4]-[7]. It has serious threshold loss for inputs are 000, 010, 100 and 110 due to simultaneous

enabling of two transistors. Logic high output at first stage of XOR gate enables M4 and Cin =0 enables M6 and similarly, logic low output at first stage of XOR gate enables M5 and Cin =0 enables M6. Thus, Sum output is degraded due to reduced device resistance as the ON transistors will have combined parallel effect on resistance. The outputs have good logic level for only four input vectors. For the remaining input vectors, there is a major degradation in output voltage that may lead to functional failure as well as increased power consumption. As the voltage is scaled down, the signal integrity deteriorates and the speed decreases tremendously.

3. PROPOSED 3T XOR CELL AND 8T FULL ADDER DESIGN

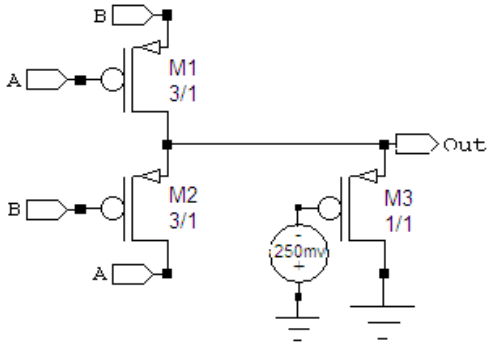

Fig 3: Schematic of proposed 3T XOR cell

The design of full adder is based on the design of the XOR gate. The schematic of new 3T XOR cell is shown in Fig. 3. It consists of 3 pMOS transistors and an negative input supply voltage of 250 mV is given to M3 so that it conducts in weak inversion and eliminates the negative voltage spikes for input combination '00'. The W/L ratios of transistors M1and M2 are taken as 3/1 to minimize the voltage drop due to the threshold loss in transistors. When AB=00, all transistors are ON and as pMOS is weak '0' device, it will pass low logic signal with threshold loss.

When AB=01, M1 is ON and pMOS being strong '1' device will pass complete logic high at the output but as M3 is always ON, so due to parallel resistance of both the devices the output will be slightly degraded than logic '1' and similar case will happen with AB =10. For AB=11, only M3 is ON and pMOS is weak '0' device, it will pass low logic signal with threshold loss.

The substrate terminals of all the transistors are connected to respective source terminal in order to nullify the substrate bias effect. This proposed design for XOR gate gives better performance than existing one. Table 1 states the performance of both the designs.

Table 1. Performance Table of Existing and Proposed 3T XOR cell

A (Volt)	B (Volt)	Expected Output (Volt)	Obtained Output (Volt)	
			Existing	Proposed
0	0	0	-0.13	0.02
0	1	1	0.99	0.84
1	0	1	0.76	0.84
1	1	0	0	0.02

Using this XOR gate an 8T adder has also been realized. Fig. 4 and Fig. 5 shows the schematic and layout design of proposed 8T full adder cell design. In this, Sum module has been implemented using cascaded 3T XOR gate in accordance with equations (1) and (2) and Cout module is designed by using 2T multiplexer.

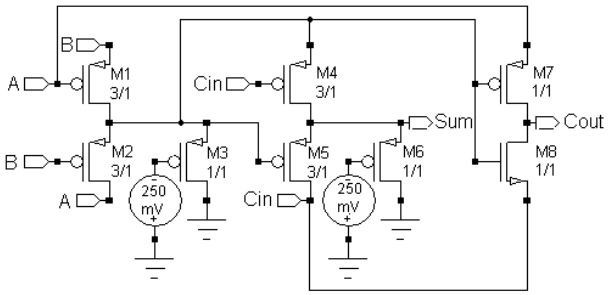

Fig 4: Schematic of proposed 8T full adder

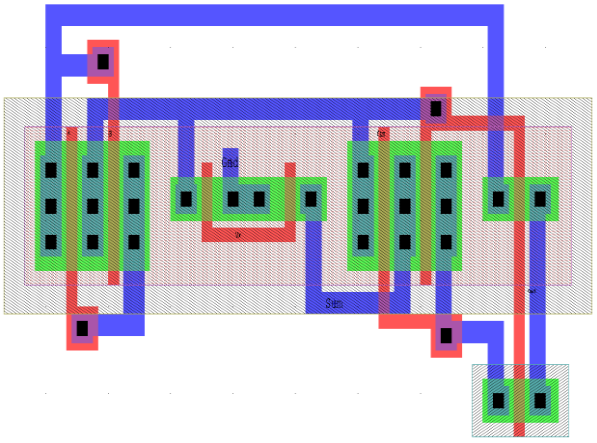

Fig 5: Layout Design of Proposed Full Adder cell

Table 2. Performance Table of Existing and Proposed 8T Full adder cell

A	B	Cin	Sum (Existing)	Sum (Proposed)
0	0	0	<< $\lvert V_{Tp} \rvert$	2% of logic "0"
0	0	1	1	90% of logic "1"
0	1	0	***50% of logic "1"***	***70% of logic "1"***
0	1	1	0	6% of logic "0"
1	0	0	***50% of logic "1"***	***70% of logic "1"***
1	0	1	0	6% of logic "0"
1	1	0	<< $\lvert V_{Tp} \rvert$	2% of logic "0"
1	1	1	1	90% of logic "1"

This proposed design shows small voltage drop for certain input combinations but this drop is so less that it can be assumed as logic high. Table 1 depicts the performance of both the designs. For inputs '000', all transistors are ON and

as pMOS is weak '0' device, it will pass low logic signal with threshold loss. For 010, M1 is ON and pMOS being strong '1' device will pass complete logic high at the output but as M3 is always ON, so due to parallel resistance of both the devices the output will be slightly degraded than logic '1'. Logic high output at first stage XOR will be passed through M4 but since M6 is always ON, so due to parallel resistance of both the devices the output will be slightly degraded than logic '1'and similar case will happen with AB =100. It is evident from Table 2 depicts that the proposed design has improved threshold loss as compared to existing one.

4. SIMULATIONS AND COMPARISON

All post layout simulations are performed on Tanner EDA tool version 13.0 using 45nm technology with input voltage ranges from 0.5 to 1.0 V in steps of 0.1 V. In order to prove that the proposed design is consuming low power and have better performance, simulations are carried out for power consumption and delay and as a result the overall PDP at varying input voltages and temperature has been estimated. Also to ensure the better noise immunity of the proposed design, output noise voltages have been extracted at varying frequency. To establish an impartial testing environment both circuit have been tested on the same input patterns which covers all combinations of the input stream.

After the physical layout designing post-layout simulations are carried out with extraction of parasitic capacitances. Power consumption is a function of load capacitance therefore any reduction in capacitance will lead to reduced power consumption. Table 3 shows significant improvement in total as well as output parasitic capacitance of the proposed full adders over existing one.

Table 3. Parasitic Capacitance of existing and proposed full adder cells

Full Adder Cells	Parasitic Capacitance (fF)	
	Total	Output
Existing	0.822	0.185
Proposed	0.564	0.125

The proposed design of full adder cell has remarkably less parasitic capacitance than existing design and hence, as power consumption is directly proportional to capacitance, therefore proposed design will also have remarkable reduction in power consumption. Also, both the adders has been implemented with same logic of cascading XOR gate therefore both have equal number of power consuming transitions at all the nodes and as a result switching activity will remain constant for both the adder designs. In the layout design of the proposed full adder cell, number of poly contacts is four and in existing designs it is seven. The number of overlaps is also less in proposed design. Thus, this leads to the improved power consumption of proposed design than the existing adder. The results for the same are shown in Fig. 6- Fig. 8.

Fig. 6 depicts the superiority of proposed 8T full adder in terms of PDP with varying input voltage. Fig. 7 reveals the better performance of proposed design over existing one. As the proposed cell is implemented using pMOS transistors only, therefore, the power consumption will decrease with increasing temperature and hence the PDP.

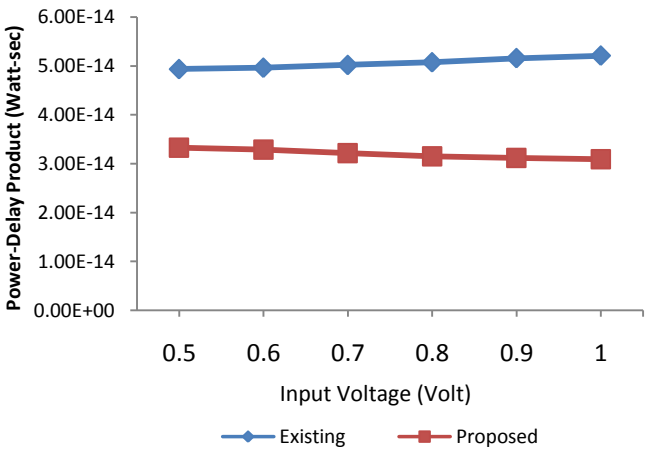

Fig 6: PDP vs input voltage

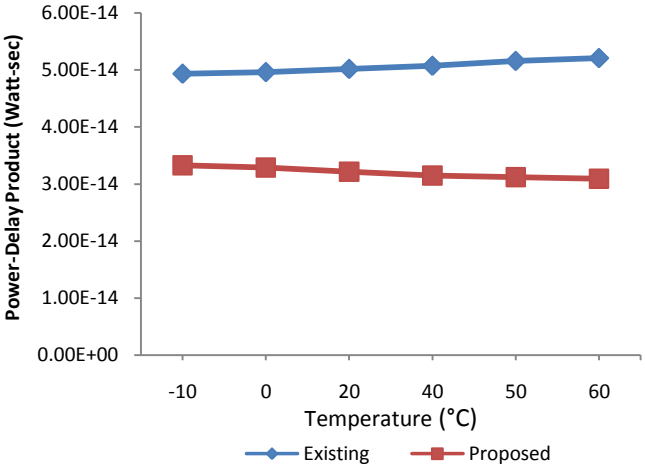

Fig 7: PDP vs varying temperature at 0.6 input voltage

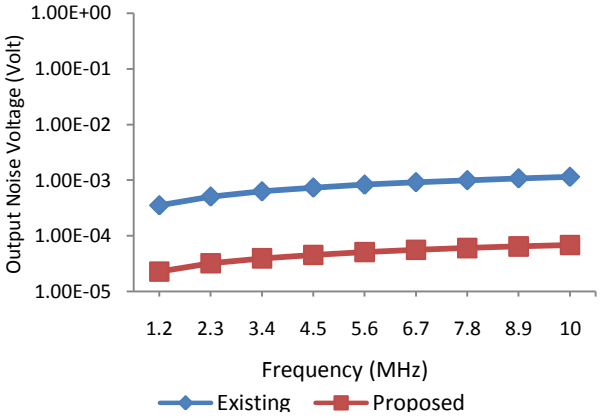

Fig 8: Output noise voltage with operating frequency

This is due to NBTI effect [8] which demonstrates the negative shift of threshold voltage caused by variation in temperature. Also the Fermi potential of the pMOS reduces with increase in temperature [9] and as a result the device threshold voltage will also decrease. On the other hand, power consumption is dependent on threshold voltage and hence it will also reduce as shown in Fig.7. Also, the noise immunity of proposed cell is remarkably better than existing one as shown in Fig.8. Therefore, the proposed adder can be a better

option for complex system design such as ripple carry adder, array multiplier etc.

The graphs based on post-layout simulations shown in Fig. 6-Fig. 8 results into the better performance of proposed design in comparison to existing design.

5. CONCLUSION

The proposed 8T full adder cell has been designed using a new 3T XOR cell implemented by pMOS transistors only. Schematic and layout of both the adder circuits in this paper have been designed and simulated using 45nm technology. The PDP of proposed circuit is remarkably improved with respect to increasing input voltage as well as temperature. Also the parasitic extracted and the output noise voltage simulated is better than the existing design. Hence in a nutshell the proposed adder proves itself to be a better option for low power devices and systems design than its peer design.

6. REFERENCES

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