

Analysis of Performance factors for PLL based Frequency Synthesizers for Wireless Applications and Impact on Overall Performance

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ABSTRACT

This paper presents the PLL based Frequency Synthesizers, which are used in modern devices for generating wide range of frequencies. The Performance depends on several factors such as phase noise, spurious outputs, loop bandwidth and lock time. The parameters loop bandwidth and lock time are inter-related which are inversely proportional to each other is simulated and the results are given. The Phase Noise for the VCO depends on the frequency range in which it is used and given by Lesson's equation. It varies linearly and L-Band and higher frequencies but varies at 6dB per octave at lower frequencies in hundreds of MHz or tenths of GHz. The results are simulated in MATLAB and presented in this paper.

Keywords

Frequency synthesizers, Phase Noise, Lesson's equation

1. INTRODUCTION

Frequency Synthesizer which can generate wide of a range of frequencies is found in many modern devices, including Radiotelephones, CB Radios, Satellite Receivers, GPS systems etc. It can perform frequency multiplication, frequency division, and frequency mixing operations to produce the desired output signal [1].

Phase Locked Loop, is a negative feedback controlled system, which compares the phases of two input signals and produces an error signal that is proportional to the difference between their phases. The Low Pass filtered error signal is used to drive a voltage-controlled oscillator (VCO), which creates an output frequency. The output frequency that is fed through a frequency divider back to the input produces a negative feedback loop.[2]

2. PLL PERFORMANCE PARAMETERS ANALYSIS

Recently the technology used for the PLL designs are simpler when compared to primitive synthesizers. The basic frequency synthesize has building blocks containing phase detector, VCO with feedback having divided N-counter and sub circuits like loop filter, reference oscillator and other interfacing components. Synthesizer used for wireless applications need to operate over a fraction of bandwidth. [3][4]

2.1 Effect of Loop Bandwidth on Performance:

The selection of loop filter components will have the impact on the loop bandwidth. The relationship between the loop bandwidth and hop time results in that the narrower the bandwidth, the longer the synthesizer takes to step from one frequency to another. [5]

The Hop Time or Lock Time for a specific loop bandwidth is computed as follows:

$$T_s = \frac{-1 \times \left(\ln \frac{F_A}{F_{STEP}} \right)}{F_N \times 2\pi \times 2\xi} \dots (1)$$

Where Natural Frequency F_N is

$$F_N = \frac{2 \times \text{loop bandwidth}}{2\pi \left(\xi + \frac{1}{4 \times \xi} \right)} \dots (2)$$

F_A is the frequency of the carrier,

F_{STEP} is Maximum Frequency change during a step,
 ξ is Damping factor; typically, 0.707

By Taking Different Values of Loop Bandwidth the Hop Time is obtained as shown in the Table 1.

Table-1 Hop Times for Various Loop Bandwidths

Loop Bandwidth (Hz)	Hop Time (ms)
300	25.8
700	11.0
1500	5.2
3000	2.6

The Loop Bandwidth vs. Hop Time plot is as follows:

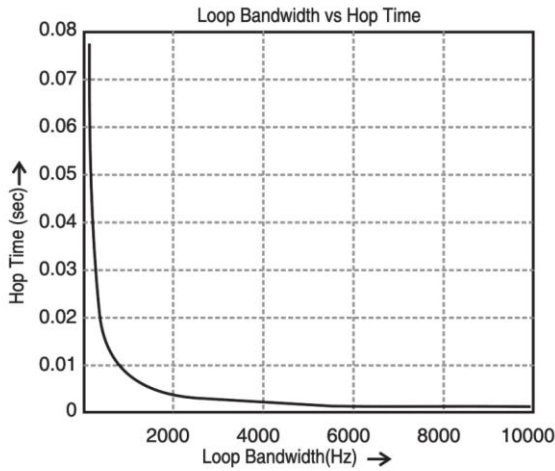


Fig (1) Loop Bandwidth Vs Hop Time

2.2 Effect of Phase noise on Performance:

Moving to the next parameter, which majorly contributes to the PLL performance, is the Phase Noise. Various blocks of the PLL contribute this Noise. VCO phase noise is caused due to various different components given by the Lessons equation.

Using Lesson’s equation the different noise components in a VCO given as

$$L_{PM} = 10 \log \left[\frac{FKT}{A} \frac{1}{8Q_L^2} \left(\frac{f_o}{f_m} \right)^2 \right] \dots\dots (3)$$

Where

- L_{PM} is single-sideband phase noise density (dBc/Hz)
- F is the device noise factor at operating power level A.
- K is the Boltzman’s Constant.
- T is the temperature (K).
- A is oscillator output power (W)
- Q_L is loaded Q (dimensionless)
- f_o is oscillator carrier frequency
- f_m is frequency offset from the carrier

In order to satisfy the Lesson’s equations the following of the conditions

- The offset frequency f_m from the carrier is greater than 1/f flicker corner frequency.
- The device operator should be linear.
- The noise factor at the operating power level is known.

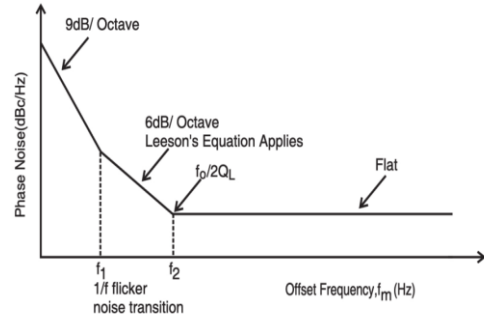


Fig (2) Phase noise in a VCO vs frequency offset

As shown in fig (2) it is observed that in the knee region between the break f_1 and the transition from the 1/f flicker corner frequency and to a frequency beyond where the amplified white noise dominates. Further f_1 should be as low as possible which is less than 1 KHz where as f_2 is in few MHz.[4][6]

In order to minimize the phase noise in VCO, the main guidelines followed are

- Keep the tuning voltage of the varactor sufficiently high.
- Using filtering on the dc voltage supply.
- Maximize the average power at the tank circuit output.

As shown in the fig(3) the VCO phase noise is plotted against the offset frequency we observed that the phase noise for hundreds of MHz seen as 6dB per octave where at higher frequencies as we go the phase noise seems to be minimized.

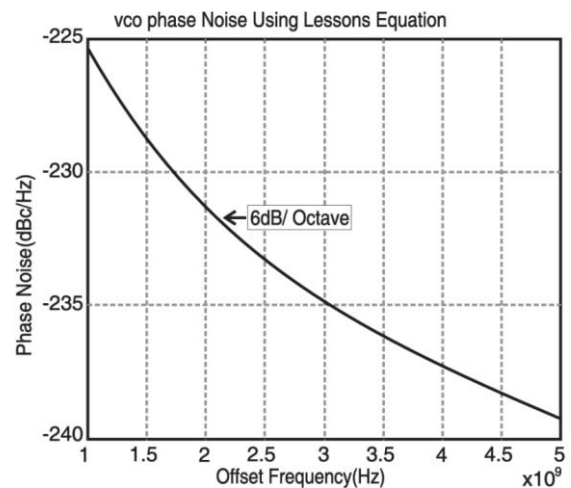


Fig (3) Phase Noise for Frequencies in MHz

Further, as shown in fig (4) & (5) at higher frequencies it is observed that in both L and S-bands the phase noise seems to be linear.

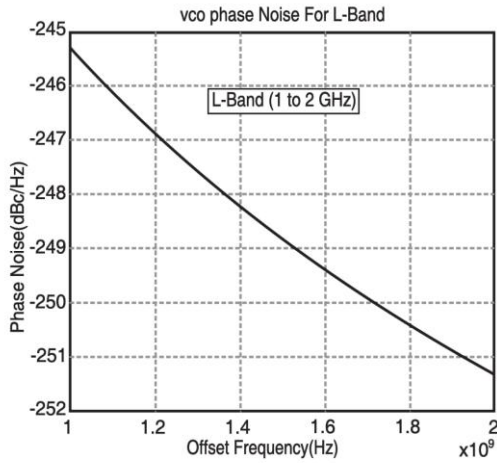


Fig (4) VCO Phase noise in L-Band

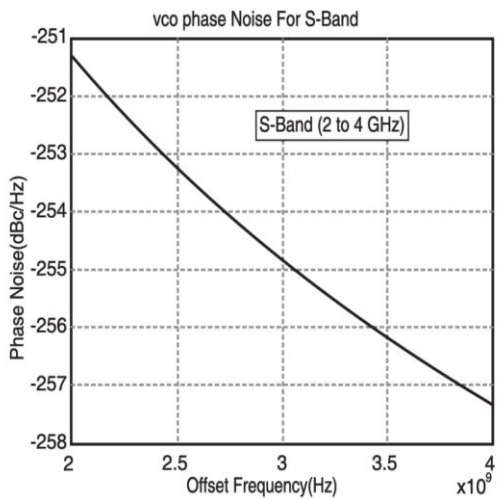


Fig (5) VCO Phase Noise for S-Band

Now consider the fig(6) showing the phase noise contribution in a PLL

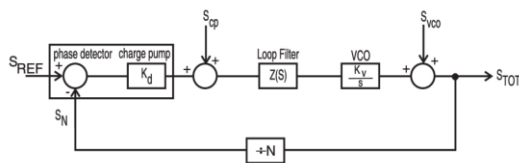


Fig (6) PLL-Phase Noise Contributors

The system transfer function can be described by the following equations.

$$\text{Closed Loop Gain} = G / (1+GH)$$

$$G = K_d * K_v * Z(s) / s$$

$$H = 1 / N$$

$$\text{closed loop gain} = \frac{k_d * k_v * z(s)}{\frac{s}{k_d * k_v * z(s)} + N * s} \dots\dots (4)$$

Fig(6) shows different contributions for the phase noise in various blocks of a PLL. The phase noise is obtained by taking the transfer function of the loop filter, VCO, reference counter and phase detector. The results are simulated using MATLAB and are as shown. The filter phase noise is also computed and compared with other noise contributors.

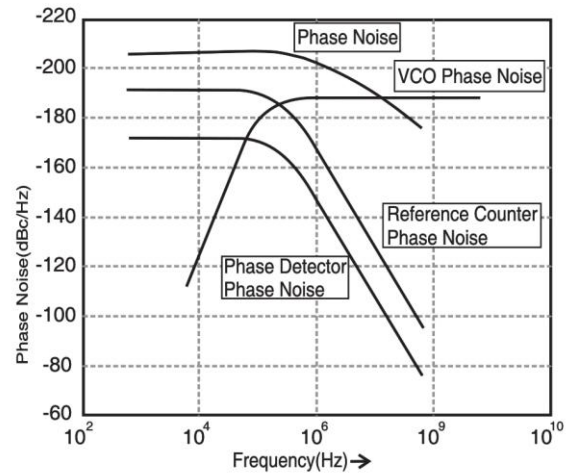


Fig (7) Phase Noise at different Blocks and Total Phase Noise

3. CONCLUSION

The phase noise performance of PLL in L-band and S-band, it is observed that both the loop bandwidth and hop time are inversely proportional to each other. Firstly it is noticed that the value of loop bandwidth should not exceed a certain limit beyond which there is an effect of phase perturbations.

Secondly, it is the phase noise which is the major problem in frequency synthesizer particularly in the VCO. It is also observed from Lesson's equation for VCO at frequency below L-band the curve follows an attenuation of 6dB per Octave and as frequency is increase from L-band to S-band the phase noise seems to be linear and impact of phase noise seems to be minimized and there by reaching a constant value which is shown in Fig(7)[VCO phase noise].The inference obtained from our results is well match as seen from Lesson's equation.

Finally the spurious outputs or the reference spurs are seems to be harmonics of the desired frequency and can be minimized by changing the order of passive filter .we can minimize the phase noise by altering the loop filter bandwidth.

4. ACKNOWLEDGMENTS

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5. REFERENCES

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