

# Design of High-performance Digital Logic Circuits based on FinFET Technology

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## ABSTRACT

Double-gate FinFET is a novel device structure used in the nanometer regime, whereas the conventional CMOS technology's performance deteriorates due to increased short channel effects (SCEs). Double-gate (DG) FinFETs has better SCEs performance compared to the conventional CMOS and stimulates technology scaling. In this paper, we are designing 32nm DGFinFETs and extracting their characteristics by using Sentaurus TCAD, Simulated results of the device show that it can be governed at the nanometer - scale regime. DGFinFET has independent gates; threshold voltage of one gate can be altered by varying the voltage at the other gate. By using this phenomenon logic circuit can be configured in one of the modes such as SG mode, LP mode, IG mode and IG/LP mode. INVERTER and NAND gate are designed in the above mentioned node and comparison has been drawn between them. Based on the simulated results SG-mode is adequate for high-performance design.

## Keywords

Double-gate FinFET (DGFinFET), High-performance, Independent gate (IG) mode, Logic Gates, Low power (LP) mode, Short channel effects (SCEs), Shorted gate (SG) mode.

## 1. INTRODUCTION

Since the fabrication of MOSFET, the minimum channel length has been shrinking continuously. The motivation behind this decrease has been an increasing interest in high speed devices and in very large scale integrated circuits. The sustained scaling of conventional bulk device requires innovations to circumvent the barriers of fundamental physics constraining the conventional MOSFET device structure. In the concern of battery-operated portable devices power consumption, chip density and operating frequency has increased because of advanced nanometer process technologies [1] - [3]. Even in the case of nonportable devices, power consumption is also very important because of the increased in packaging density and cooling costs as well as potential reliability problems. Thus, power efficiency has assumed increased importance, to meet the performance requirements within a power budget for VLSI [14] designers. Speed and area are also important parameters and proper tradeoff between them should be drawn while designing a circuit. FinFETs (fin-type field effect transistors) [4], offer interesting power-delay tradeoffs and better characteristics (short-channel-effects) in the nanometer regime in order to meet the performance expected by the ITRS (International Technology Roadmap for Semiconductor) for the forthcoming technological nodes [5]. Furthermore, bulk architecture requires a high channel doping density in order to control the short channel effects, leading to large transversal electric fields and unacceptable degradation of the electron mobility.

Double-gate (DG) FinFETs are broadly classified into two types, namely, simultaneously driven double-gate (SDDG) and independently driven double gate (IDDG) [6], [7] FinFETs. SDDG behaves like a three-terminal MOSFET because it has both the gates (front and back) connected each other, whereas the IDDG has two independent gates. SDDG FinFETs have a third gate on top of the gate, called trigate, however the top gate of IDDG FinFET is detached through a thicker oxide layer. IDDG FinFETs has the superiority in threshold-voltage ( $V_T$ ) [8] and leakage-current control.

Due to nonplanar structure, and the width quantization effect of FinFET devices still suffers from the issue such as process complexity and additional parasitic capacitance; however it is promising candidate for the nanometer regime. Particularly in analog applications, the width quantization effect [9] is important and also where the self-loading dominates. For example, increasing the active width of the device increases the current and the load capacitance in the same ratio, thereby making the delay invariant. The channel width of the single fin device is restricted by the height of the fin  $H_{FIN}$ . The channel width for a multi gate device is given by following [10]:

$$W \sim 2H_{FIN} + W_{FIN} \quad (1)$$

Where  $W_{FIN}$  is the fin width. For a device having  $H_{FIN} = 60$  nm and  $W_{FIN} = 10$  nm, the effective channel width can be calculated [from (1)] as 130 nm. For technologies below 20-nm channel length, such a high channel width only increases the static and dynamic power dissipation (due to the higher currents) for a given value of delay.

This paper is organized as follows. Section 2 explains the double-gate (DG) FinFET devices realization and simulation setup. Variation of threshold voltage with back gate voltage is explained in section 3. Designing of different FinFET based logic gates in SG, LP, IG and IG/LP modes are presented in section 4. Section 5 describes the simulation results of various design-mode gates and finally Section 6 concludes the paper.

## 2. DEVICE REALIZATION

Figure 1 shows the top view of a single-fin double-gate (DG) FinFET realized using *Sentaurus Structure Editor* [11]. The device structure is having two gates (front and back gates). The most common mode of operation of the double-gate (DG) FinFET is to switch the two gates simultaneously. The threshold voltage of the DGFinFET can be varied by applying the bias to any one of the gate terminal based on the application of our design. Table 1 illustrates the device dimensions and doping levels of both p-type FinFET and n-type FinFET transistors. In order to control the short channel effects (SCEs), we are using the thickness of the fin equal to half of the channel length ( $L_G$ ) i.e.  $T_{FIN} = 15$  nm and  $L_G = 32$  nm. The fin channel is having a doping density of  $1 \times 10^{15} \text{ cm}^{-3}$  which rescue the random dopant fluctuations and improves the current drive (or gate capacitance)

per device area. Polysilicon is used as a gate material and silicon nitride for the spacer.

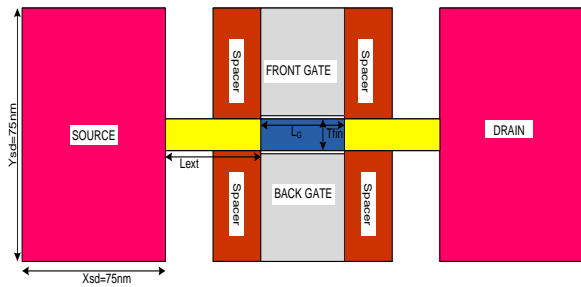


Figure 1 Double-gate (DG) n-channel FinFET Device structure of gate length  $L_G = 32$  nm

Table 1  
Device Dimensions and Dopings (for n-type and p-type FinFET)

Parameters	Values
$L_G$	32 nm
$T_{FIN}$	15 nm
$T_{OX}$	1nm
$L_{ext}$	32 nm
Spacers	16 nm
Xsd and Ysd	75 nm
Fin Doping	$1 \times 10^{15} \text{ cm}^{-3}$
S/D Doping	$1 \times 10^{20} \text{ cm}^{-3}$
Extension Doping	$1 \times 10^{19} \text{ cm}^{-3}$

The current-voltage ( $I_D$ - $V_G$ ) characteristics of double-gate (DG) FinFET are shown in Figure 2. The graph is plotted for  $V_{DS} = 0.05V$  and  $V_{DS} = 1V$ .

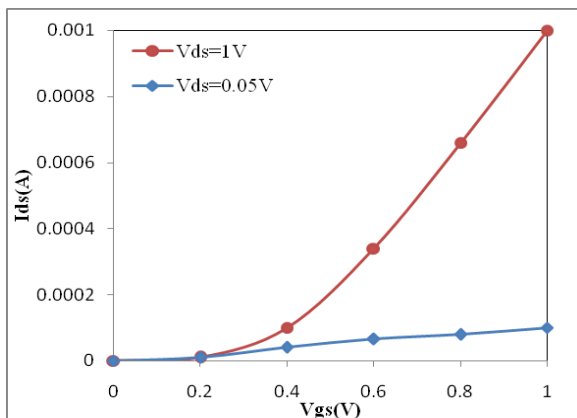


Figure 2  $I_D$ - $V_{GS}$  characteristics double-gate n-type FinFET Device of gate length  $L_G = 32$  nm

Figure 3 shows the  $I_D$ - $V_{DS}$  characteristics of NMOS device with the gate length ( $L_G$ ) of 32 nm, where  $V_{GS}$  is varied from 0.1V to 0.8V; same characteristics are also drawn for p-type FinFET device.

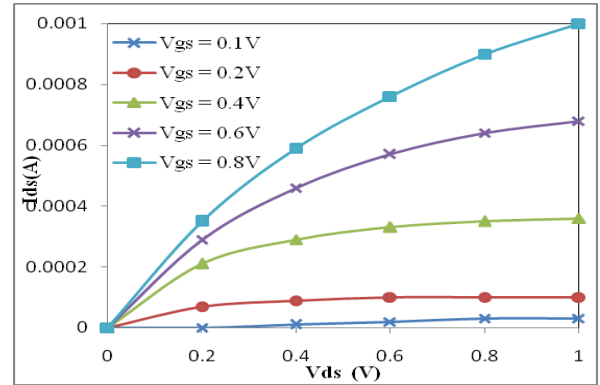


Figure 3  $I_D$ - $V_{DS}$  double-gate n-type FinFET Device of gate length  $L_G = 32$  nm

### 3. THRESHOLD VOLTAGE CONTROL IN FINFETS

FinFET has two gates, which can be operated independently or together. The threshold voltage at one gate can be controlled with the help of voltage at the other gate. Figure 4 shows the FinFET in different configurations. The transfer characteristic of shorted gate and independent gate is shown in the Figure 5, wherein for independent gate FinFET configuration we have applied different gate voltages at the back gate. The current  $I_{ON}$  and  $I_{OFF}$  for these configurations are tabulated in Table 2

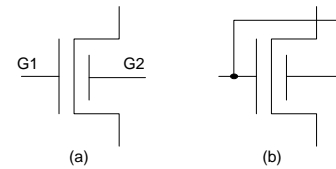


Figure 4 FinFET configurations (a) Independent gates (b) Shorted gates

Table 2  
Current  $I_{ON}$  and  $I_{OFF}$  for different back gate voltages

Back gate voltages	$I_{on}$ (A)	$I_{off}$ (A)
$V_{G2} = V_{G1}$	$3 \times 10^{-3}$	$1.02 \times 10^{-7}$
$V_{G2} = -0.4V$	$5.41 \times 10^{-4}$	$4.64 \times 10^{-10}$
$V_{G2} = -0.2V$	$7.52 \times 10^{-4}$	$4.2 \times 10^{-9}$
$V_{G2} = 0V$	$1.05 \times 10^{-3}$	$9.2 \times 10^{-8}$
$V_{G2} = 0.2V$	$1.31 \times 10^{-3}$	$5 \times 10^{-6}$

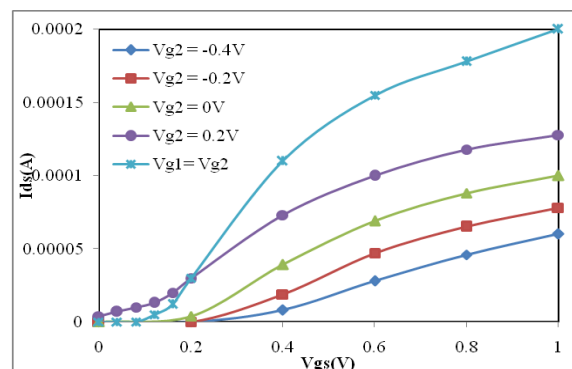


Figure 5 Transfer characteristics of FinFET with different back gate voltages

#### 4. DESIGNING OF DIFFERENT FinFET BASED LOGIC GATES

By using different methodologies used in section 3 we can design different logic gates. Logic gates can be configured in one of the following modes, (1) Shorted-gate (SG) mode of operation back gate is tied to front gate, in this case we get improved drive strength and have better control over the channel. (2) Independent-gate [12], [13] (IG) mode, in which independent signals drive the two device gates; back gate can have a different voltage from front gate. This may reduce the number of transistors in the circuit. (3) Low-power [15] (LP) mode, we are applying a low voltage to n-type FinFET and high voltage to p-type FinFET. This varies the threshold voltage of the devices which reduces the leakage power dissipation at the cost of increased delay. A hybrid IG/LP-mode is a combination of LP and IG modes.

The inverter implementation of each of the above three modes is shown in Figure 6. Figure 6 (a) depicts shorted-gate (SG) mode inverter in which both transistor p-type FinFET and n-type FinFET back gates are connected its front gate; this configuration is best suitable for high-performance applications. In low-power (LP) mode inverter configuration [Figure 6 (b)], p-type FinFET back gate is biased at high ( $V_{high} = 1V$ ) and n-type FinFET back gate is reverse biased at low ( $V_{low} = -0.2V$ ), back gate applied potential changes the threshold voltages of the both FinFETs, which is requisite for low-power applications at a cost of increased delay. Figure 6 (c) and (d) are independent-gate n-type FinFET and P-type FinFET inverter configurations respectively, in 6 (c) p-type FinFET both gates are tied together and in n-type FinFET back gate is biased at low ( $V_{low} = -0.2V$ ), in 4 (d) n-type FinFET both gates are tied together and in p-type FinFET back gate is biased at high ( $V_{high} = 1V$ ) respectively. The last two configurations are mixed of prior two compositions.

Inception of each of the above three modes of a NAND gate circuits is shown in Figure 7. In shorted-gate (SG) mode NAND [shown in Figure 7 (a)] both p-type FinFET and n-type FinFET transistors back gates are connected to their front gates; this composition is best suitable for high-performance applications. Figure 7 (b) shows the Low-power (LP) mode NAND gate; in which both p-type FinFET back gates are biased at high potential and n-type FinFET transistors back gates are biased at low potential. Figure 7 (c) shows the IG-mode NAND gate; in which single p-type FinFET transistor has connected to two input signals (one input at the front gate and other at back gate) and the rest of the two n-type FinFET transistors connected in SG mode. This design results in a reduction of one p-type FinFET and is conducive in area significant designs. At IG/LP mode NAND gate [Figure 7 (d)], single p-type FinFET transistor is connected to two input signals (one input at the front gate and other at back gate) and n-type FinFET transistors back gates are biased at low potential. This type of composition is also adequate in area efficient design.

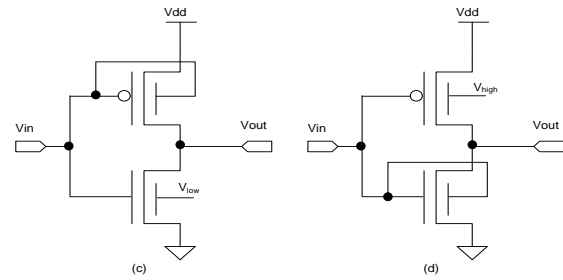
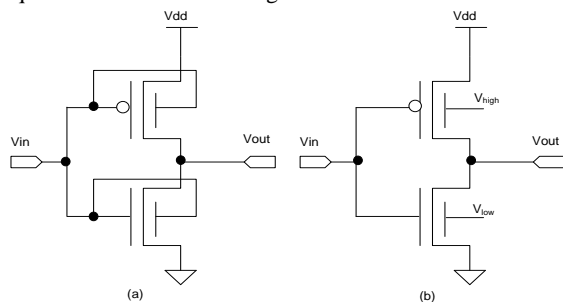


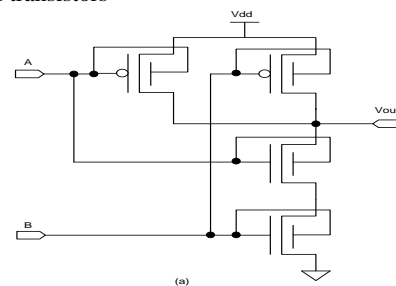
Figure 6 Different modes of Inverter circuits (a) Shorted-gate (b) Low-power (c) Independent-gate-n (d) Independent-gate-p

#### 5. SIMULATION RESULTS AND DISCUSSION

In this section, we present simulation results of 32nm FinFET, delay calculation of the inverter and NAND gates of different mode using sentaurus TCAD. The doping profile of double-gate (DG) n-channel FinFET and p-channel FinFET has shown in Figure 8 and Figure 9, respectively. As shown in Figure 8 and Figure 9, source and drain region doping concentration is  $1 \times 10^{20} \text{ cm}^{-3}$ , extension region doping is  $1 \times 10^{19} \text{ cm}^{-3}$ , channel doping is  $1 \times 10^{15} \text{ cm}^{-3}$ , respectively. An important FinFET characteristic is a threshold voltage ( $V_T$ ) controllability. The ( $V_T$ ) at each gate can controlled through the application of a voltage at the other gate. The threshold voltage controllability is a powerful tool for circuit optimization. Figure 5 shows the threshold voltage ( $V_T$ ) variation of a n-type FinFET device with different back gate bias voltages.

The transient characteristics of an inverter driving another inverter circuit having the waveform of input/output and the dynamic (short-circuit) current through the active (n-type FinFET or p-type FinFET) device during inverter switching operation is shown in Figure 10. The short-circuit power dissipation in the inverter circuit is because of short-circuit current flowing through the respective (i.e., n-type FinFET or n-type FinFET) active device and which is maximum during the switching operation. Thus, leads to heating of the device.

Figure 11 shows the transient input/output characteristics of NAND gate, there is no threshold voltage loss at the output. All design modes of gates are simulated with minimum size,  $T_{PHL}$  and  $T_{PLH}$  are calculated for each mode and the average delay is tabulated in Table 3. From the Table 3, we can observe that SG-mode NAND and INVERTER gates takes lesser delay than other modes of NAND and INVERTER gates. Thus, the SG - mode is conducive in high-performance design. LP-mode NAND and INVERTER gate takes more delay and we observed that lesser the leakage current, so we use this mode in low-power design. The IG - mode is moderate in delay-power and takes a lesser number of transistors



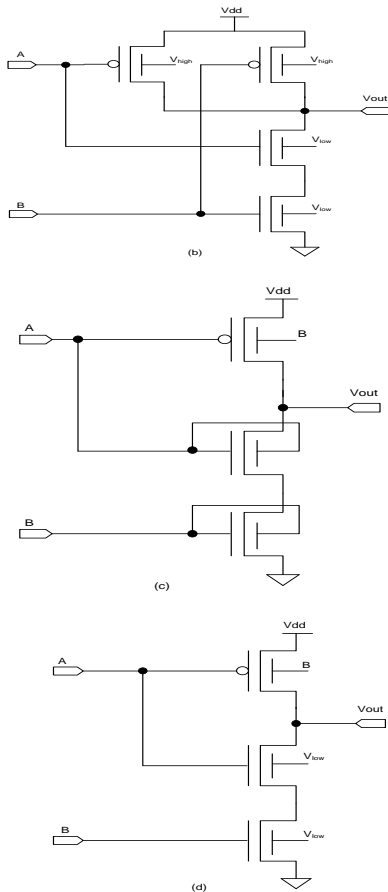


Figure 7 Different FinFET based NAND gate designs (a) SG-mode NAND (b) LP-mode NAND (c) IG-mode NAND (d) IG/LP-mode NAND

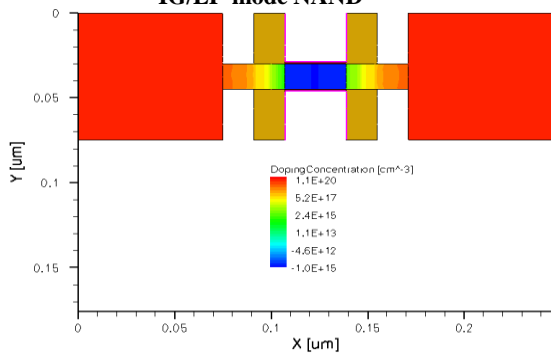


Figure 8 Double-gate (DG) n-type FinFET Doping concentrations of gate length  $L_G = 32$  nm

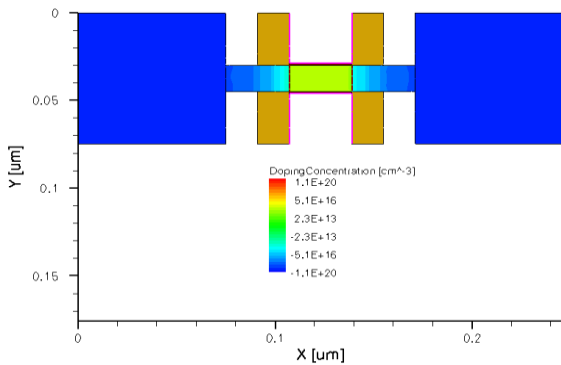


Figure 9 Double-gate (DG) p-type FinFET Doping concentrations of gate length  $L_G = 32$  nm

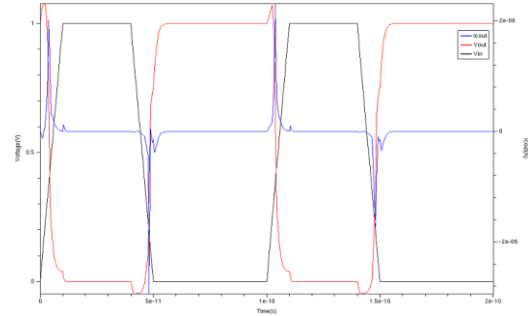


Figure 10 Transient input/output characteristics of inverter driving another and dynamic (short-circuit) current through the active device during the inverter switching operation.

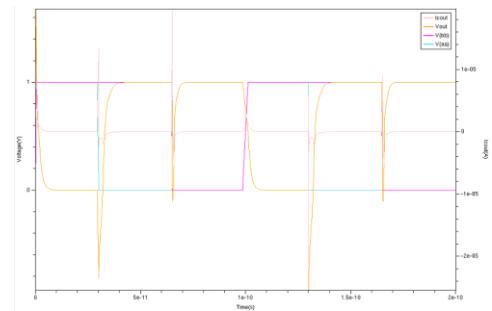


Figure 11 Transient input/output characteristics of NAND gate driving another NAND gate and dynamic (short-circuit) current through the active devices during the switching operation.

Table 3  
Delay measurement of FinFET based gates

Design-mode	Delay (ps)
INV-SG	2.156
INV-LP	2.955
INV-IGn	2.250
INV-IGp	3.130
NAND-SG	2.161
NAND-LP	3.250
NAND-IG	2.340
NAND-IG/LP	3.400

## 6. CONCLUSION

In this paper, double-gate (DG) FinFET device of n-type and p-type has been simulated using sentaurus TCAD and its various characteristics are plotted. Back gate is used to control the threshold voltage ( $V_T$ ) of the front gate, which is very important for the performance of the circuit. This is helpful in optimization of different circuits in terms of delay, area and power. The simulation of different modes of INVERTER and NAND gates with 32nm FinFET shows that, we can get a minimum delay in SG mode, low power is obtained in LP configuration at the expense of increased delay while in IG mode we can give the inputs to the two different gates and the number of devices in a circuit can be reduced, reducing the area requirement of the circuit. An IG / LP mode is a mix of IG and LP modes and results in low leakage, reduced area and higher delay.

This also shows that FinFETs are the answer for technological scaling beyond 45 nm technology and results in the lower delay.

## 7. ACKNOWLEDGMENT

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