Active Inductor Based Low Noise Amplifier for Ultra Wide Band Receiver

V. Vaithianathan
Assistant Professor
Dept. of ECE
SSN College of Engineering Chennai, India

R. Srinivasan
Professor
Dept. of IT
SSN College of Engineering Chennai, India

J. Raja
Professor
Dept. of ECE
Anna University of Technology, Trichy, India

M. Chandra Praveen
PG Student
Dept. of ECE
SSN College of Engineering, Chennai, India

ABSTRACT
In this paper a three stage Active Inductor (AI) based Low Noise Amplifier (LNA) for Ultra Wide Band (UWB) receiver is presented. A fully differential topology has been adopted in order to improve the circuit robustness against unwanted common mode signals. T-coil peaking is used to enhance the bandwidth over the entire Ultra Wide Band frequency range. Active inductor is employed because of its low area, tunable inductance and high quality factor. Simultaneous Noise and Impedance Matching (SNIM) is employed to reduce the noise figure of the design. Resistive source degeneration has been implemented to improve the linearity of the circuit. The proposed LNA is designed using 90nm CMOS technology. The proposed LNA achieves power gain (S_{21}) greater than 12dB throughout the UWB spectrum providing a bandwidth of 4 – 11 GHz. The input matching (S_{11}) and output matching (S_{22}) are kept well below -10 dB and – 8dB respectively, while the reverse isolation (S_{12}) is less than -43 dB providing a linearity of -6.9 dBm. Upon adoption of SNIM the Noise Figure falls in the range 4.4 - 8.2 dB.

General Terms
Full Custom Design, RF VLSI

Keywords
Power Gain, Simultaneous Noise and Impedance Matching, Noise Figure, Resistive Source Degeneration, Third Order Input Intercept Point,

1. INTRODUCTION
Rapid growth and demand in wireless devices for higher capacity, faster service, and more secure wireless connections initiates the development of new wireless standards. The ultra wide band (UWB) technology is a promising solution for low cost, high data and short range wireless applications. UWB radio transceivers can legally operate in the range from 3.1GHz to 10.6GtHz at a limited transmit power spectral density of -41.3dBm. UWB achieves wide bandwidth through its implementation by means of "impulse" signal rather than using conventional RF carrier signals. The UWB systems find applications in the areas of ground penetrating radars, imaging and surveillance systems, safety/health monitoring and wireless home video data links.

There are two types of UWB Communication systems. The DS-UWB [1] uses nano second pulses and time-domain signal processing combined with DS spread spectrum techniques to transmit and receive information. As shown in Fig. 1, the entire band is divided into lower and upper bands. The lower band occupies the spectrum in the range of 3.1 GHz to 4.85GHz while the upper band falls in the range of 6.2GHz to 9.7GHz. It provides a data rate of 28 to 1320 Mb/s within the transmission bands.

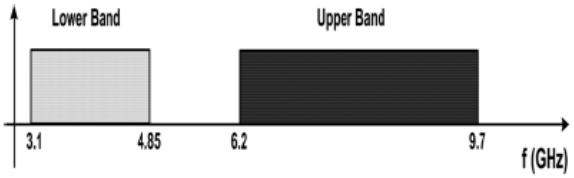

Fig 1: DS UWB

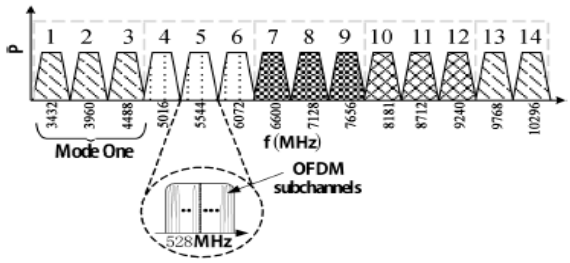

Fig 2: MB-OFDM UWB

MB-OFDM transmits information over multiple carriers. The MB-OFDM based UWB technique uses the whole spectrum by dividing it into 14 bands [2]. This is organized into five groups with each group having bandwidth greater than 500 MHz. The operation within the first group is mandatory, while all the other groups are optional. This is illustrated in Fig. 2.

Being the first signal processing element in the analog front-end circuits, serious challenges exist for the realization of LNA. The received UWB signal exhibits very low Power-Spectral Density (PSD) at the receiver antenna. The primary goal of LNA is to amplify the weak signal received from the antenna with less distortion and little self generated noise [3]. Major metrics used to measure the performance of LNA are reduced noise figure, moderated gain, input & output impedance matching, low power consumption, isolation between input and output, acceptable linearity (low distortion) and stability.

Inductors synthesized using active devices is known as Active Inductors [4]. It offers a number of unique advantages over their spiral counterparts including less chip area requirement,

large and tunable inductances with large inductance tuning ranges, large and tunable quality factors, high self-resonant frequencies, and full compatibility with digital oriented CMOS technologies. Active inductors have found increasing applications in high-speed analog signal processing and data communications where spiral inductors are usually employed. Several Active Inductors have been discussed for achieving high quality factor, high inductance and reduced noise figure in [4].

Most of the recent designs of LNA using CMOS technology have focused on achieving an optimal performance metrics with some tradeoff through different topologies. The cascode topology with inductive source degeneration provides good noise figure, good linearity with moderate gain [5]. The shunt-series peaking for common source amplifier provides good gain, reduced noise figure and low power consumption. But it does not provide wide bandwidth [6].The CG amplifier topology [7] achieves wideband input matching and better input-output isolation. But it exhibits high noise figure and low power gain. The resistive shunt feedback amplifier employed in [8] provides a low power gain and high noise figure. The resistive shunt feedback amplifier faces a tough task for providing high gain and low noise figure simultaneously while satisfying impedance matching [8]. Several Linearity enhancing techniques such as Multiple Gated Transistor, optimum biasing, Derivative Superposition and Feedback techniques has been investigated in [9].

This paper focuses on a three stage differential LNA for UWB. T Coil peaking technique is used to achieve bandwidth over the entire frequency range. Section 2 discusses the operation of the SNIM technique, T-coil Peaking and proposed LNA with its equivalent circuit. In Section 3, operation of the used Differential Active Inductor [10] is discussed. One of the passive inductor in the proposed LNA is replaced by the Differential Active Inductor. The simulation results of the proposed LNA with and without Active Inductor are discussed in Section IV.

2. LOW NOISE AMPLIFIER

2.1 Simultaneous Noise and Impedance Match

Resistive termination and negative parallel feedback are the general methods employed to provide 50Ω input matching. Presence of resistor in both these approaches affects the noise figure of the amplifier. As first stage of the design provides major contribution to the overall system noise figure resistive network at the input stage can be avoided. So, inductive source degeneration (L_s) as illustrated in Fig. 3 can be used to present a 50Ω input resistance [11]. The inductance controls the input resistance of the circuit. It uses the inductor L_S to generate the real impedance to match the input impedance to 50Ω, which results in good noise performance.

To have a good input matching, input impedance should be equal to source resistance. i.e. input impedance should have only real term. As gate-to-source capacitance mainly depends on the device size, the imaginary terms rarely tend to cancel. So a small gate inductor L_g in series with the gate can be added to cancel the imaginary term. From the small signal analysis as shown in Fig. 4 of the inductive source degeneration model shown above, the input impedance is given as (1)

$$Z_{in}^{'} \approx \left(sL_g + \frac{1}{sC_{gs}} \right) \| \, sL_s \qquad (1)$$

where C_{gs} and g_m are Gate-to-Source capacitance and transconductance of the transistor respectively.

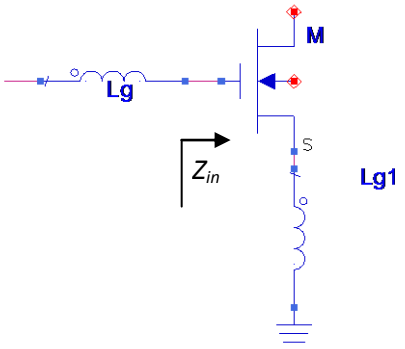

Fig 3: Simultaneous Noise and Impedance Matching (SNIM)

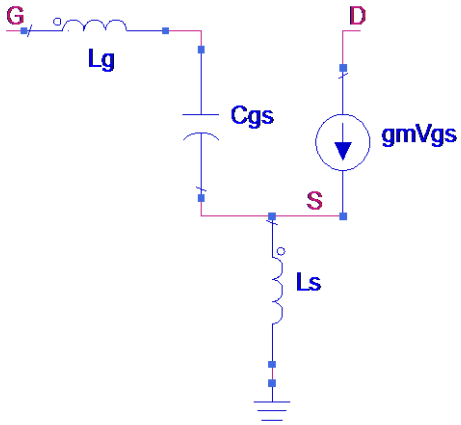

Fig 4: Small signal equivalent of SNIM

By providing suitable values of L_g, imaginary terms gets cancel. Selecting these inductors provides a power match, and also can provide a noise match. In general noise figure of a two port device is given by (2)

$$F \approx F_{\min} + \frac{R_n}{G_s} \left| Y_s - Y_{opt} \right|^2 \qquad (2)$$

where $Y_s = G_s + jB_s$ is the source admittance
$Y_{opt} = G_{opt} + jB_{opt}$ is the optimum source admittance
R_n is the equivalent noise resistance of transistor
G_s is the real part of source admittance

Transistor size is chosen in such a way that the real part of optimum input admittance (G_{opt}) is equal to the source admittance ($1/Z_o$). In this case, optimum source admittance for noise is equal to optimum source admittance for power matching, and we will have simultaneous noise and impedance match. So SNIM have been added in the first common gate stage to provide impedance and noise matching.

2.2 T Coil Bandwidth Enhancement

Peaking Techniques and distributed amplification are the generally used techniques for bandwidth extension in wideband amplifiers. Depending on the placement of the coil,

inductive peaking can be achieved in many ways. T Coil peaking is a combination of a shunt and double series peaking method [12, 13, 14]. The mutually coupled inductors form a letter T and it gains the name T Coil Peaking. It has highest Bandwidth Enhancement Ratio of about 2.72 when compared with other bandwidth extension techniques. A bridging capacitance can also be introduced between the inductors to improve the performance. The simplified schematic of the T Coil Peaking is shown in Fig.5

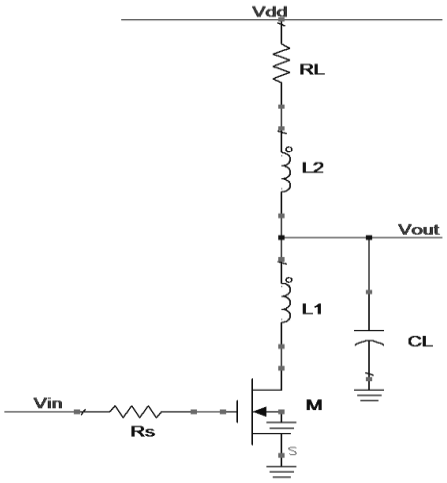

Fig 5: Simplified Schematic of T Coil Peaking

Both the inductor L_1 and L_2 blocks the flow of current into the load resistor and hence the charging of the load capacitance increases. But transistor should also have to drive its own output capacitance for some time. Hence rise time at the drain improves. This action leads to improved bandwidth. So we have employed Asymmetric T Coil peaking (L_1 and L_2 are not equal) in all the three stages to improve the bandwidth of our design.

2.3 Resistive Source Degeneration

Linearity depicts a circuit's ability to handle large signals. Very large signals cause desensitization and affect the dynamic range of the circuit. It results in gain compression. For a MOS transistor operated in saturation region, the small-signal drain current can be expressed as in equation (3)

$$i_d(V_{gs}) = g_1 V_{gs} + g_1 V_{gs}^2 + g_1 V_{gs}^3 + ... \quad (3)$$

where g_i is the transconductance of i^{th} order derivative.

As SNIM technique is employed, it results in mixing of the 2nd order harmonic component and fundamental component due to addition of source inductance (L_{s1} and L_{s2}) at the source of the transistor. This will affect the performance of the LNA when the source impedance is purely inductive. So the linearity of this circuit can be improved by adding resistors (R_7, R_8, R_9, R_{10}) at the source of the transistor [15, 16]. Introduction of this resistor slightly affects the gain of the amplifier while providing improvement in linearity.

2.4 Proposed Low Noise Amplifier

The proposed UWB LNA consists of three stages with asymmetric T coil peaking for bandwidth enhancement. A fully differential topology has been adopted because of its noise reduction properties and its ability to achieve a wide dynamic range at the cost of increase in power consumption with respect to a single-ended implementation. The first common gate stage (M_1, M2) provides a wideband input impedance matching and moderate gain with poor noise properties. So SNIM have been employed in the first stage. Since the common gate stage does not provide the adequate gain, two common source stages (M_3, M_4 & M_5, M_6) have been inserted as subsequent amplifier stages and T Coil peaking method is used in all the three stages to achieve bandwidth over the entire UWB spectrum. Because of the adopted SNIM technique, the linearity of LNA is affected due to interaction of the Intermodulation products. So resistive source degeneration is adopted in the gain enhancing two common source stages to achieve good linearity. The simplified schematic of the proposed UWB Differential LNA is shown in Fig 6.

2.5 Analysis and Design

The wideband input matching is achieved by the first common gate stage. The dimensions of the input transistors, L_s and L_g are chosen in such a way that they provide an input matching of 50Ω. The equation for the input impedance is obtained from the small signal equivalent circuit as shown in Fig. 7 is given by (4)

$$Z_{in} \approx \left(sL_{s1} \parallel \left(\frac{1}{sC_{gs1}} + sL_{g1} \right) \right) + \left(sL_{s2} \parallel \left(\frac{1}{sC_{gs2}} + sL_{g2} \right) \right) \quad (4)$$

where L_1 - Effective inductance of the T Coil L_{11} and L_{21},
L_2 - Effective inductance of the T Coil L_{12} and L_{22}
L_3 - Effective inductance of the T Coil L_{13} and L_{23}
L_4 - Effective inductance of the T Coil L_{14} and L_{24}
L_5 - Effective inductance of the T Coil L_{15} and L_{25}
L_6 - Effective inductance of the T Coil L_{16} and L_{26}
C_{gs1}- Gate-to-Source capacitance of the Transistor M_1

The T-coil network used in the output stage performs the wideband output matching as well as enhancing the R provide the linearity improvement at the output stage. This network is chosen in such a way to provide 50Ω impedance matching as shown in Fig. 8 and is given by (5)

$$Z_{out} \approx s(L_5 + L_6) + R_5 + R_6 \quad (5)$$

Gain-bandwidth product is a technology constant dependent on the process technology used. The main constraint in design of wideband amplifier is to achieve large gain and wide bandwidth simultaneously. One potential alternative to overcome this problem is to distribute gain on many stages. So, two common source stages are added subsequently in order to increase the gain of the amplifier. The gain of this LNA is given by (6).

$$A_{vd} \approx g'_{m1} g'_{m2} g'_{m3} Z_1 Z_2 Z_3 \quad (6)$$

where $Z_1 \approx r_{ds1} + r_{ds2} + sL_1 + sL_2 + R_1 + R_2$
$Z_2 \approx r_{ds3} \parallel [sL_3 + R_3] + r_{ds4} \parallel [sL_4 + R_4]$
$Z_3 \approx r_{ds5} \parallel [sL_5 + R_5] + r_{ds6} \parallel [sL_6 + R_6]$

Here, g'_{m1}, g'_{m2} and g'_{m3} are the effective transconductances of the first, second and third stages respectively. The passive inductor L_{16} is replaced by the following active inductor and the simulation results have been analyzed.

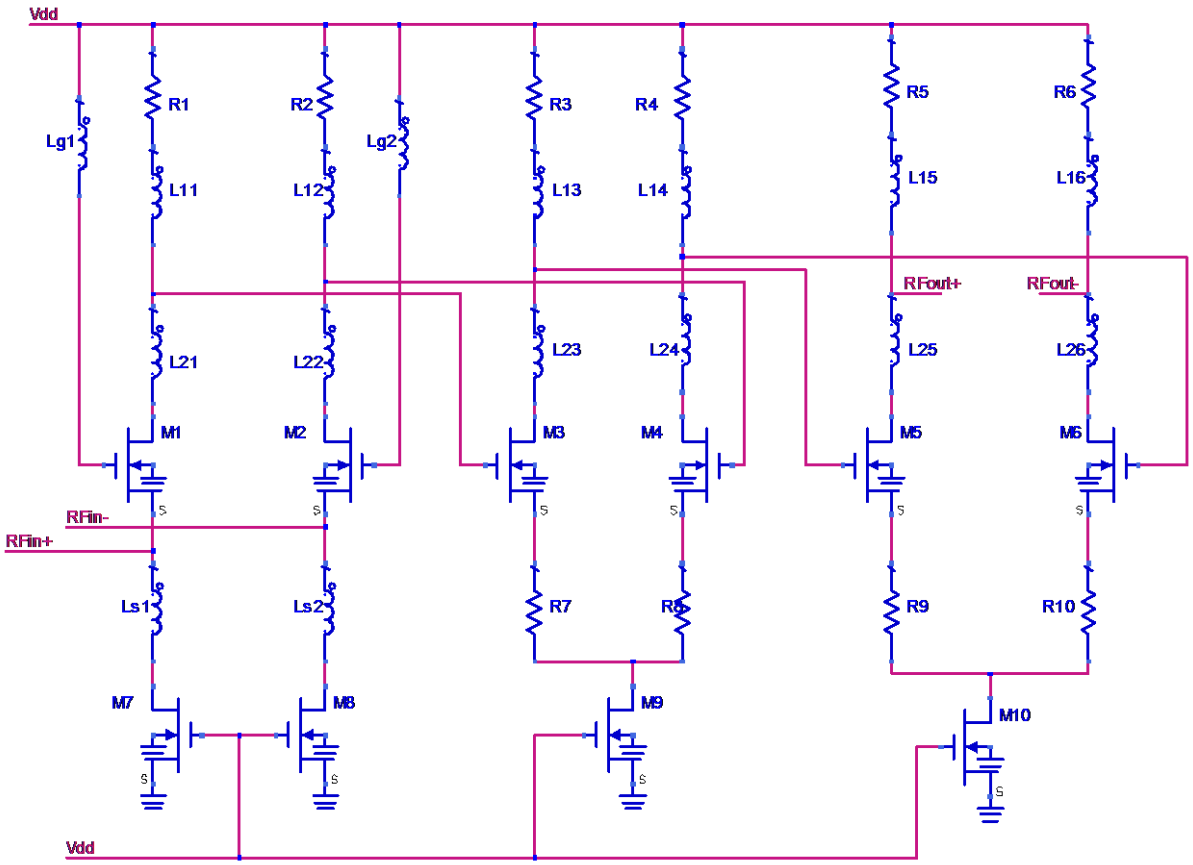

Fig 6: Proposed Differential LNA

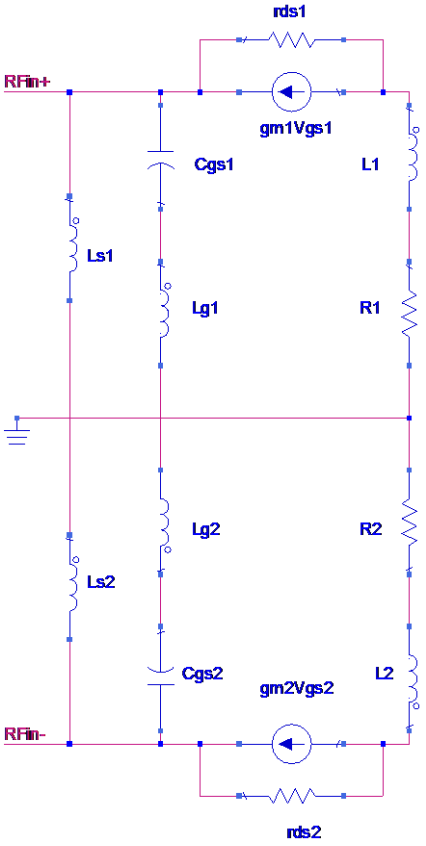

Fig 7: Equivalent Circuit of CG Stage

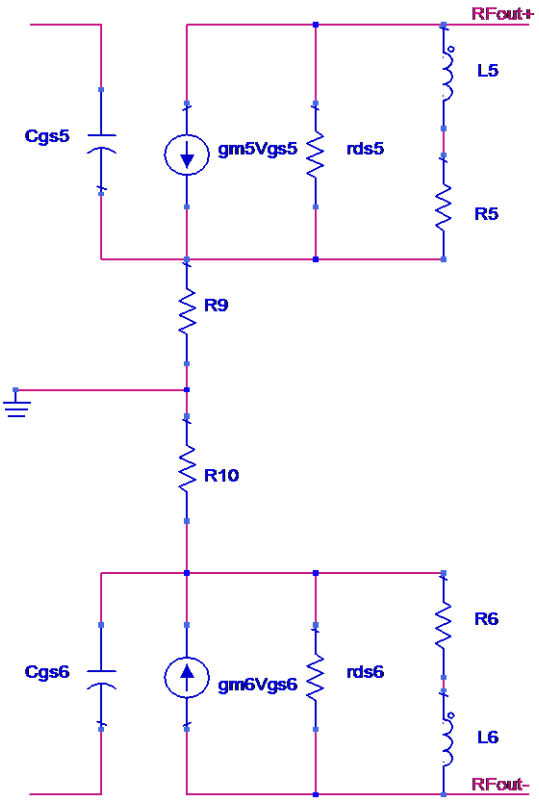

Fig 8: Equivalent Circuit of CS Stage

3. ACTIVE INDUCTOR

The Differential Active Inductor as shown in Fig 9, proposed in [10] has been used to replace the passive inductor (L_{16}) in the proposed LNA. Simple gyrator can be visualized as a differential circuit as it requires input signals of opposite sign. M_{2a} and M_{2b} act as the core circuit whereas a pair of stabilizers (M_{3a} and M_{3b}) and negative impedance cross coupled MOSFET pair (M_{1a} and M_{1b}) has been utilized in order to remove the instability problem. The Q factor is affected by inductance tuning due to non-linear nature of active inductor. So a pair of current sinks (M_Q) is introduced to eliminate this effect. In order to control the current flow, one branch of the differential circuit is used as a current mirror. This leads to low current dissipation because of current reuse technique. This active inductor proposed in [10] is designed to produce inductance in the range of 1.5nH-3nH throughout the desired UWB range.

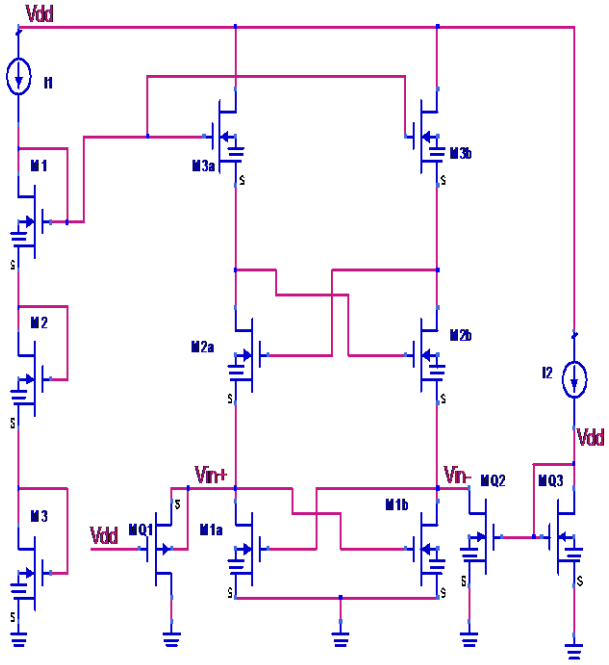

Fig 9: Differential Active Inductor

The Inductance and Quality Factor has been calculated using the formula given in (7) and (8) respectively.

$$L_d = \frac{imag(Z_d)}{\omega} \qquad (7)$$

$$L_d = \frac{imag(Z_d)}{real(Z_d)} \qquad (8)$$

$$Z_d = Z_{11} - Z_{12} - Z_{21} - Z_{22}$$

The simulation results of the designed active inductor are presented from Fig 10 – 12. The above designed Active Inductor has been used instead of passive inductor L_{16} in the proposed LNA and the simulation results have been analyzed in the following section.

4. SIMULATION RESULTS

The proposed LNA is simulated using 90 nm CMOS technology. The simulation results of the LNA, LNA with Active Inductor (LNA_AI) and the impact of noise reduction techniques (LNA_AI_NR) is presented in Fig. 11 through Fig.15.

Fig 10: Inductance Vs Frequency

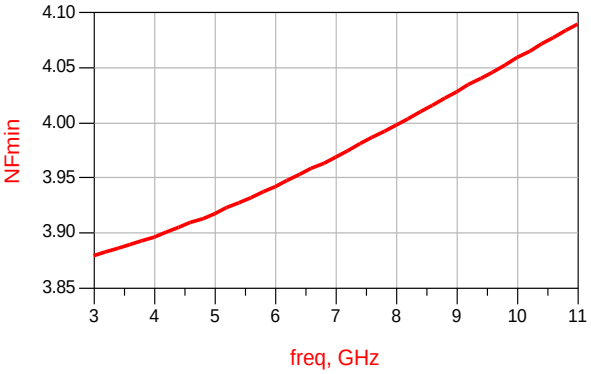

Fig 11: Noise Figure Vs Frequency

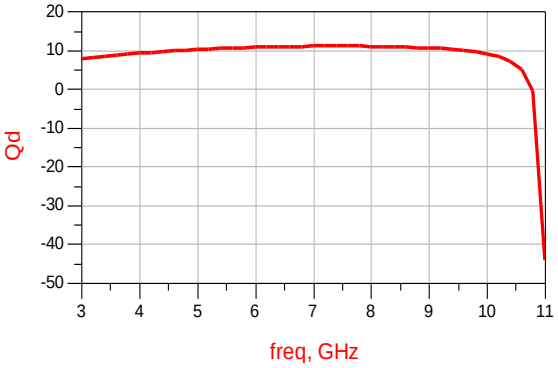

Fig 12: Quality Factor Vs Frequency

From the Fig. 13, maximum gain of 17.5 dB is achieved at 5.5 GHz while gain more than 12 dB is maintained from 3.1 GHz to 10.6 GHz in the design with Noise Reduction techniques. Usage of resistive source degeneration to enhance linearity has a direct trade off with the power gain of this circuit. The noise figure (NF) for LNA without active inductor falls in the range 6.9-9.4 dB due to increased stages .Due to addition of active inductor whose Noise figure falls in the range 3.9-4.1dB, the noise figure reaches 7.9-8.4dB in the design with active inductor. In order to circumvent the noise effect of Active inductor in the design, SNIM technique is adopted. This has resulted the noise figure to fall between 4.4 – 8.2 dB

as illustrated in Fig. 14. From the Fig. 15, this circuit claims the desired input matching (S_{11}) of less than – 12 dB over the entire UWB range with SNIM technique.

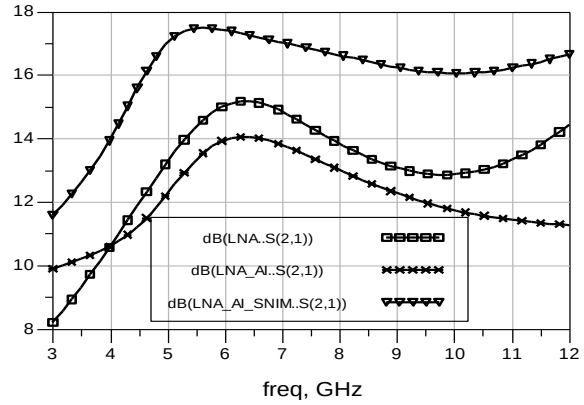

Fig 13: Power Gain (S_{21})

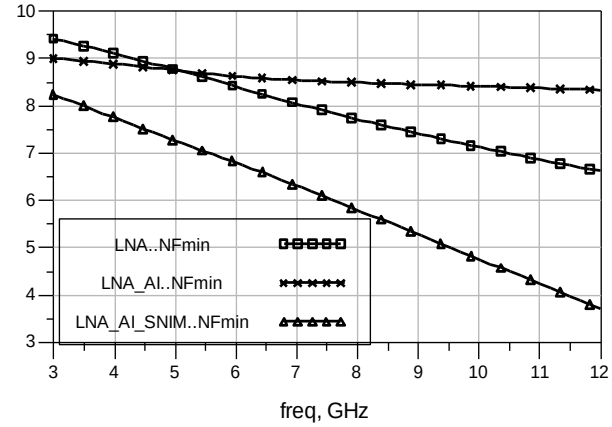

Fig 14: Noise Figure (NF_{min})

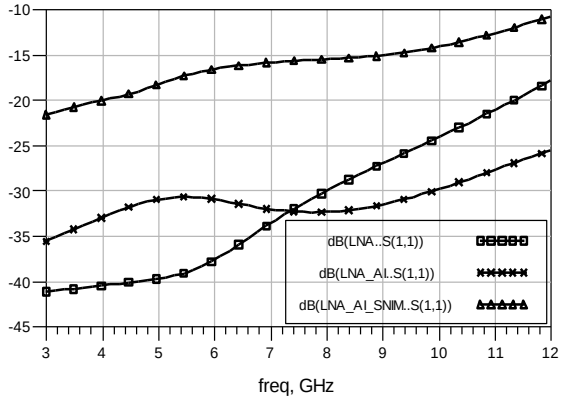

Fig 15: Input Matching (S_{11})

The output matching (S_{22}) is less than – 12dB at the lower band and reaches 20dB at 5GHz (Fig. 13).But it declines to –6 dB for upper band in the design of LNA without active Inductor. But output matching falls well below –8dB throughout the band even after adoption of noise reduction techniques in design with active inductor (Fig. 16). The reverse gain (S_{12}) is maintained well below -43dB for both the designs throughout the UWB frequency range as shown in Fig. 17. The proposed LNA consumes 14.63 mW due to increased number of stages while operating at 1V power supply. As active inductor is an active element it increases the power consumption of LNA to 16.92 mW.

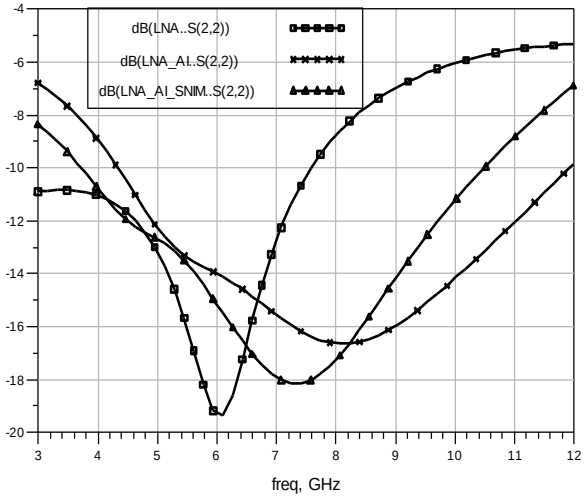

Fig 16: Output Matching (S_{22})

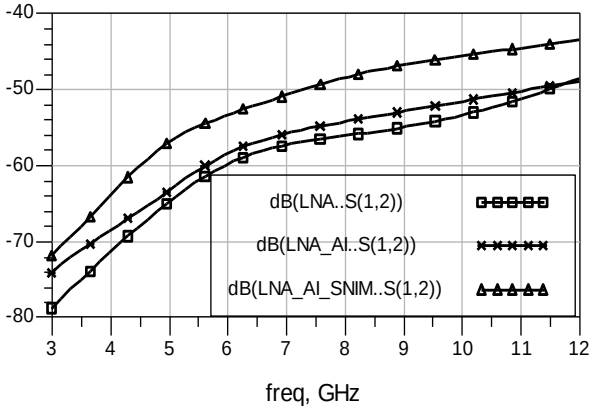

Fig 17: Reverse Isolation (S_{12})

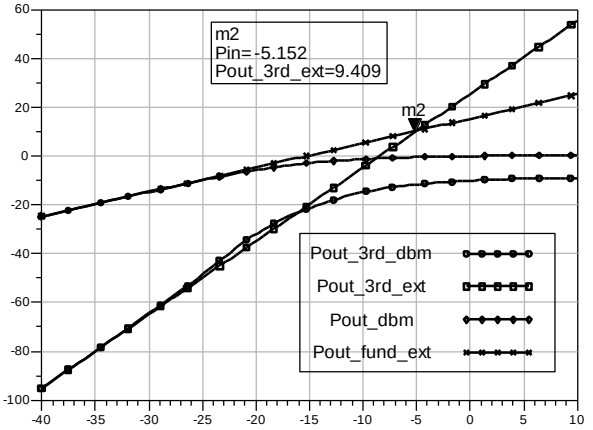

Fig 18: T-coil Linearity

Third order Input Intercept point (IIP3) is a measure used to describe the circuit's linearity. The point where the linear extrapolation of the fundamental signal equals the linear extrapolation of the 3rd order harmonic is called third order Input Intercept Point (IIP_3). After the adoption of Resistive Source Degeneration technique in the circuit, a very good linearity has been achieved with the values of – 5 dBm, - 4 dBm and – 6 dBm for LNA, LNA_AI, LNA_AI_SNIM as depicted in the Fig. 18, Fig. 19, and Fig. 20 respectively with small reduction in gain.

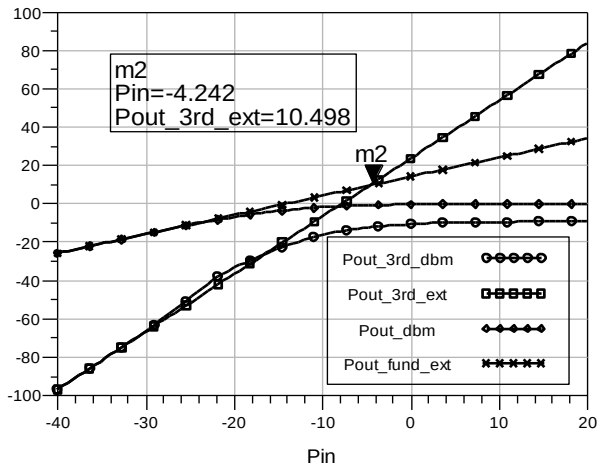

Fig 19: T-coil AI Linearity

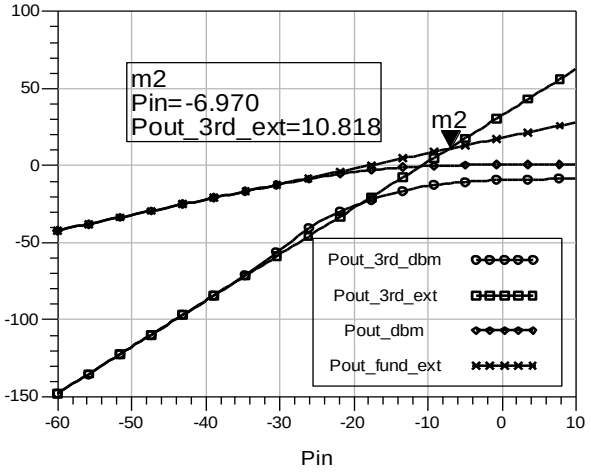

Fig 20: T-coil AI- SNIM Linearity

Table 1. Simulation Results Analysis and Performance Analysis

Parameters	**[17]**	**[18]**	**[19]**	**[20]**	***This Work (WOAI)**	****This Work(WAI)**
Technology	90nm	90nm	90nm	90nm	90nm	90nm
3-dB BW (GHz)	2-11	14.5	0.5 – 8.2	4 - 8	4-11	4 – 11
Gain S_{21}(dB)	12	10	12.5	12.2	14.5	17.5
NF (dB)	5.5-8	5.8-6	1.9 – 2.6	2 – 2.4	6.9-9.4	4.4-8.2
Input Matching S_{11} dB	< -10	< -10	- 13	< - 5	< -24	< -10
Reverse Gain S_{12}(dB)	-	-	-	-	< -49	< - 43
Output Matching S_{22} (dB)	< -10	-	< -10	< - 10	<-6	< -8
Power (mW)	17	30	42	9.2	14.63	16.92

***Without Active Inductor, ** With Active Inductor using Noise Reduction Technique**

Table 1 summarize the results achieved by the proposed LNA (With and Without Active Inductor).From the Table 1, we can claim that our proposed AI based LNA with SNIM performs better as compared to other LNAs at the cost of increase in power consumption.

5. CONCLUSION

A three stage active inductor based differential LNA is designed using 90nm CMOS technology and simulated. A power gain of more than 12dB is achieved throughout the UWB spectrum. The input matching (S_{11}) and output matching (S_{22}) are kept well below – 10 dB and – 8 dB respectively while the reverse Isolation (S_{12}) is less than – 43 dB. A single passive inductor is replaced by active inductor. Increased number of stages and active inductors lead to noise figure of about 8dB. Noise reduction techniques are used to reduce the effect of noise contributed by the active inductor and the results are compared. Resistive source degeneration in the common source stage enhances the linearity of the circuit. The power consumption of this LNA is quiet high due to increased number of stages while operating at 1V power supply. Thus the proposed LNA claims a high gain with good input and output matching providing a bandwidth of 4– 11 GHz.

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