An Efficient Design of 2:1 Multiplexer and its Application in 1-Bit Full Adder Cell

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ABSTRACT
A multiplexer, sometimes referred to as a "mux", is a device that selects between a numbers of input signals. It is a combinational logic circuit. It is a unidirectional device and used in any application in which data must be switched from multiple sources to a destination. This paper represents the simulation of different 2:1 Multiplexer Structures and their comparative analysis on different parameters such as power supply voltage, operating frequency, temperature and area efficiency etc and its application in 1 bit full adder cell. All the simulations have been carried out on BSIM 3V3 90nm technology at Tanner EDA tool.

General Terms
2:1 multiplexer, Power-delay product and Speed.

Keywords
CMOS Logic, Low power, Full adder, and VLSI.

1. INTRODUCTION
Advances in CMOS technology have led to a renewed interest in the design of basic functional units for digital systems. The use of integrated circuits in high performance computing, telecommunications, and consumer electronics has been growing at a very fast pace. This trend is expected to continue, with very important implications for power-efficient VLSI and systems designs. Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift where power dissipation has become as important a consideration as performance and area [1]. A 2-to-1 multiplexer is a basic building block of the "switch logic". The concept of the switch logic is that logic circuits are implemented as combination of switches, rather than logic gate. Multiplexers are used in building digital semiconductors such as CPUs and graphics controller, as programmable logic devices, in telecommunications, in computer networks and digital video. This paper compares the different 2:1 multiplexer structures on the basis of the power dissipation, speed, operating frequency range and their temperature dependence with the area efficiency of the circuit and its application in 1 bit full adder cell.

2. LITERATURE REVIEW OF DIFFERENT 2:1 MULTIPLEXER STRUCTURES

2.1 NMOS 2:1 Multiplexer Structure
The schematic diagram of NMOS 2:1multiplexer is shown in Fig.1. Pass transistor logic (PTL) describes several designs of circuits. Among them are CPL (Complementary Pass-Transistor Logic) and DPL (Double Pass-Transistor Logic). It is based on CPL. It reduces the count of transistors. It can only be connected to the source/drain input of another MOS transistor. This reduces the number of active devices, but has the disadvantage that output levels can be no higher than the input level [2].

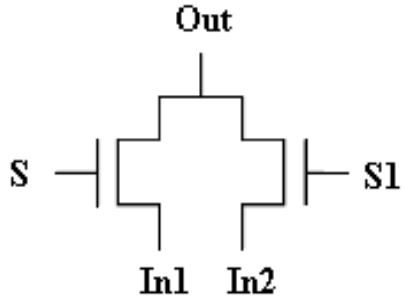

Figure 1. Schematic of NMOS 2:1 Multiplexer

2.2 MD 2:1 Multiplexer Structure
The schematic diagram of MD 2:1 multiplexer is shown in Fig.2. MD stands for multiplexer double. With the help of this circuit we find the inverted output also [3].

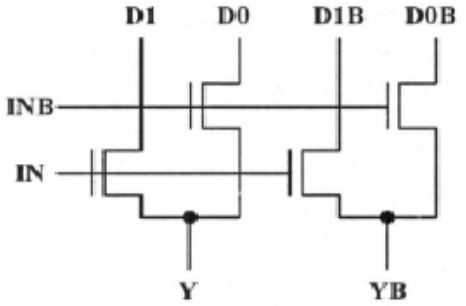

Figure 2. Schematic of MD structure

2.3 DCVSL 2:1 Multiplexer Structure
Cascode Voltage Switch Logic (CVSL) refers to a CMOS-type logic family which is designed for certain advantages. A logic function and its inverse are automatically implemented in this logic style. The schematic diagram of DCVSL 2:1multiplexer is shown in Fig.3. The pull-down network implemented by the NMOS logic tree generated complementary output. This logic family is also known as Differential Cascode Voltage Switch Logic (DCVS or DCVSL).The advantage of DCVSL is in its logic density that is achieved by elimination of large PFETS from each logic function. It can be divided it to two basic parts: a differential

latching circuit and a cascoded complementary logic array. [4]- [8]

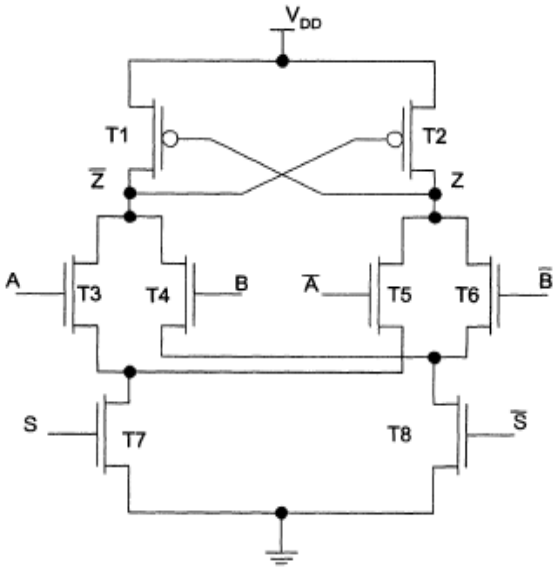

Figure 3. Schematic of DCVSL structure

2.4 MDCVSL 2:1 Multiplexer Structure

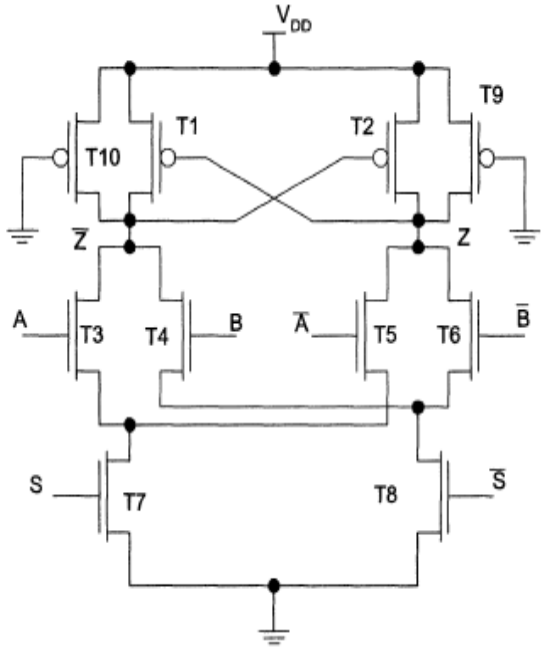

Figure 4. Schematic of MDCVSL structure

MDCVSL stands for modified differential cascode voltage switch logic. If we modify DCVSL circuit by adding two weak p channel devices i.e. transistors T9 and T10 the output of modified DCVSL 2:1 multiplexer will show better results in terms of power consumption, delay, temperature and output load capacitance and operating frequency. The schematic diagram of MDCVSL 2:1multiplexer is shown in Fig.4 [4] - [8].

3. SIMULATIONS AND COMPARISON

3.1 Simulation Environment

A simulation of various 2:1 multiplexer are done using Tanner EDA Tool version 13.0. Various 2:1 multiplexer circuits simulations are performed on BSIM3v3 90nm technology with supply voltage ranging from 0.6V to 1.4V. In order to prove that which design is consuming low power and have high performance, simulations are carried out for power, delay, power-delay product at varying supply voltages, temperatures and operating frequencies. To establish an impartial simulation circumstance, each circuit have been tested on the same input patterns which covers every possible combination of input a, b and s.

3.2 Simulation Analysis

The graph shown in Fig.5 reveals that the power consumption of DCVSL circuit is remarkably reduced than the other approaches at 90nm technology. The delays of all the circuits are shown in Fig.6. MDCVSL approach shows slightly less delay than the delay of other design for input voltage ranging from 0.6V to 1.4V. Similar results for power consumption vs. temperature and power consumption vs. output load capacitance are shown in Fig.7, Fig.8, and Fig.9 respectively at 90nm technology. As it is found from the simulations MDCVSL circuit shows better performance for the range of temperature and output load capacitance among all the other design approaches for 2:1 Multiplexers.

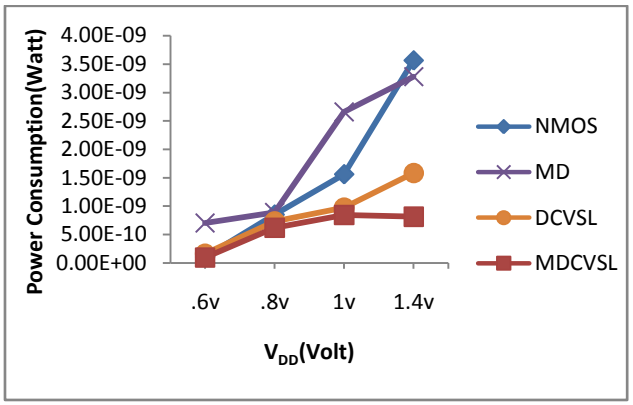

Figure 5. Power consumption comparison of various 2:1 multiplexer technologies at different supply voltages

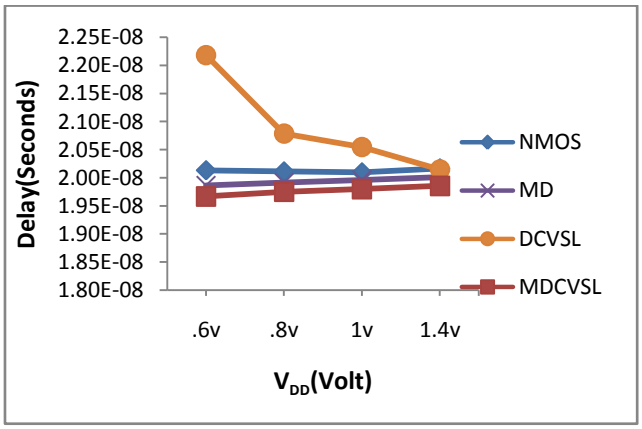

Figure 6. Delay comparison of various 2:1 multiplexer technologies at different supply voltages

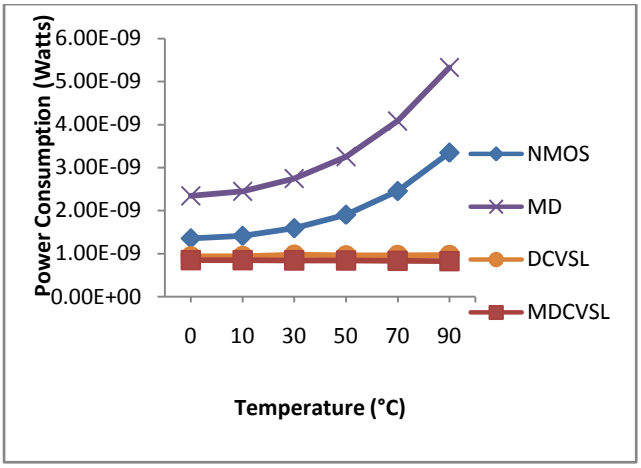

Figure 7. Power consumption comparison of various 2:1 multiplexer technologies at different temperatures

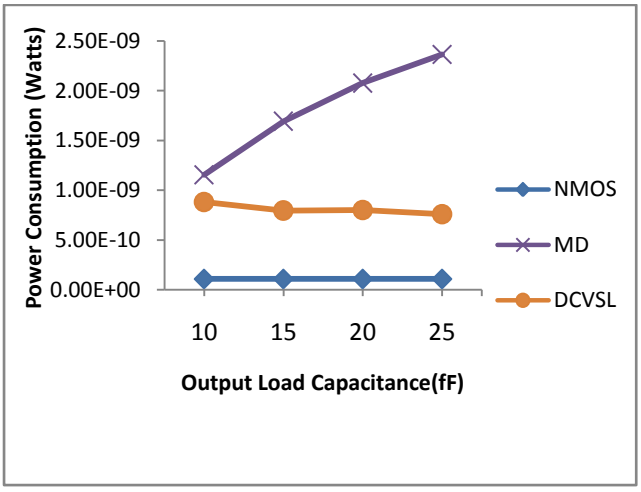

Figure 8. Power consumption comparison of various 2:1 multiplexer technologies at different output load capacitance

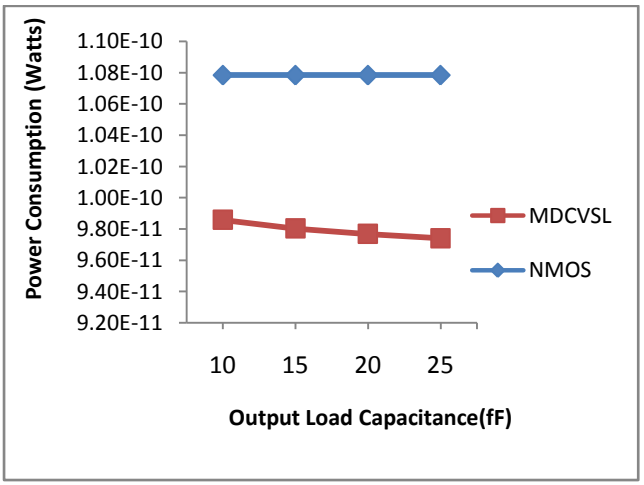

Figure 9. Power consumption comparison of various 2:1 multiplexer technologies at different output load capacitance

Table 1 show the power delay product over a range of power supply voltages and as it is shown in the table that MDCVSL circuit for 2:1 multiplexer show minimum Power delay product.

Table 1: Power delay product comparison of different 2:1 multiplexer structure

Different 2-To-1 Multiplexer Structure	Power Delay Product (90 nm) (Watt Second)			
	V_{DD}=.6v	V_{DD}=.8v	V_{DD}=1v	V_{DD}=1.4v
NMOS	2.17E-18	1.71E-17	3.13E-17	7.18E-17
MD	1.39E-17	1.76E-17	5.30E-17	6.56E-17
DCVSL	3.70E-18	1.52E-17	2.00E-17	3.18E-17
MDCVSL	**1.94E-18**	**1.22E-17**	**1.66E-17**	**1.61E-17**

4. APPLICATION OF MODIFIED DCVSL 2:1 MULTIPLEXER IN LOW POWER HIGH PERFORMANCE ADDER CELL

4.1 Adder Circuit Using NMOS 2:1 Multiplexer Circuit

Schematic of Adder circuit using NMOS 2:1 multiplexer circuit is shown in Fig.10. This design of full adder circuit is based on three transistor XOR gates and NMOS 2:1 multiplexer. In this circuit the (W/L) ratio for transistor T2 ,T5 are $(W/L)_n$=1/1 and for transistor T1, T4 are $(W/L)_p$=3/1 and for transistor T 3, T6 are $(W/L)_p$=5/1 and for transistor T7, T8 are $(W/L)_n$=7/1 [9],[10].The Boolean equations for the design of this circuit are

$$Sum = A \oplus B \oplus Ci$$
$$Cout = Cin(A \oplus B) + A \cdot B$$

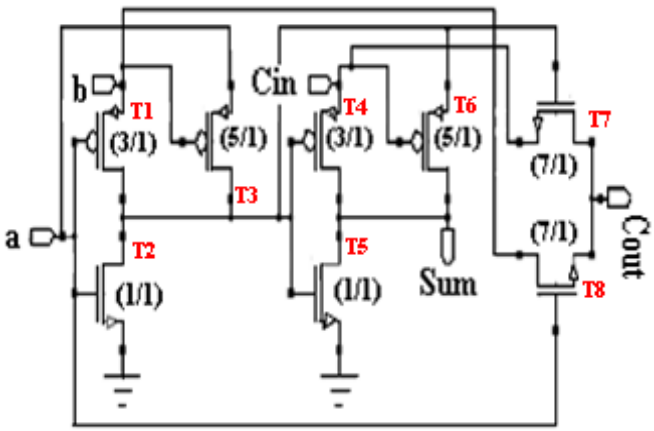

Figure 10. Schematic of Adder circuit using NMOS 2:1 multiplexer

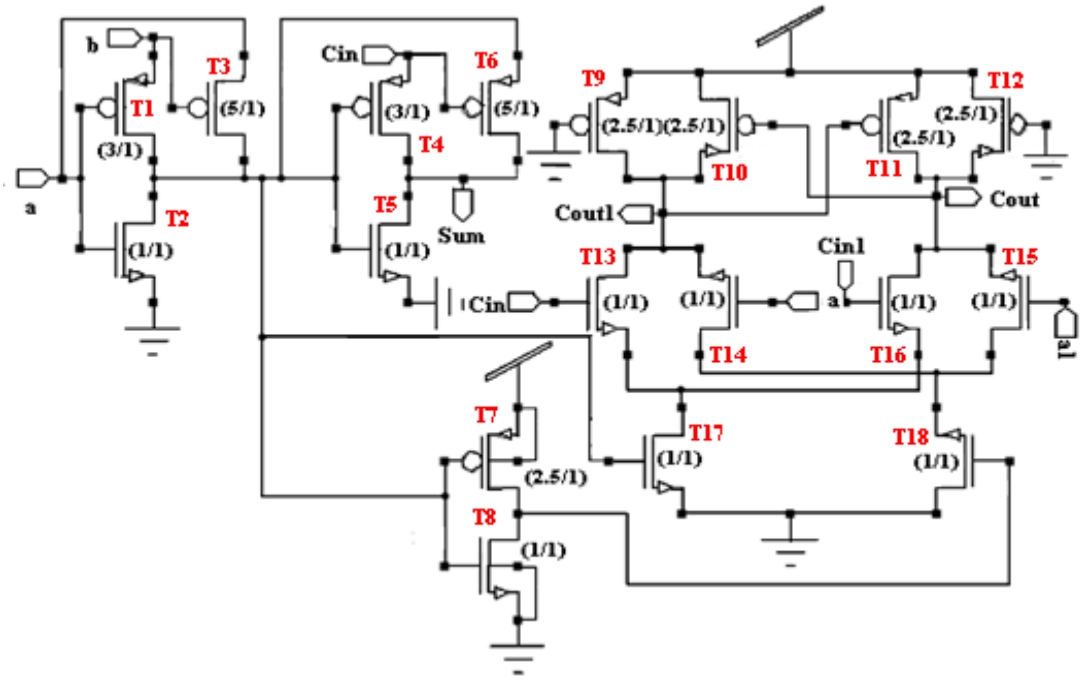

Figure 11. Schematic of Adder circuit using MDCVSL 2:1 multiplexer

4.2 Adder Circuit Using Modified DCVSL 2:1 Multiplexer Circuit

Schematic of Adder circuit using modified DCVSL 2:1 multiplexer circuit and simulated waveforms are shown in Fig.11. This design of full adder circuit is based on three transistor XOR gates and modified DCVSL 2:1 multiplexer [9],[10]. The Boolean equations for the design of this circuit are as follows:

$$Sum = A \oplus B \oplus Cin$$
$$Cout = Cin(A \oplus B) + A \cdot (A \odot B)$$

5. PERFORMANCE ANALYSIS

The graph shown in Fig. 12 - Fig. 16 reveals that the one bit full adder cell using MDCVSL technology proves superiority in terms of power delay product at varying input voltage and frequency, output load capacitance and temperature sustainability over using NMOS technology. The graph shown in Fig.12 reveals that the power consumption of MDCVSL based one bit full adder cell circuit is remarkably reduced than the NMOS based one bit full adder cell at 90nm technology. The delays of the circuits are shown in Fig.13. MDCVSL based one bit full adder cell circuit shows slightly more delay than the delay of NMOS based one bit full adder cell for input voltage ranging from 0.6V to 1.4V. Results for power consumption vs. temperature and power consumption vs. operating frequency and power consumption vs. output load capacitance are shown in Fig.14, Fig.15 and Fig.16 respectively at 90 nm technologies. As it is found from the simulations MDCVSL based one bit full adder cell is remarkably reduced than the NMOS based one bit full adder circuit shows better performance for the range of operating frequency and operating temperature and output load capacitance. Fig.17 reveal that the power consumption of the MDCVSL based one bit full adder is less than that of NMOS based one bit full adder circuit.

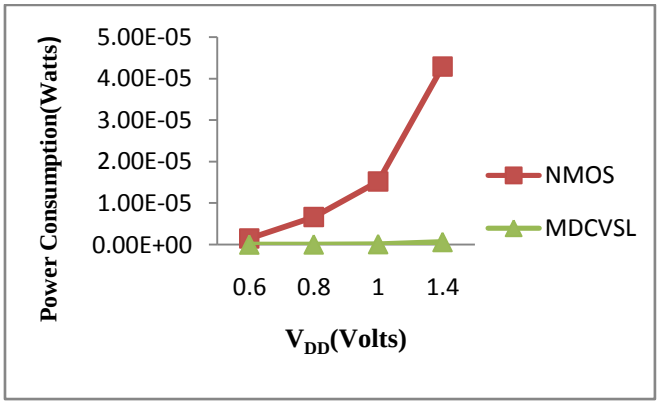

Figure 12. Power Consumption comparison of one bit full adder cell using NMOS and MDCVSL technology at different supply voltages

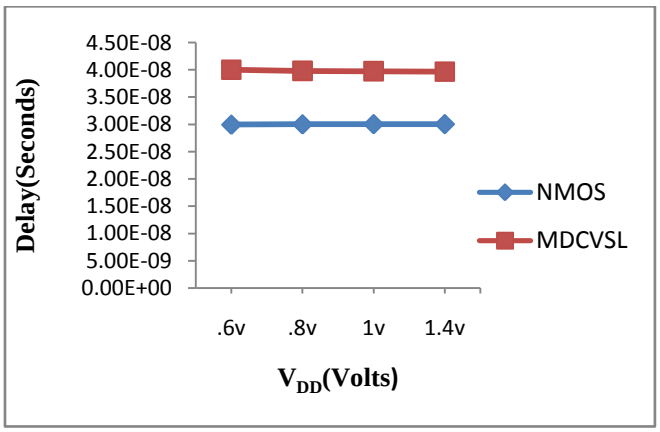

Figure 13. Delay comparison of one bit full adder cell using NMOS and MDCVSL technology at different supply voltage

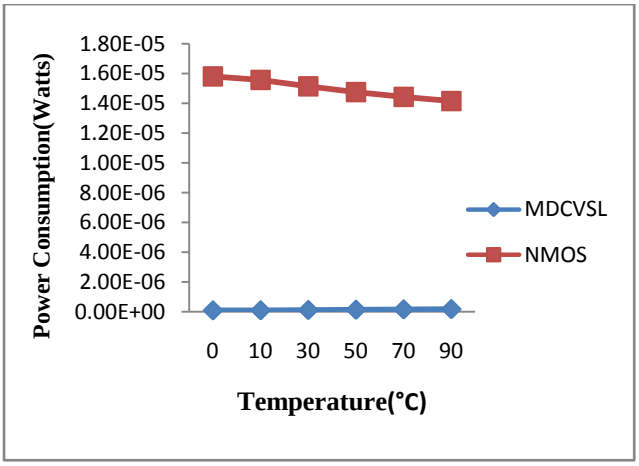

Figure 14. Power Consumption comparison of one bit full adder cell using NMOS and MDCVSL technology at different temperatures

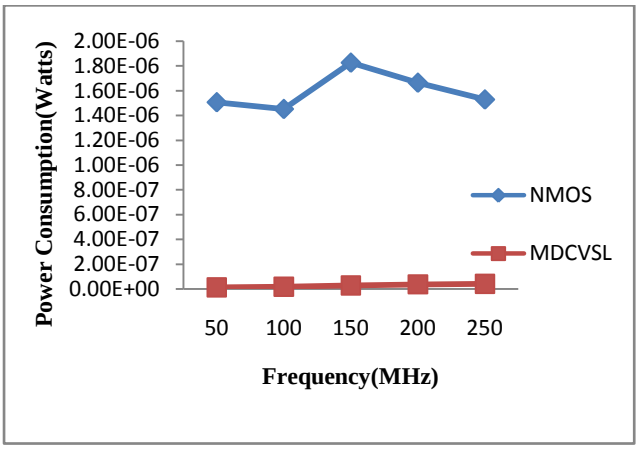

Figure 15. Power Consumption comparison of one bit full adder cell using NMOS and MDCVSL technology at different operating frequency

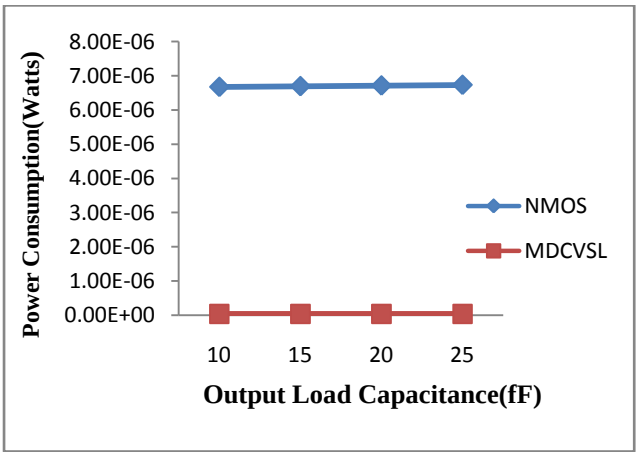

Figure 16. Power Consumption comparison of one bit full adder cell using NMOS and MDCVSL technology at different output load capacitance

Table 2. Power Delay Product Comparison of NMOS and MDCVSL based adder Cell

V_{DD} (volts)	Power Delay Product(Watt-sec) (90nm)	
	NMOS	MDCVSL
.6	4.51105E-14	5.03905E-16
.8	1.99311E-13	1.58825E-15
1	4.58125E-13	4.30337E-15
1.4	1.29024E-12	2.44445E-14

6. CONCLUSION

For low-leakage and high-speed circuits concern should be on both the factors speed and power [11]. This paper concluded with the efficient approach of multiplexer at 90nm technology. Modified Differential Cascade Voltage Switch Logic (MDCVSL) shows least power consumption over a range of power supply voltage, power-delay product, operating frequency, output load capacitance and operating temperature over other circuit design of 2:1 multiplexer. The MDCVSL based 1-bit full adder is found to give better performance than the NMOS based full adder. It shows remarkable improvement in power delay product and has better temperature sustainability. Hence, MDCVSL multiplexer based adder is suitable for lower power high-speed applications. It has a marginal increase in area compared to the NMOS multiplexer based adder; overall, we achieved the lowest power consumption and power-delay product. Fig.17 reveal that the power consumption of the proposed cell is less than that of existing one and thus proposed cell proves its superiority over existing one and hence ensuring the better performance for low power systems.

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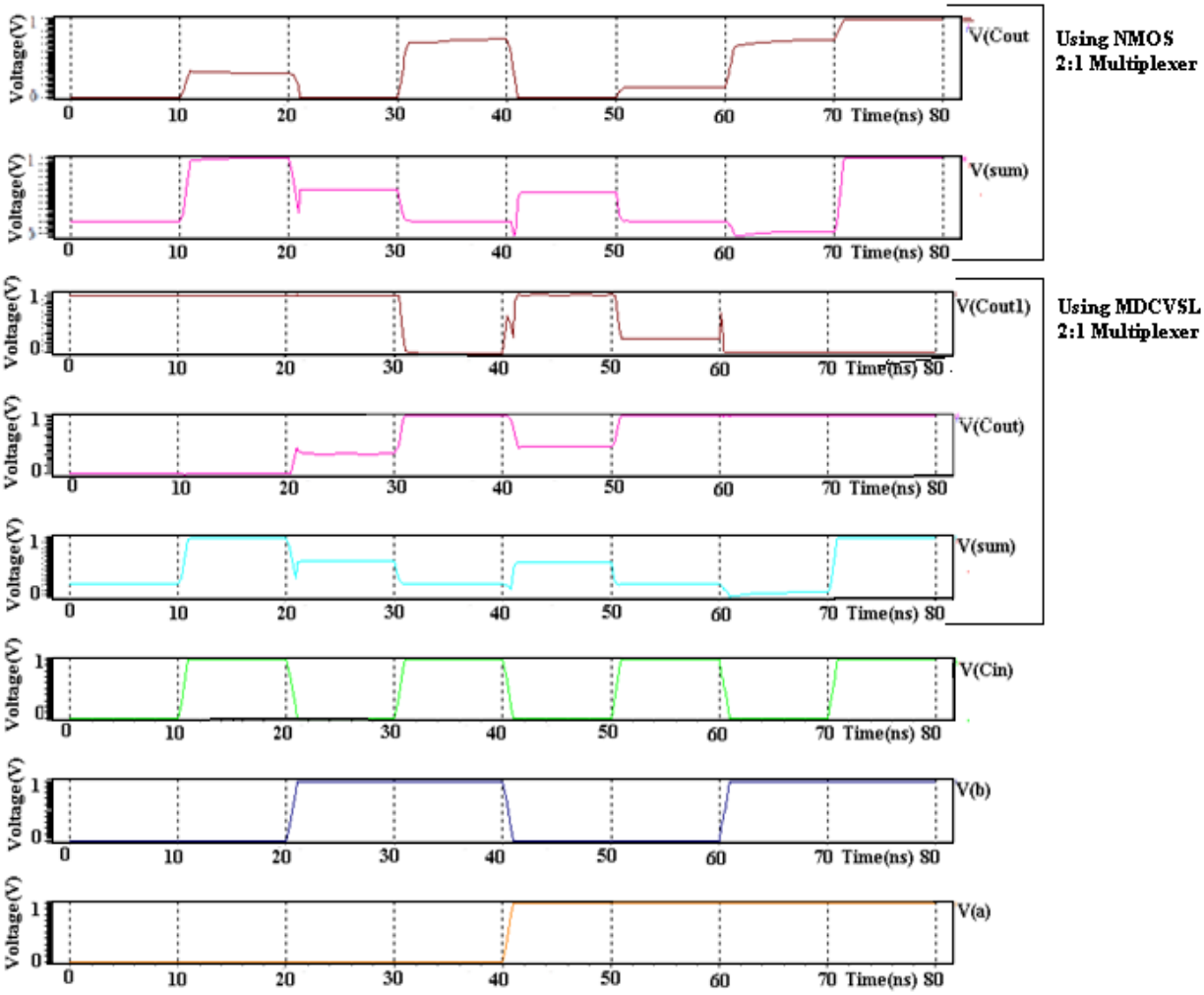

Figure 17. Simulated waveforms of Adder circuit using NMOS 2:1 multiplexer and using MDCVSL 2:1 multiplexer