Performance Analysis of Parallel FIR Digital Filter using VHDL

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ABSTRACT
With the continuing trends to reduce the chip size and integrates multichip solution into a single chip solution it is important to limit the silicon area required to implement parallel FIR digital filter in VLSI implementation. The Need for high performance and low power digital signal processing is getting increased. Finite Impulse Response (FIR) filters are one of the most widely used fundamental devices performed in DSP system. This paper presents the performance analysis of parallel FIR digital filter, In this paper, Traditional FIR filter structure and FFA based FIR filter structure and symmetric convolution based FFA FIR filter are designed for 2-parallel filter (2*2). These entire filter structures are designed based on Carry Save Adder (CSA) and Ripple Carry Adder (RCA).Exchanging multipliers with adder is advantageous because adders weight less then multipliers in terms of silicon area. The performance of parallel FIR filter structure based on Ripple Carry Adder and Carry Save Adder will be compared.

General words

Ripple Carry Adder (RCA), Carry Save Adder (CAS), Multiple Input Multiple Output (MIMO).

Keywords

Digital Signal Processing (DSP), Fast Finite Impulse Response (FIR) Algorithms (FFA), Parallel FIR, Very Large Scale Integration (VLSI).

1. INTRODUCTION
Finite Impulse Response (FIR) filter is one of the fundamental processing elements in many digital signal processing (DSP) system. Ranging from wireless communication to video and Image Processing. FIR filter must be operate at high frequency. In MIMO (Multiple Input Multiple Output) systems request high throughput FIR filter. Parallel processing is a well known technique for finite impulse response (FIR) digital filters, which increases the throughput, and decreases the power consumption by lowering the supply voltage [1].

However due to its linear increase in the hardware implementation cost brought by the increase of block size "L". The Parallel Processing technique lost its advantage to be employed in practice therefore it has become a research topic to reduce the complexity of parallel FIR filter in last decades [1-10].In many design situation, hardware overhead that is incurred by parallel processing cannot be tolerated due to limitation in design area therefore it is advantageous to realize parallel FIR filtering structure that consume less area than traditional parallel FIR filtering structure. This paper is organized as follows; section 2, explains related work of parallel FIR filter design. Section 3, explains a brief introduction of parallel FIR filter design structures are presented. Section 4 gives the Xilinx Results. Section 5, investigates the performance analysis of parallel FIR filter structure. In section 6, gives the conclusion.

2. RELATED WORK
Implementing Area efficient parallel FIR filter, parallel processing technique is used. MAD and fast FIR filtering algorithm produce parallel FIR filtering structure with reduction in hardware consumption, requires less area than traditional block FIR filter structure. Application of parallel processing involves replication of hardware unit [1]. Design an Area efficient parallel FIR filter implementation. Filter spectrum characteristics are exploited to select the best fast filter structure (FFA).A novel block filter quantization algorithm is introduced. Selection based on the frequency spectrum characteristics, further reduces the hardware cost and power consumption of parallel filter. But Speed of the filter Reduces [2]. Multiple bit DA algorithm formulation compressor Architecture involves hardware Efficient pipelined FIR structure with programmable coefficients FIR operation are first reformulated into the multibit DA form at an algorithm levels then at the Architecture level, the compressor instead of Booth encoding or RAM implementation is used for high speed operation .High speed programmable FIR filters are hard to implement efficiently because of the programmability require high cost. Programmability allows FIR coefficient to be changed at run time. There is no way to pre compute and store the common sub expression of programmable coefficients or to perform real time CSD encoding. For that Distributed Arithmetic is introduced. It replace ROM based programmable filter into RAM based filter [3].

Fast convolution algorithm to decompose the convolution matrix with simple Pre addition and Post addition matrix, computationally efficient parallel FIR filter with reduced number of required delay elements. Simple pre addition and post Addition matrix, when L is large ISCA based parallel filter involves many sub filters; require many multiplications [4]. Efficient use of recently proposed Fast FIR algorithms, Short length FIR filters with reduced arithmetic complexity where all multiplication is replaced by decimated sub filters. This algorithm most effective for short length FIR filters [5]. Computational structure for fast L-path and L-block digital filter based on the theory of fast algorithm for short linear convolution, Number of transfer function to be implemented by this approach plays same role in number of multiplication in linear convolution algorithm. This structure is fast but Computation complexity [6]. Conventional block digital filtering has been generalized to overlap case, Block digital filtering derived from fast FIR filtering algorithm short length based on Fast linear convolution algorithm and DFT algorithm. When block size is fixed, down sampling factor 'M' determines the data rate of each branch [7]. Sub filters in the previous parallel FIR structure are replaced by a second stage parallel FIR filter, reduces the number of required multiplication and addition at expense of delay elements. For very large size block, these filters are irregular [8]. Focus on storing architecture of coefficient and input block in order to efficiently reduce not only the occupied area of memory block. This is a large portion of silicon area. Also, addressing design technique for low power operation and decreased area of coded coefficient memory block, but this structure increases the power consumption [9].For symmetric convolution based design, symmetry of coefficients has been taken into consideration for the design structures yields more number of reductions in the multiplication at the expense of additional adders.FIR filter structure based on symmetric convolution provides low power and area efficient, high speed design [10]. Polyphase decomposition is one of the method for realizing FIR digital filter structure where the small sized parallel FIR filter structures are derived first and then large block- sized ones can be constructed by cascading or iterating small size parallel FIR filtering blocks [1]-[4].FFA can implement a L-parallel filter using approximately (2L-1) Sub filter Blocks, each of which is of Length N/L.FFA structures Successfully break the constraint that hardware implementation cost of a parallel FIR filter has a Linear increase with Block size L. It reduces the required number Multipliers to (2N-N/L) from L*N [1]-[3]. Fast Linear Convolution is decomposed into several short convolutions. That is larger block size filtering structures can be constructed through iteration of small sized filtering structures [5]-[9]. Above methods when it comes to symmetric convolution, symmetry of coefficient has not been taken in to consideration for design of structures yet, which can lead to a significant saving in hardware cost [10].

3. PARALLEL FIR FILTER

In this paper, Parallel FIR digital filter are designed using three structures for 2*2 parallel filters. The 2*2 parallel FIR filter consist of two filter inputs (X0, X1), two filter coefficient (H0, H1), and two filter output (Y0, Y1).

3.1 Traditional parallel FIR filter structure

This Figure 1, shows the traditional parallel FIR filter structure

$$Y_0=H_0X_0+Z^{-2}H_1X_1$$
$$Y_1=H_0X_1+H_1X_0$$

This equation gives the output of 2*2 traditional parallel FIR filter structure .This traditional filter requires four sub filter blocks of length N/2, 4 multiplier and 2 adders.

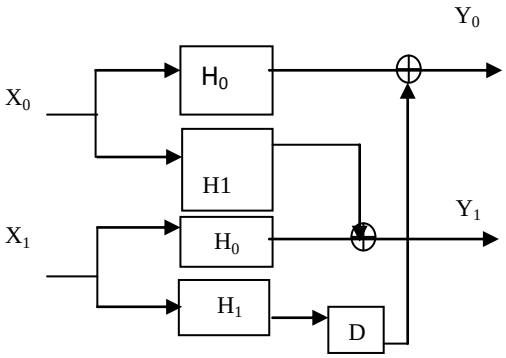


Figure 1

3.2 FFA based FIR filter structure

This Figure 2, shows the FFA based FIR filter structure

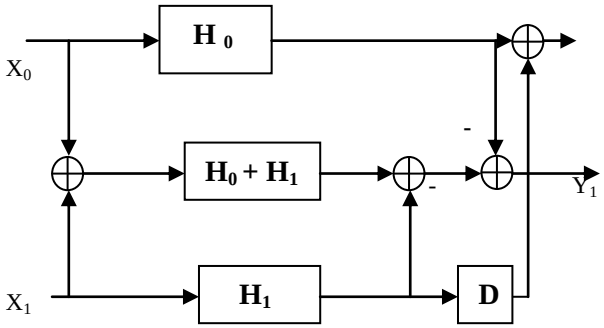


Figure 2

The output equation for this filter structure is

$$Y_0=H_0X_0+Z^{-2}H_1X_1$$
$$Y_1=(H_0+H_1)(X_0+X_1)- H_0X_0-H_1X_1$$

In this filter structure, three sub filter blocks of length N/2 and 3 multipliers and 4 adders are used.

3.3 Symmetric convolution based FFA

This Figure 3, shows the symmetric convolution based FFA FIR filter structure

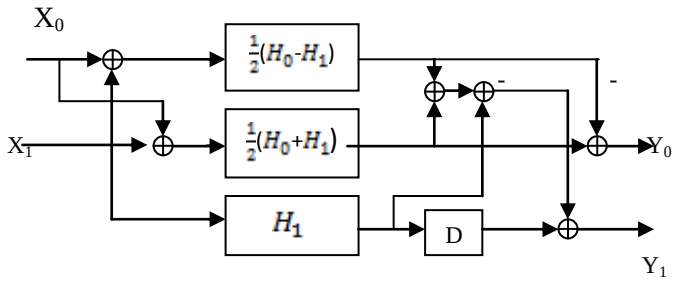


Figure 3

Output equation for this filter structure is

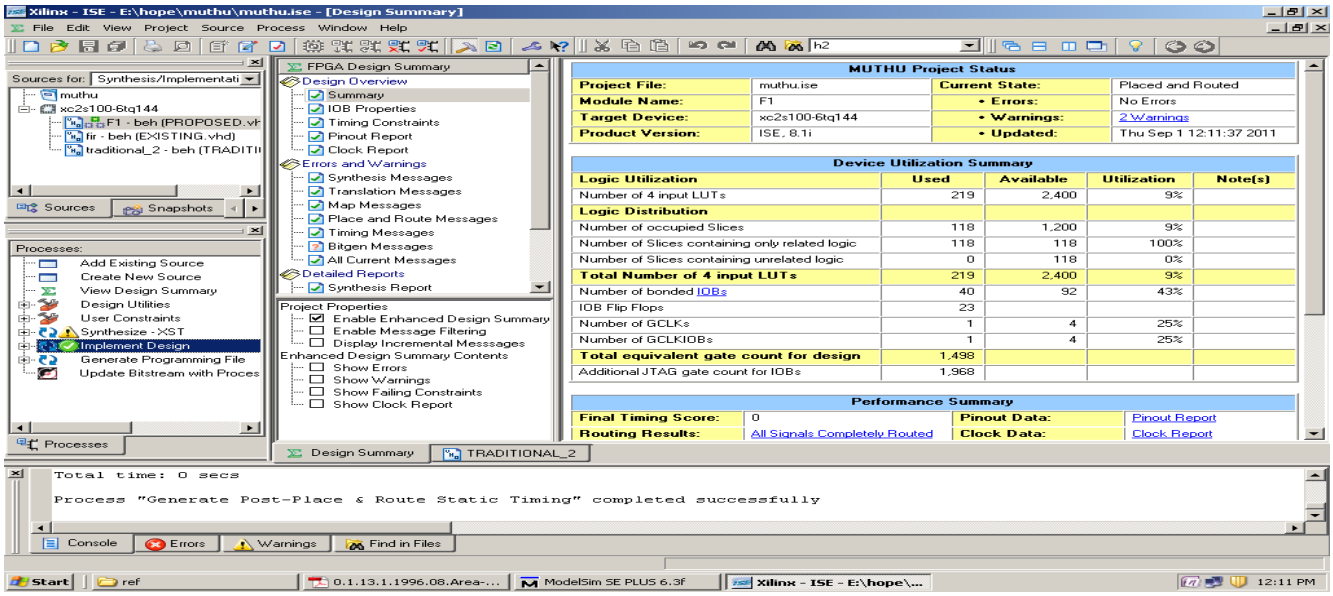
$$Y_0=\{\frac{1}{2}[(H_0+H_1)(X_0+X_1)+(H_0+H_1)(X_0-X_1)]-H_1X_1\}+Z^{-2}H_1X_1$$

$$Y_1=\frac{1}{2}\{(H_0+H_1)(X_0+X_1)-(H_0-H_1)(X_0-X_1)\}$$

These three FIR filter structures are designed using Carry Save Adder (CSA) initially then Carry Save Adder replaced by Ripple Carry Adder (RCA).Finally performance (Area & power) of these three FIR filter structures are compared.

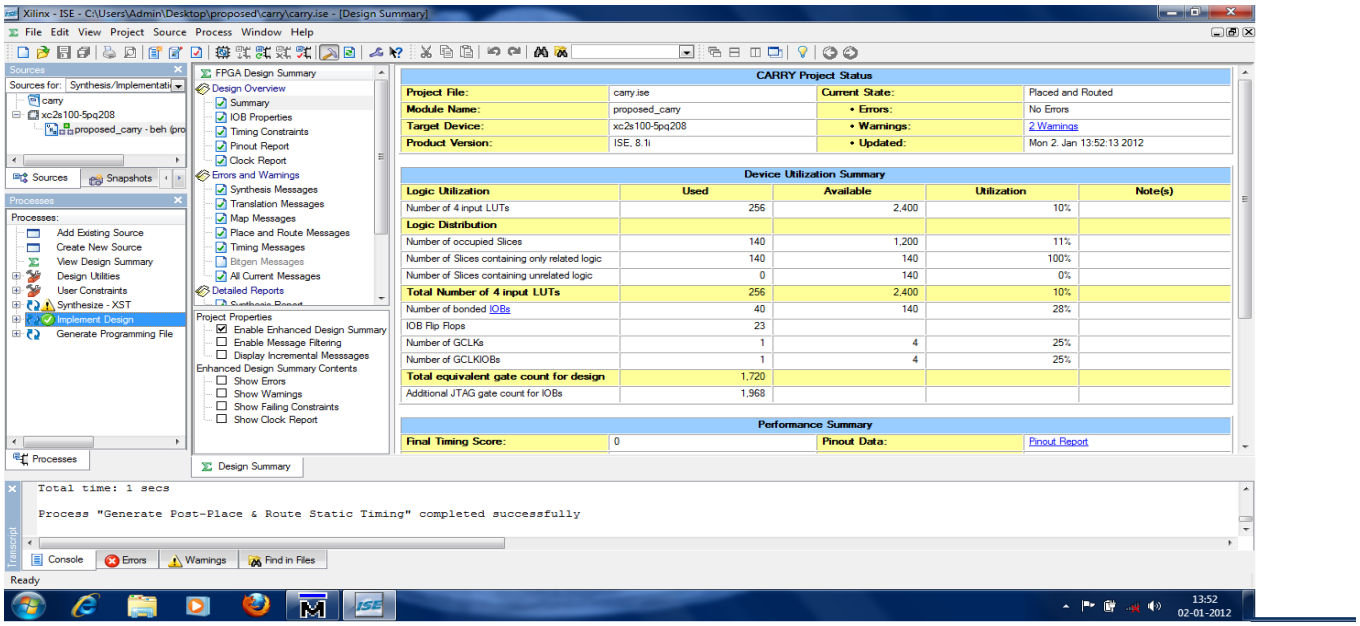
4. Xilinx Results:

4.1Output Area for FIR filter based on Ripple carry Adder: [Symmetric convolution based FIR Design]



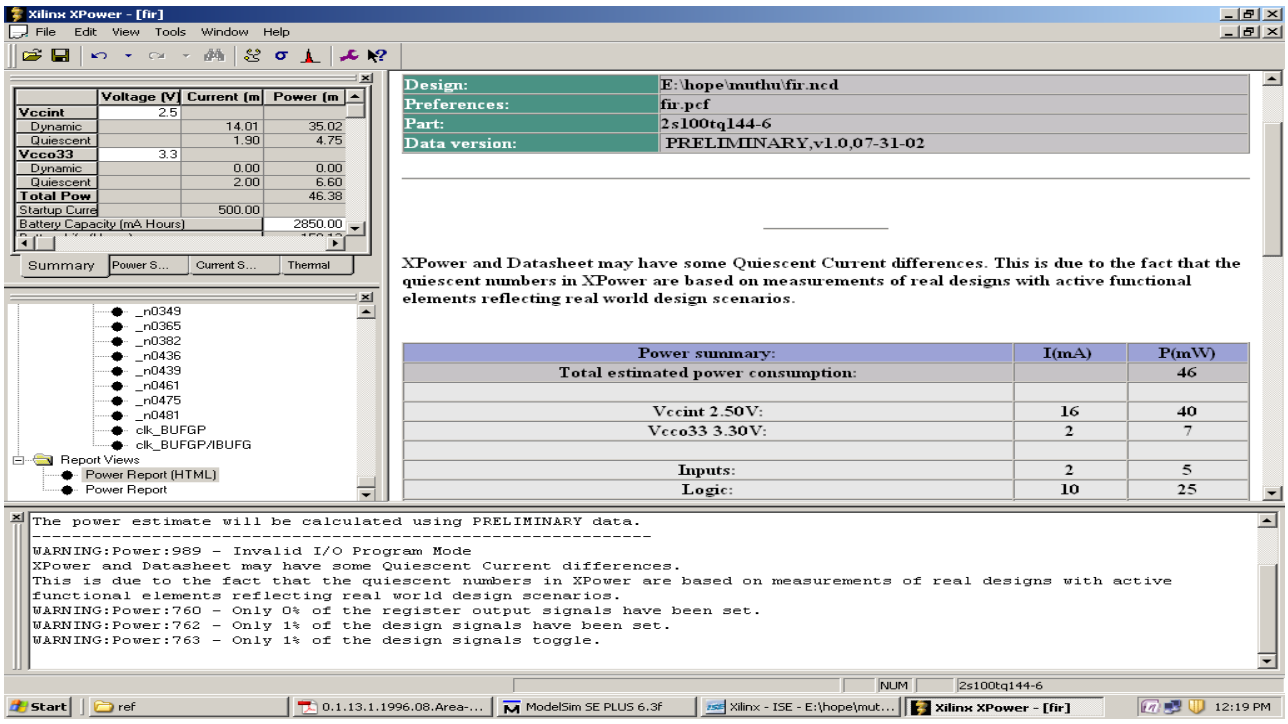
The Figure 4.1 shows the Xilinx result of area for FIR filter based on Ripple carry Adder of Symmetric convolution based FIR Design; Total equivalent gate count for design is 1498.

4.2 Output Area for FIR filter Based on Carry save Adder:[Symmetric convolution based FIR Design]



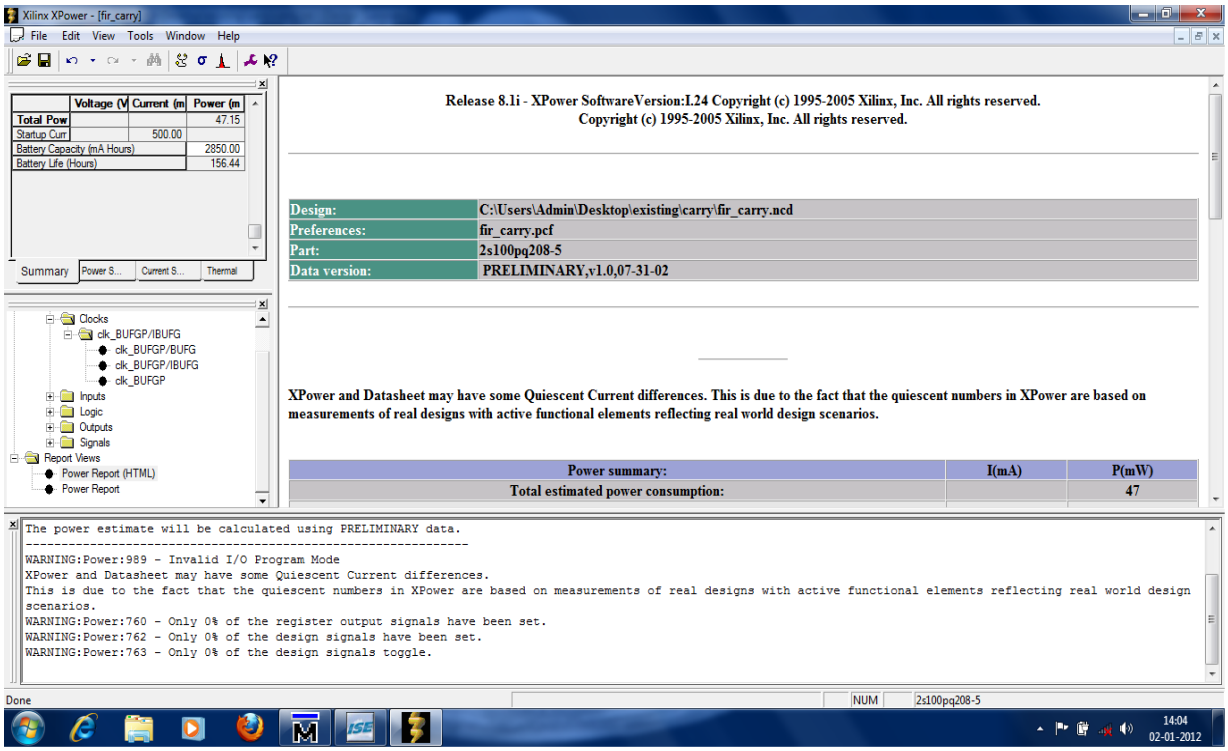
The Figure 4.2 shows the Xilinx result of area for FIR filter based on Carry Save Adder of Symmetric convolution based FIR Design; Total equivalent gate count for design is 1720.

4.3 Output Power for FIR filter Based on Ripple carry Adder: [FFA based FIR filter Design]



The Figure 4.3 shows the Xilinx result of power for FIR filter based on Ripple carry Adder of FFA based FIR Design; Total estimated power consumption is 46.

4.4 Output Power for FIR filter Based on Carry Save Adder: [FFA based FIR filter Design]



The Figure 4.4 shows the Xilinx result of power for FIR filter based on Carry Save Adder of FFA based FIR Design; Total estimated power consumption is 47.

5. PERFORMANCE ANALYSIS

The Performance of these three FIR filter structure based on Ripple Carry Adder and Carry Save Adder analyzed for 2*2 filters.

Table 4.1 Analysis of Area for parallel FIR filter

Filter Structure	AREA(based on Ripple carry adder)	AREA(based on Carry save adder)
Traditional FIR	3306	3558
FFA based FIR	2474	1470
Symmetric convolution based FFA FIR	1498	1720

Table 4.1 shows the performance analysis of three parallel FIR filter structure for area.

From the analysis of Area for parallel FIR filter structures, Ripple carry adder based FIR design is hardware efficient for Traditional and Symmetric convolution based FFA FIR structures. From the analysis of power for parallel FIR filter

Table 4.2 Analysis of power for parallel FIR filter

Filter Structure	Power(based on Ripple carry adder)mw	Power(based on Carry save adder)mw
Traditional FIR	48	48
FFA based FIR	46	47
Symmetric convolution based FFA FIR	44	44.09

Table 4.2 shows the performance Analysis of three parallel FIR filter structure for power.

structures, Ripple carry adder based FIR design is low power design for all these three structures.

6. CONCLUSION

In this Paper ,We have presented the performance analysis of parallel FIR filter .These parallel FIR filter are designed using Traditional FIR filter and FFA based FIR and symmetric convolution based FFA FIR .Initially all three parallel FIR filter structure design based on ripple carry adder then it replace by carry save adder .These filter structures are designed using VHDL .After designing these structures using VHDL coding are simulated using ModelSim 6.3 .Then the performance (area and power) of these parallel FIR filters are evaluated using Xilinx ISE 9.1 simulator. Multipliers are the major portion in hardware consumption for parallel FIR filter implementation. Proposed work will save as significant amount of multiplier at the expense of additional adders. Finally concluded that parallel FIR filter structure based on ripple carry adder provides hardware efficient and low power design, This structure comparatively better than existing FFA structure in terms of hardware cost.

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