

VLSI Architecture of Digital Auditory Filter for Speech Processor of Cochlear Implant

K. Rajalakshmi

Assistant Professor Sr.Gr.
Department of Electronics and Communication
Engg, PSG College of Technology, Peelamedu,
Coimbatore, India - 641 004

A. Kandaswamy

Professor & Head
Department of Biomedical Engineering
PSG College of Technology, Peelamedu,
Coimbatore, India - 641 004

ABSTRACT

Digital VLSI implementation of an auditory filter for speech processor of cochlear implant (CI) is proposed. Optimized design for hardware implementation of the filter with respect to area, power and speed is the significant criterion for the implementation of auditory filter for a CI. A digital filter is designed using the System Generator10.1 through the mathematical model of the FIR filter developed in Simulink using FDA tool. It is further downloaded onto the Spartan 3E FPGA Kit. Translation of the Simulink model into a hardware realization is done using system generator. Thus simulation is done both in the hardware and software environment. VHDL code for the filter is developed using the coefficients generated from FDA tool of System generator. The area, power and delay analysis for the design is done using SYNOPSIS Design Vision tool with 180micron technology.

General Terms

Auditory filter, VLSI Signal Processing,

Keywords

Keywords—Cochlear implant (CI), Finite-impulse response filter(FIR), area, power, speed

1. INTRODUCTION

A cochlear implant (CI) is a surgically implanted electronic device that provides a sense of sound to a person who is profoundly deaf or severely hard of hearing. The cochlear implant is often referred to as a bionic ear. Unlike hearing aids, the cochlear implant does not amplify sound, but works by directly stimulating any functioning auditory nerves inside the cochlea with electric fields stimulated through electric impulses. External components of the cochlear implant include a microphone, speech processor, an antenna and a RF receiver as in Figure.1. The speech processor splits the auditory signal into bands of different frequencies and converts them into suitable codes for stimulating the electrodes implanted in the cochlea of the ear. The electrode activates auditory nerve fibres to provide hearing sensation. The cost of the CI alone goes to around 100,000 US dollars. For the economical less affluent people with hearing ailment, it may be too costly to afford for this equipment to recover from the hearing loss. It becomes necessary to bring down the cost. The cost reduction may be achieved with reduced area, low power and enhanced performance of the cochlear implant. This objective intuited both the analog and the digital based CI designers to research their methods to provide people with cheaper and highly intelligible Cochlear implant as described in [6].

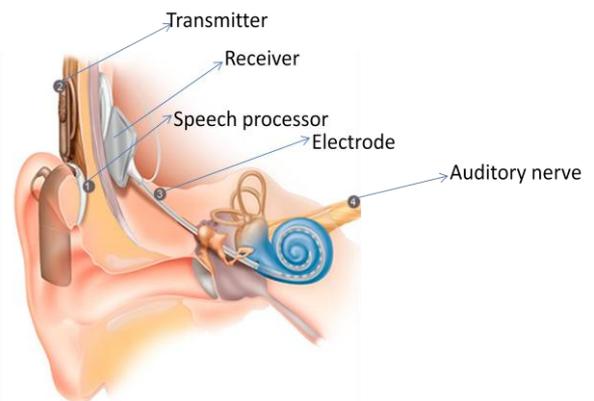


Figure 1.The Structure of Cochlear Implant

The speech processor part is the heart of the device that models electronically, cochlea of the ear. Many such implementations use the well accepted Patterson's Ear Model in [7] which models the audio-sensitive part of the ear as a bank of auditory filters each responsible for a particular band of hearing in the human audio spectrum[4]. The speech processor consists of a filter bank to split the speech spectrum into signals of various bandwidths in the range of audible frequencies. Since hearing is a real time activity there cannot be any significant delay introduced by the device into the line of hearing. The filter bank occupies the major portion of the speech processor which forms the external part of the cochlear implant and so it should occupy as little area as possible. So it becomes imperative that an optimized digital VLSI architecture be designed for this application that is tailor made to meet these requirements [1].A FPGA implementation of the of cochlea takes shorter design time and provides a high performance decimation filter as in Leong .M.P.'s paper[8][5]. In this paper, a model for the digital auditory filter of a speech processor is implemented.

2. FUNCTIONAL MECHANISM OF COCHLEA

The human hearing system is divided into four functional units such as a) the external ear b) the middle ear c) the inner ear and d) the auditory nerve. The first functional unit is the external ear which consists of the pinna and the auditory canal. The second functional unit is the middle ear which consists of three small bones called malleus, incus and stapes. The middle ear acts as an acoustic impedance matcher and increases the efficiency of transmission of sound by decreasing the amount of sound reflection. The third and the

most important functional unit is the inner ear or the cochlea. The basilar membrane in the cochlea is responsible for splitting the input signal into different frequencies. The location of inner hair cells along the basilar membrane determines the hair cells optimal response to various frequencies. When sound signal is transmitted in the form of travelling wave in cochlea, the hair cells at the apex respond to low frequencies whereas hair cells at the base respond to high frequencies as shown in Figure.2.and discussed in [2].

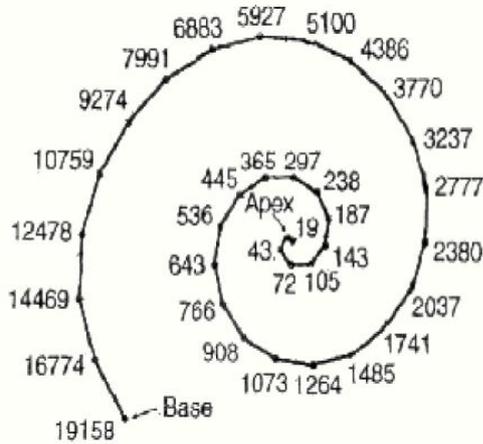


Figure 2: The structure of Basilar membrane shows the speech frequencies at apex and base.

3. FILTER DESIGN

In the previous section, we have seen the functional mechanism of the cochlea or the inner ear. The speech processor of the cochlear implant imitates the cochlea of human ear. Spectral analysis of speech signal is generally done by a filter bank model or a linear predictive coding (LPC) model. The speech signal is passed through a bank of band pass filters whose coverage spans the frequency range of interest in the signal which is from 100-5500Hz. The individual filters which generally do overlap in frequency can be implemented as finite impulse response filter FIR or infinite impulse response filter IIR. Generally the numbers of filters in the filter bank depend on the number of channels which in turn depend on the number of stimulating electrodes as mentioned in [3]. Hence the filter bank consists of 8 channels of band pass FIR filter as depicted in Figure.4a. Even though the characteristic of cochlea filter is nonlinear, the linear phase FIR filter is used here to overcome the disadvantage of IIR filter due to interaction of speech signal from different channels. FIR has several advantages over IIR filters. FIR filters do not have poles and are unconditionally stable. FIR does not accumulate errors since they depend on only a finite number of past input samples. The general definition of an FIR filter is,

$$y[n] = \sum_{k=0}^M b_k x[n - k] \dots\dots (1)$$

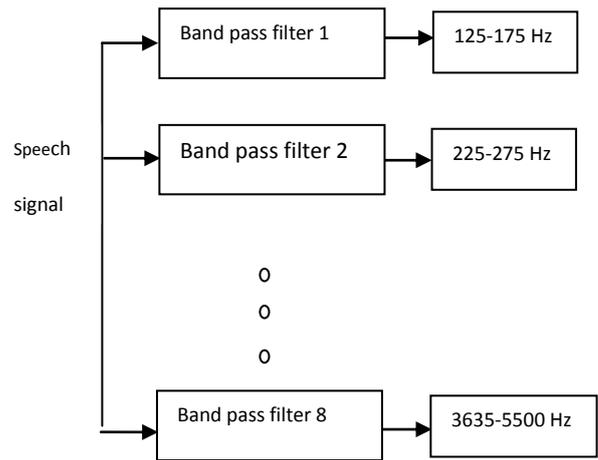


Figure 3a. Model of filter bank for speech processor

The impulse response is of finite length M, as required. The FIR filters have only zeros (no poles). Hence known as all-zero filters.

3.1. Structure of the FIR Filter

The algorithms for implementing the transfer function in hardware depend on the filter structure chosen to realize the transfer function. The real hardware has a finite number of bits representing the coefficients of the filter as well as the values of the input signal. The internal signals at the input of multipliers and the signals at the output of the multipliers and adders also are represented by a finite number of bits. The effect of rounding or truncation in the addition and multiplications of signal values depends on, for example, the type of representation of binary numbers whether they are in sign magnitude or two-complementary form. For linear phase FIR filters, the filter coefficients are symmetric or anti-symmetric. So for an N-th order filter, the number of multiplications can be reduced from N to N/2 for N even and to (N+1)/2 for N odd. The output of the filter is given as,

$$y[n] = h[0]x[n] + h[1]x[n - 1] + h[2]x[n - 2] \dots + h[M - 1]x[n - M + 1] \dots\dots\dots (2)$$

In this design we have chosen the Direct Form I structure of one FIR filter shown in Figure 3b. The work is on the implementation of a single band pass FIR filter from the filter bank of 8 band pass filters using the Xilinx Spartan 3E FPGA board.

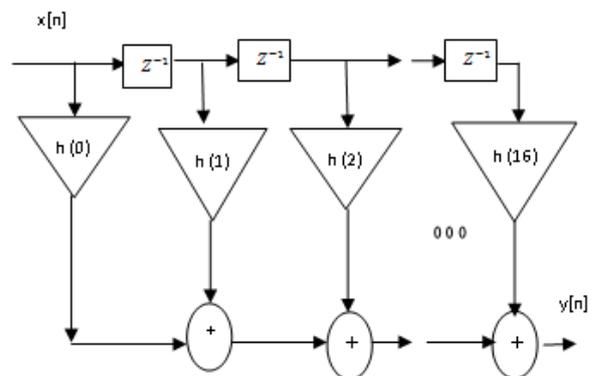


Figure 3b: Structure of Direct Form I FIR Filter

3.2. Generation of Filter Coefficients

The fir filter is designed as a band pass filter of order 16 with cut off frequencies $fc_1=500$ Hz, $fc_2=3000$ Hz and a sampling frequency $fs=8$ kHz. The filter structure is Direct Form I. Filter design and analysis tool (FDATool) of MATLAB is a Graphical User Interface (GUI) that allows designing, importing and analysing digital filters. So the specifications of the filter mentioned above are imported to the FDATool and the filter is designed in a mathematical environment and the filter coefficients are generated as in Figure.4.

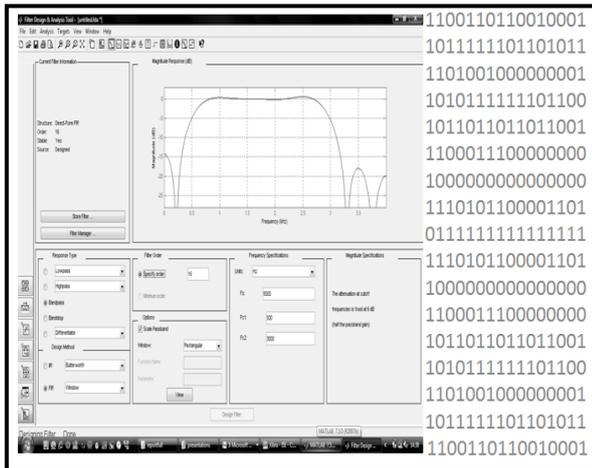


Figure 4. Filter Design using FDA tool and the Generated Coefficients

The generated coefficients were used in the HDL design of FIR filter and its functional verification was done on Xilinx ISE 10.1 environment. The operation of the filter is further verified by applying the testbench stimulus to the design and the results are compared and analyzed. The simulation results show a correct and efficient implementation of the FIR filter digitized using XILINX. The FIR filter module designed in Xilinx is imported to the Synopsys Design Vision tool to determine the area, power and timing.

3.3. Implementation of A Single FIR Band Pass Filter

The block processing work flow of System generator is used in the implementation of FIR filter; since it reduces the time of writing coding & debugging [6].The advantage of block processing is that the software itself will convert the processing block to its equivalent HDL code. This is called hw/sw co-simulation and hence implementing a complex cochlea FIR filter seems to be easier by this work flow. System Generator tool of Xilinx includes a FIR Compiler block that represents the single FIR band pass filter of order 16 that targets the dedicated hardware resources in the Spartan3E devices to create highly optimized implementations. The block diagram using Xilinx blockset for the single FIR band pass filter is shown in Figure 5a.

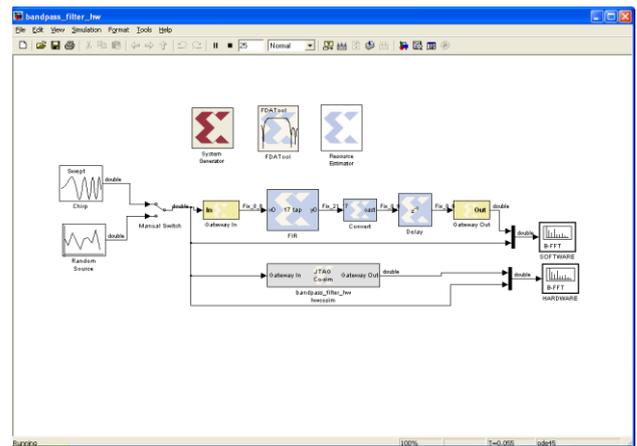


Figure.5a.The block diagram of the designed cochlea filter

4. RESULTS AND CONCLUSION

The hardware implementation of cochlea filter on the Spartan 3E reports the device utilization summary as shown in Figure.5b.

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of Slice Flip Flops	128	9,312	1%
Number of 4 input LUTs	201	9,312	2%
Logic Distribution			
Number of occupied Slices	179	4,656	3%
Number of Slices containing only related logic	179	179	100%
Number of Slices containing unrelated logic	0	179	0%
Total Number of 4 input LUTs	201	9,312	2%
Number of bonded IOBs	23	232	9%
IOB Flip Flops	20		
Number of GCLKs	1	24	4%
Number of MULT18X18SIOs	15	20	75%
Total equivalent gate count for design	3,101		
Additional JTAG gate count for IOBs	1,104		

Figure.5b. Summary of Hardware utilization on FPGA

The percentage of multiplier utilized out of the total multipliers on FPGA is reported as 75. The hardware and the software simulation of the cochlea filter are shown in Figure. 6a and 6b respectively.

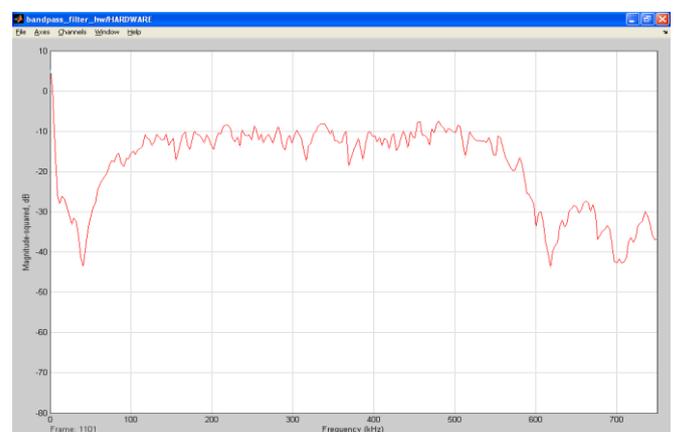


Figure.6a. Hardware simulation of cochlea filter

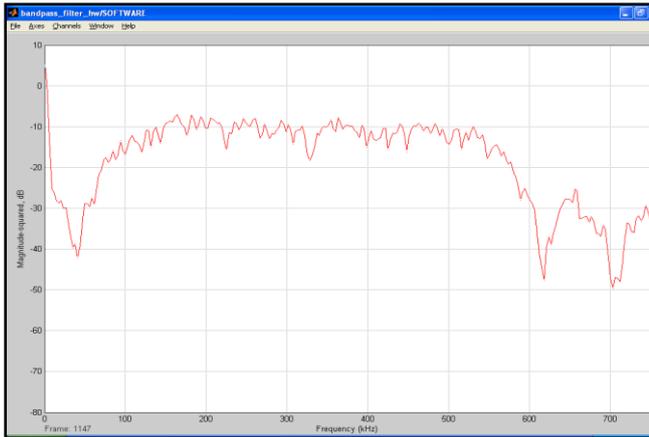


Figure.6b. Software simulation of cochlea filter

Both simulations are closely matched and proved that the complex cochlea filter can be designed and implemented in the hardware very quickly. In future years, this may lead to replace cochlear implants as easily as the optical lenses are replaced in the case of patient suffering from vision effect. When the cochlear filter is designed and implemented quickly the cost can be reduced and become affordable to the patient suffering from hearing ailment.

The filter coefficients generated from FDA tool are used in HDL design of cochlea whose functional verification is first implemented using Xilinx tools. This filter is modeled in VHDL and synthesized by using Synopsys Design Compiler in 0.18µm technology which estimates the area, power and timing parameters of the cochlea filter as shown in table 1.

Table 1. Analysis Results For The Cochlear Filter Instance

S.No.	Critical parameters	Cochlear Filter of Rekha et al	Proposed Cochlear filter
1	Timing	12.61125s	2.26 ms
2	Power	-	0.5656 mW
3	Area	11048 slices	67435 µm ²

Table.1 concludes that the proposed filter design is proven to be efficient in terms of timing and area parameter. In the future work VLSI signal processing concepts may be applied to obtain different optimized architecture in terms of area, power and performance. The real time speech signal must be processed through the suitable interfaces and FPGA.

5. ACKNOWLEDGMENT

The project “Special Manpower Development for VLSI and related software tools, SMDP II,” granted by Ministry of Information Technology, India must be acknowledged for making it possible to implement this research.

6. REFERENCES

- [1] Mishra, A., Hubbard, A.E “A cochlear filter implemented with a field-programmable gate array,” *Circuits and Systems II: Analog and Digital Signal Processing*, IEEE Transactions Volume 49, Issue 1, Jan.2002 Page(s):54 – 60.
- [2] Rekha,V.Dundur, M.V.Latte, S.Y.Kulkarni, and M. K.Venkatesha, “Digital Filter for Cochlear Implant Implemented on a Field-Programmable Gate Array”, *PWASET*, Vol 33, Sep 2008, pp 468-472.
- [3] Mahalakshmi.P., Reddy.M.R., “Signal Analysis by using FIR Filter banks in Cochlear Implant Prostheses”, *Proceedings of 2010 International Conference on Systems in Medicine and Biology 16-18 December 2010*, IIT Kharagpur, India
- [4] Philipos C. Loizou, “Signal Processing Techniques for Cochlear Implants”, *IEEE Engg. in Medicine and Biology*, 1999, pp 34- 45.
- [5] Hanukumar.V., Seetha Ramaiah.P., “Digital Speech Processing Design for FPGA Architecture for Auditory Prostheses”, *Journal of Computer Science And Engineering*, Volume 6, Issue 1, March 2011.
- [6] A. G. Katsiamis, E. M. Drakakis, and R. F. Lyon, “ A Practical Gammatone-Like Filters for Auditory Processing” *Hindawi Publishing Corporation, EURASIP Journal on Audio, Speech, and Music Processing*, Volume 2007, Article ID 63685, 15 pages, doi:10.1155/2007/63685
- [7] M. Slaney, “An Efficient Implementation of the Patterson-Holdsworth Auditory Filter Bank,” *Apple Computer Corporate Library, Apple Technical Report #35*, 1993.
- [8] M. P. Leong, Craig T. Jin and Philip H. W. Leong, “An FPGA-based Electronic Cochlea,” *EURASIP Journal on Applied Signal Processing*, no. 7, pp. 629-638, 2003.