A 1.7 – 2.5 GHz Active Inductor based Low Power Low Noise Amplifier for Multi Standard Applications

V. Vaithianathan
Assistant Professor,
SSN College of Engineering,
Kalavakkam-603110
Chennai, India

J. Raja
Professor& Head,
Anna University of Technology,
Tiruchirapalli- 620 024,
India

R. Srinivasan
Professor,
SSN College of Engineering, Kalavakkam-603110 Chennai, India

ABSTRACT
Due to an increasing demand for simultaneous global roaming and all-in-one wireless phones, the interest in the development of the multi-standard transceivers has been increased. In the receiver front end, the performance of Low Noise Amplifier (LNA) decides overall receiver sensitivity and hence its design plays a crucial role. In this paper, an active inductor based tunable two-stage LNA employing current reuse technique is proposed for multi-standard applications. The LNA is aimed at supporting CDMA-2000, GSM, WCDMA, WiMAX, Bluetooth and UMTS-TDD in the bandwidth range of 1.7 – 2.5 GHz. The proposed LNA achieved a power gain of greater than 13 dB, noise figure less than 2 dB and impedance matching less than –8 dB for all the standards. The stability factor is maintained above 1, ensuring stable operation of the LNA without oscillations. The LNA consumes very low power of 7.96 mW at an operating voltage of 1V. The performance analysis of the proposed active inductor based tunable LNA is carried out using Agilent's ADS simulator employing 90 nm CMOS technology.

General Terms
RF Circuit Design, Full Custom VLSI Design

Keywords
Multi Standard, Active Inductors, Tunable LNAs, Cascode Amplifier, Noise Figure

1. INTRODUCTION
Starting from the invention of telephone by Alexander Graham Bell to the latest fourth generation cellular wireless applications, everything has been driven by curiosity, especially in the pursuit of quality of life. In today's fast paced world, wireless communications are becoming increasingly popular owing to the mobility, portability and unlimited access to information it provides. The evolution of wireless technologies has been incredibly rapid and the future of this growth is endless. With the advent of 3G and 4G cellular systems, it has become quite essential to integrate many standards into a single wireless terminal [1]. According to an increasing demand for simultaneous global roaming and all-in-one wireless phones, the interest in the development of the multi-standard transceivers has been increased.

1.1. Multi Standard Receiver Front End
A Multi Standard Receiver can be implemented either by integrating different modules of individual standards on a single hardware chip or by using Software Defined Radio (SDR) [2]. A typical multi-standard receiver front-end comprises of a tunable LNA, a filter and a down conversion mixer as shown in Fig 1. It poses a unique challenge in the receiver design as the operating points of different components in the receiver must be set in such a way that it can provide an optimal performance for all the required standards.

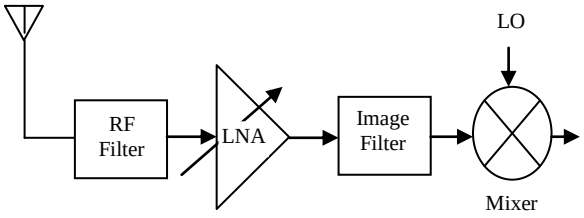

Fig 1: A Multi Standard Receiver Front End

The most popular standards that are currently in use are Worldwide Interoperability for Microwave Access (WiMAX), Code Division Multiple Access 2000 (CDMA2000), Global System for Mobile Communications (GSM), Wideband CDMA (WCDMA), Universal Mobile Telecommunication Systems Time Division Duplex (UMTS TDD) and Bluetooth (BT) [3] and [4]. The operating frequencies of the different standards are given in Table 1.

Table 1. Operating frequencies of the chosen standards

Standard	Frequency (GHz)
CDMA2000	1.7
GSM	1.9
WCDMA	2.1
WiMAX	2.3
Bluetooth/WLAN	2.4
UMTS TDD	2.5

1.2.Reconfigurable LNAs

The reconfigurable LNAs form the core of a multi standard receiver and it decides the overall efficiency of the system. The simplest way to obtain tunability is the use of switched capacitors [5] and switched inductors [6] but they both suffer from very high noise figure. The tunability can also be achieved by varying the resonant frequency of the ladder network using MOS varactors [7], [8]. The use of varactors reduces the circuit stability and its fabrication is also difficult. A con-current dual band LNA is used in [9] and [10] but it requires a precise characterization of the inductors and the capacitors used in the LC ladder which is extremely tedious.

1.3. Active Inductors

The active inductors use only MOS transistors connected in such a way that it can perform the function of conventional spiral inductors. They facilitate easy tuning of inductance with high quality factor and they also occupy less area when compared to spiral inductors [11]. The most commonly used active inductor structure is Gyrator C active inductor the schematic of which is given in Fig 2. The use of active inductors in multi standard receivers is proposed in [12] which uses digital band selector for tuning.

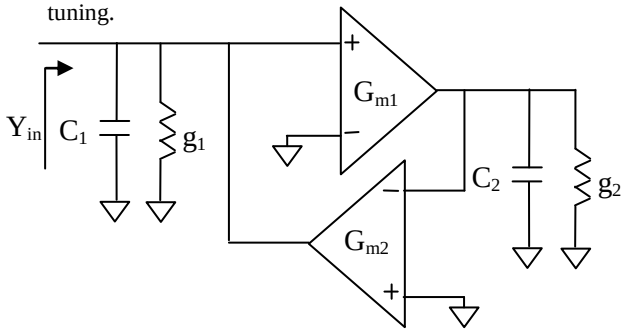

Fig 2: Gyrator C Active Inductor

In this paper, we proposed a low voltage high dynamic range CMOS active inductor based tunable LNA. The rest of the paper is organized as follows. Section 2 presents the circuit structure and operation of the proposed active inductor based tunable LNA for multi-standard applications. The simulation results and the performance analysis of the proposed active inductor based tunable LNA are presented in Section 3. The conclusions are given in Section 4.

2. PROPOSED LNA

The proposed LNA circuit comprises of two main stages, a cascade stage, with two common gate transistors (M_1 and M_2) stacked one on top of the other and a cascode stage made up of a common source (M_3) followed by a common gate (M_4) transistor as shown in Fig 3. Both stages employ a current reuse technique for power reduction and gain enhancement. The equivalent circuits are given in Fig 4, Fig 5 and Fig 6. The first stage common gate transistor (M_1), having low input impedance is used to obtain a perfect 50 Ω termination. By a proper choice of the device dimensions and by using a suitable combination of inductors and capacitors the input matching can be maintained below -10 dB. The input impedance of the proposed LNA is derived as given in equation (1)

$$Z_{in} \approx \frac{1}{sC_1} + \frac{sL_1}{1+s^2 L_1 C_{gs1}} \quad (1)$$

The parasitic capacitance present in the equation will make the input matching get worse at a high frequency. So best input matching is obtained at the resonant frequency which is given by equation (2)

$$\omega_{in} \approx \frac{1}{\sqrt{L_1(C_{gs1}+C_1)}} \quad (2)$$

The cascade stage constructed with the transistors M_1 and M_2 is used to achieve sufficient gain with higher bandwidth. It also reduces the effect of the parasitic capacitance at the drain terminals of the transistors. The inductance at the drain of M_1 (L_3) provides an advantage that it offers no extra dc voltage drop. The cascode arrangement reduces the Miller feedback capacitance [13], thereby isolating the input from the output return signals. This stage further enhances the amplification of the LNA. The gain equations for the proposed LNA are given by the following equations.

$$A_{V1} \approx g_{m1} Z_1 \quad (3)$$

where

$$Z_1 \approx \left(sL_3 + \frac{1}{sC_2}\right) \| \left(sL_3 + \frac{1}{sC_{gs2}}\right) \quad (4)$$

$$A_{V2} \approx g_{m2} Z_2 \quad (5)$$

where

$$Z_2 \approx sL_4 \| \frac{1}{sC_{in3}} \quad (6)$$

$$C_{in3} \approx C_{gs3} + (1 + A_{V3}) C_{gd3} \quad (7)$$

$$A_{V3} \approx g_{m3} Z_3 \quad (8)$$

$$Z_3 \approx \left(sL_6 + \frac{1}{sC_3}\right) \| \left(sL_5 + \frac{1}{sC_{gs4}}\right) \quad (9)$$

$$A_{V4} \approx g_{m4} Z_4 \quad (10)$$

$$Z_4 \approx sL_7 \| \frac{1}{sC_{in5}} \quad (11)$$

$$C_{in3} \approx C_{gs5} + C_{gd5} \quad (12)$$

$$A_{V5} \approx \frac{g_{m5} r_{o5}}{1 + g_{m5} r_{o5}} \quad (13)$$

$$A_V \approx A_{V1} \times A_{V2} \times A_{V3} \times A_{V4} \times A_{V5} \quad (14)$$

The circuit incorporates a current reuse technique [14] to effectively distribute the operating current and prevent it from sinking to the ground. This leads to improved power performance and overall gain flatness.

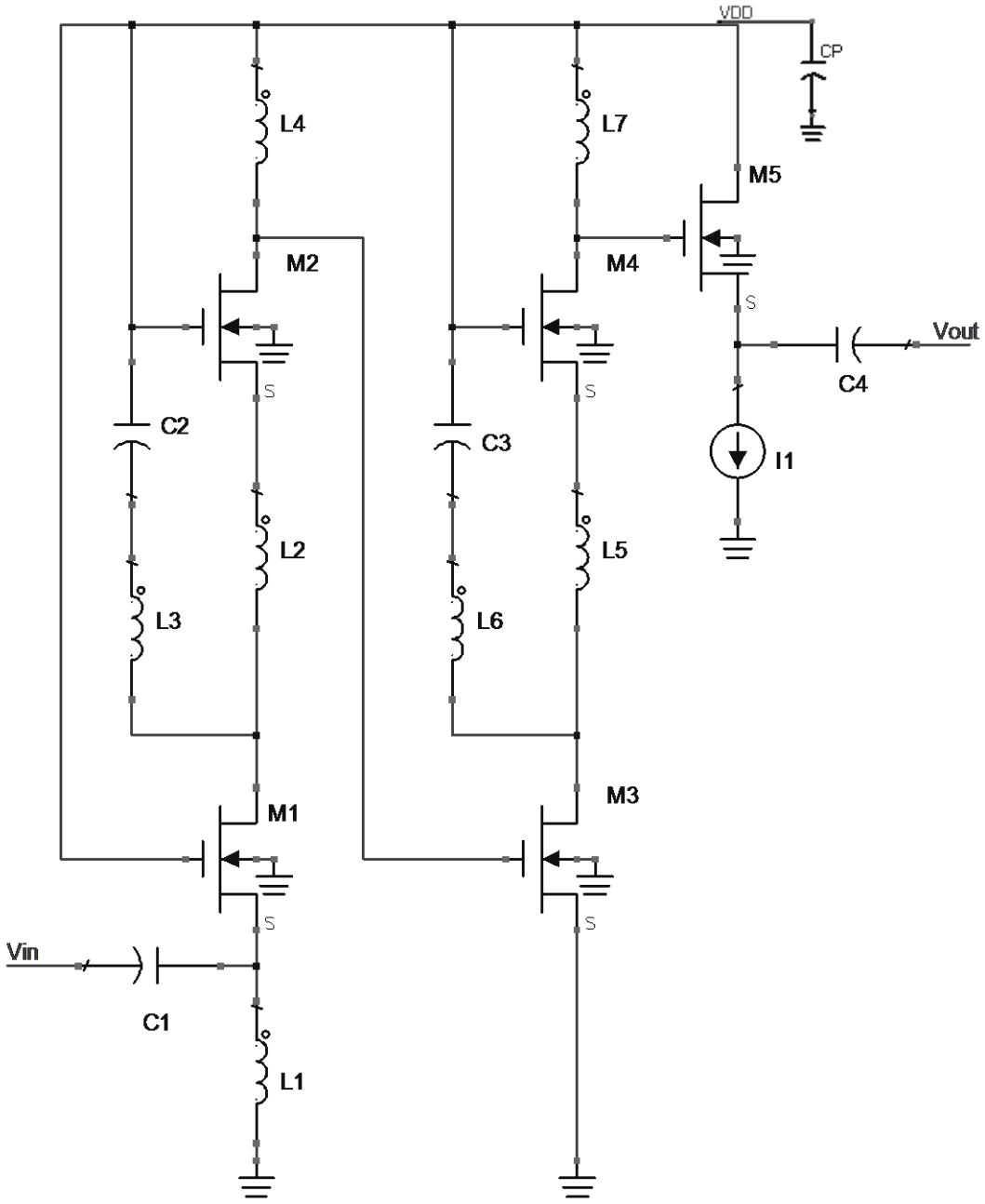

Fig 3: Proposed LNA

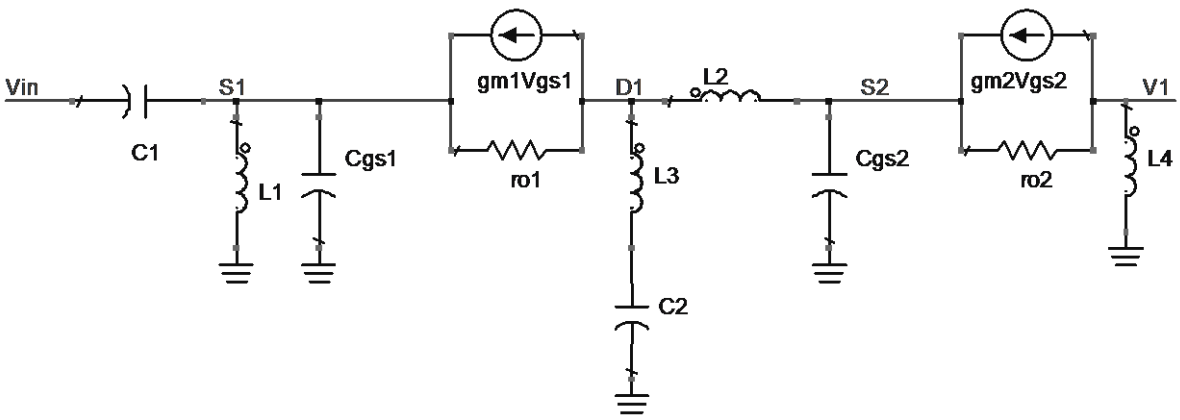

Fig 4: First Stage Equivalent Circuit

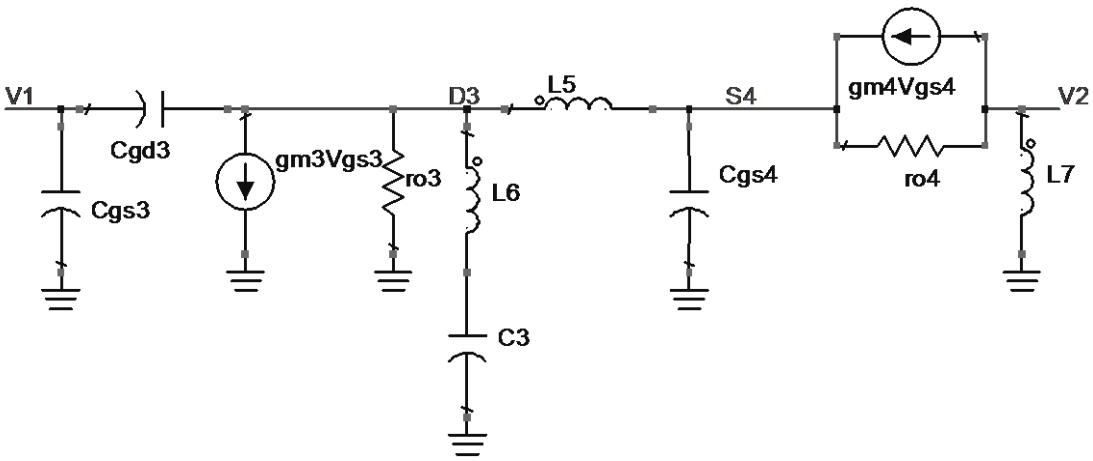

Fig 5: Second Stage Equivalent Circuit

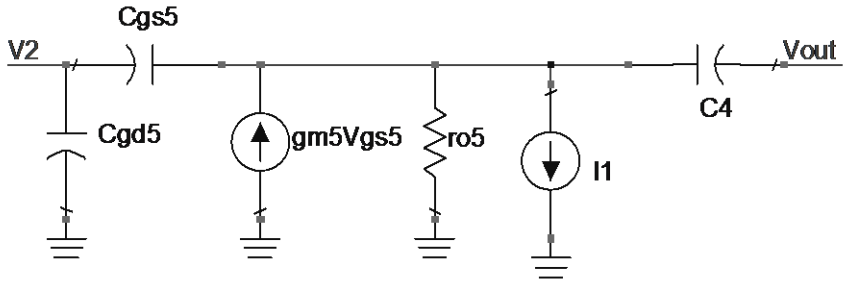

Fig 6: Buffer Equivalent Circuit

The current reuse configuration involves the use of cascode transistors along with a drain load inductance (L_3), and the loop inductance (L_2) and capacitance (C_1). A portion of the dc supply voltage is dropped across capacitor C_1. By principle this charge is stored by C_1, which can be used to bias the upper common gate transistor. Thus this transistor does not consume the entire voltage provided by the supply, leading to lesser power consumption.

In general, the load inductance at the drain has a value greater than the loop inductance. At the high operating frequencies the inductance L_3 provides a high impedance path. Thus the signal current flows through the lower impedance path containing L_2 and C_1, enabling the reuse of this current. As a result the input signal can be amplified twice, giving rise to better gain than the normal structure. Using this configuration we obtain a high gain with low power consumption. It is important to understand that a large loop capacitance is preferred in the design for a better signal coupling. With M_1 and M_2 sharing the same bias current, the total power consumption of the current-reused amplifier is minimized. The same principle can be used to describe the reuse of current in the second stage. The design considerations of the current-reused LNA are similar to those of cascaded amplifier. The common drain amplifier offers low output impedance, thus making it a suitable choice to be placed at the output end for perfect matching. The output impedance of the LNA is derived as

$$Z_{out} \approx r_{o5} \qquad (15)$$

A constant current source is used at the output of the buffer in order to obtain linear input-output transfer characteristics [15].

Table 2. Values of the variable inductors for all six standards

Standard	L3 (nH)	L4 (nH)	L6 (nH)	L7 (nH)
CDMA 2000	**9.08**	**6.9**	**8.05**	**6.14**
GSM	**8.41**	**6**	**7.86**	**6.53**
WCDMA	**7.85**	**6.15**	**7.5**	**7.12**
WiMAX	**7.33**	**7.1**	**6.33**	**7.84**
BT	**6.96**	**7.6**	**6.14**	**8.34**
UMTS TDD	**6.24**	**5.96**	**6.08**	**8.52**

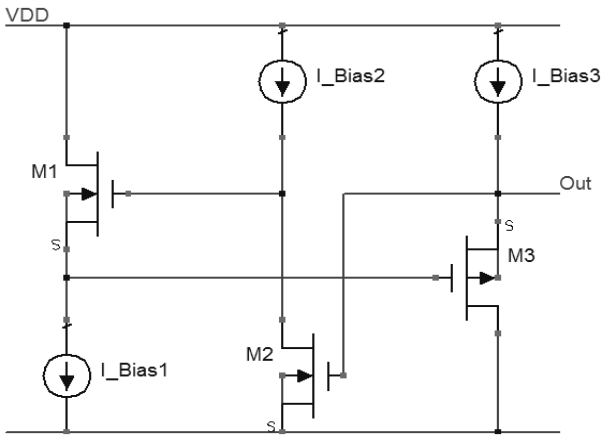

Fig 7: Low Voltage CMOS Gyrator C Active Inductor

In our proposed LNA the inductors L_3, L_4, L_6 and L_7 are made tunable in order to make a single LNA compatible for multi standard applications. A low voltage CMOS Gyrator C active inductor as proposed by Ngow and

Thanachayanont in [16] is employed in our circuit to achieve the desired tunability. The schematic of this active inductor is given in Fig 7. The current source I_Bias2 is varied in order to obtain different values of inductances suitable for various standards. The circuit offers easy biasing and it also ensures a better stability [17].

3. SIMULATION RESULTS

The simulations are done in Agilent's Advanced Design System (ADS) using CMOS 90 nm process along with the macro model generated for tunable capacitor and inductor.

The simulation results are presented in Fig 8 to 14. The parameters such as Quality Factor(Q), Input Matching (S_{11}), Reverse Isolation (S_{12}), Power Gain (S_{21}), Noise Figure (NF), Output Matching (S_{22}) are verified for each of the six standards.

3.1 Quality Factor (Q)

The Fig 8 shows the obtained quality factor for the proposed active inductor over frequency range of 1.7 to 2.6 GHz. Its value ranges from 51.6 to 53.5 which is acceptable for our applications.

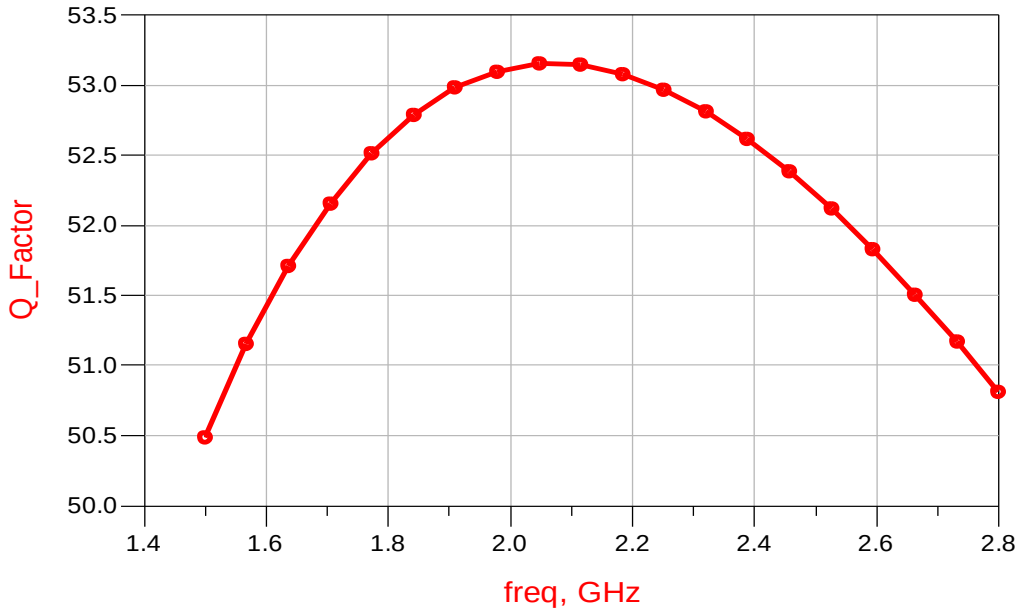

Fig 8: Quality Factor (Q)

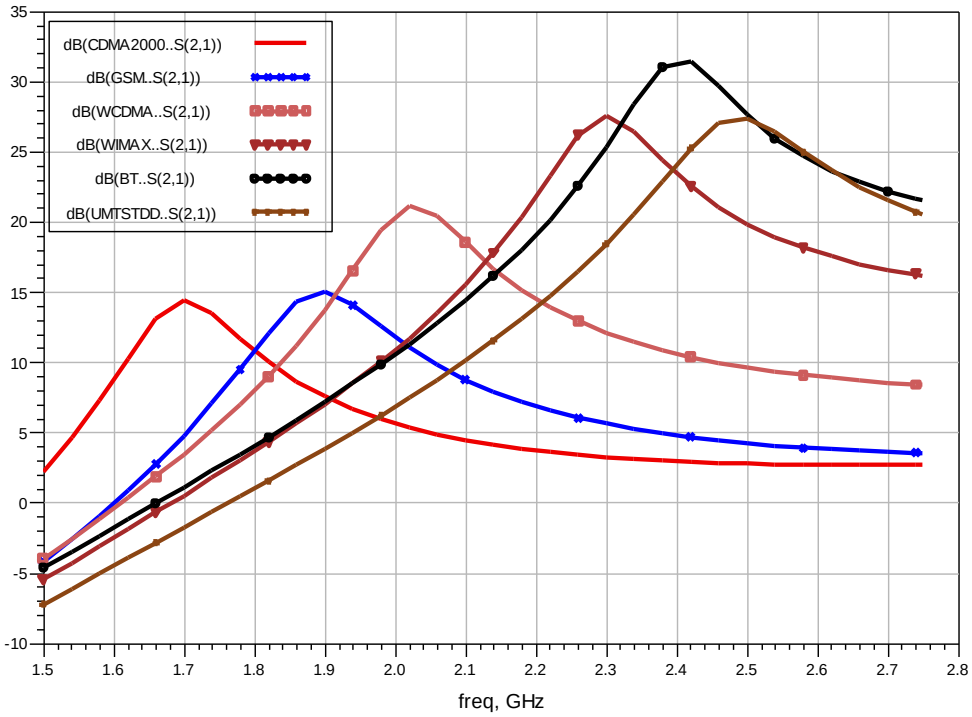

Fig 9: Power Gain (S_{21}).

3.2 Power Gain (S_{21})

Fig 9 shows the power gain which is above 13 dB at the operating frequencies for all the standards. A maximum gain of 33 dB is obtained for BT at 2.4 GHz.

3.3 Noise Figure (NF)

Fig 10 plots the noise figure of the LNA which is observed to below 2 dB for all the required frequencies. A minimum noise figure of 1.3 dB was obtained at a frequency of 1.7GHz which corresponds to CDMA 2000.

3.4 Input Matching (S_{11})

The input matching is kept well below -8 dB for all the standards as shown in Fig 11. The best matching is obtained for WiMAX where S_{11} is -15 dB at 2.3 GHz.

3.5 Output Matching (S_{22})

Fig 12 shows output matching characteristics for the proposed LNA. It is evident that for all the desired frequencies it is kept well below -10 dB so that there are minimal reflections at the load resulting in efficient power transfer.

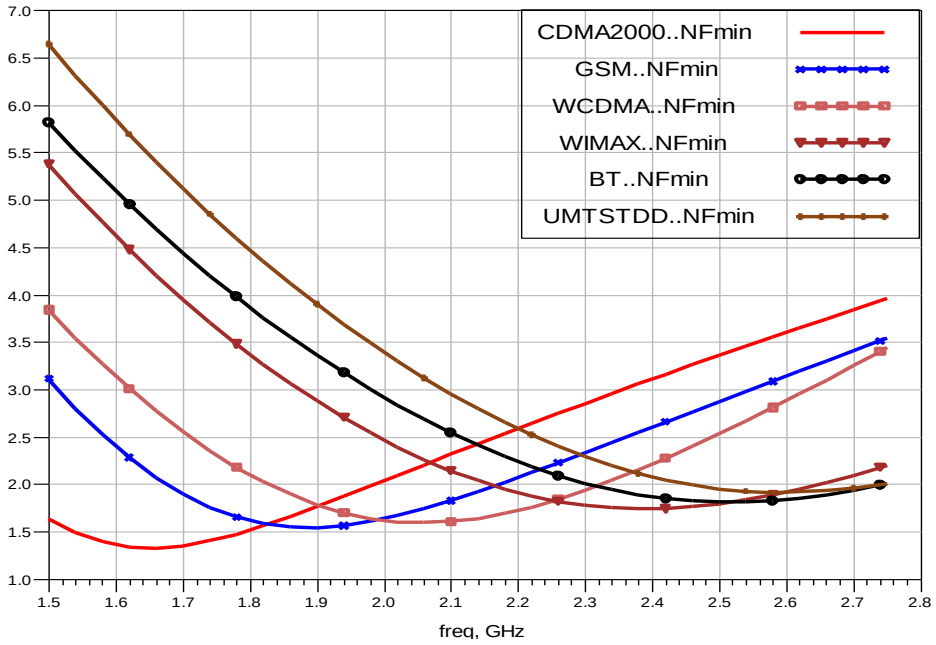

Fig 10: Noise Factor (NFmin)

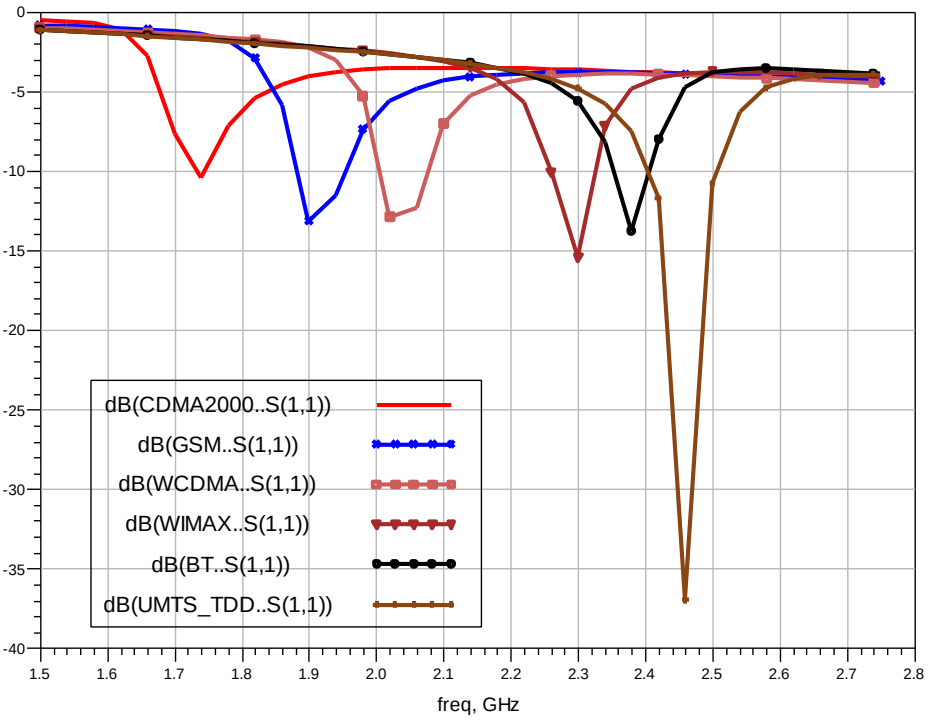

Fig 11: Input Matching (S_{11})

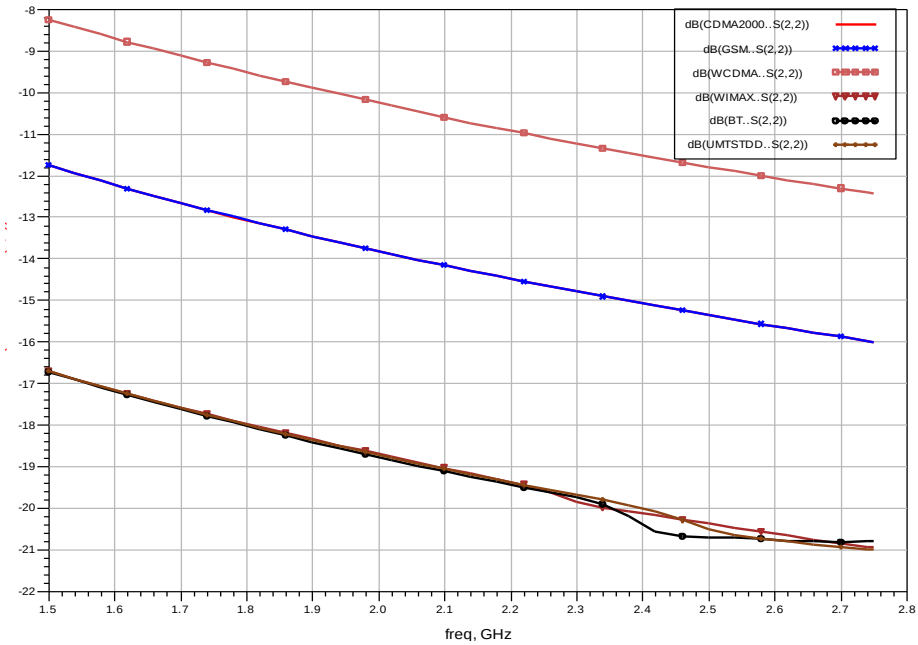

Fig 12: Output Matching (S_{22})

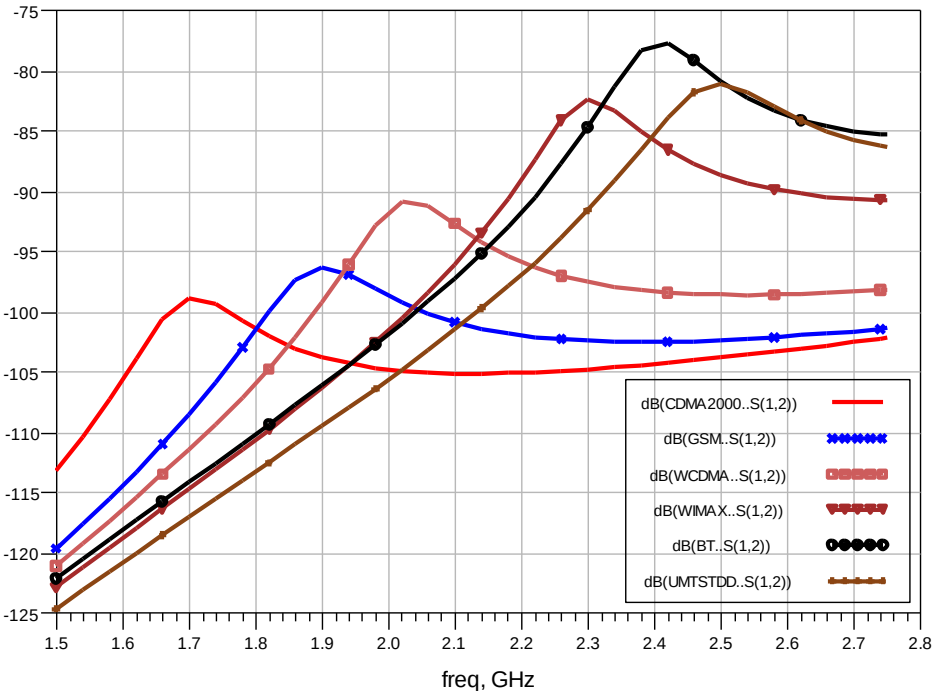

Fig 13: Reverse Isolation (S_{12})

3.6 Reverse Isolation (S_{12})

The reverse isolation characteristic is presented in Fig 13, with a minimum value of – 99 dB corresponding to the CDMA-2000. The value is kept well below –77 dB throughout the entire frequency range, thereby offering better stability to the design.

3.7 Stability Factor (K)

The Rollett stability factor, `K' is calculated for all the standards by using the equation (16). It is observed that the value of 'K' is above unity thereby ensuring that the circuit is unconditionally stable without oscillations [18].

$$K = \frac{1+|S_{11}S_{22}-S_{12}S_{21}|^2-|S_{11}|^2-|S_{22}|^2}{2|S_{12}S_{21}|} \quad (16)$$

The Table 3 presents the performance summary of the proposed LNA for all six standards and the Table 4 presents a comparison of simulation results of the proposed LNA with recently reported LNAs.

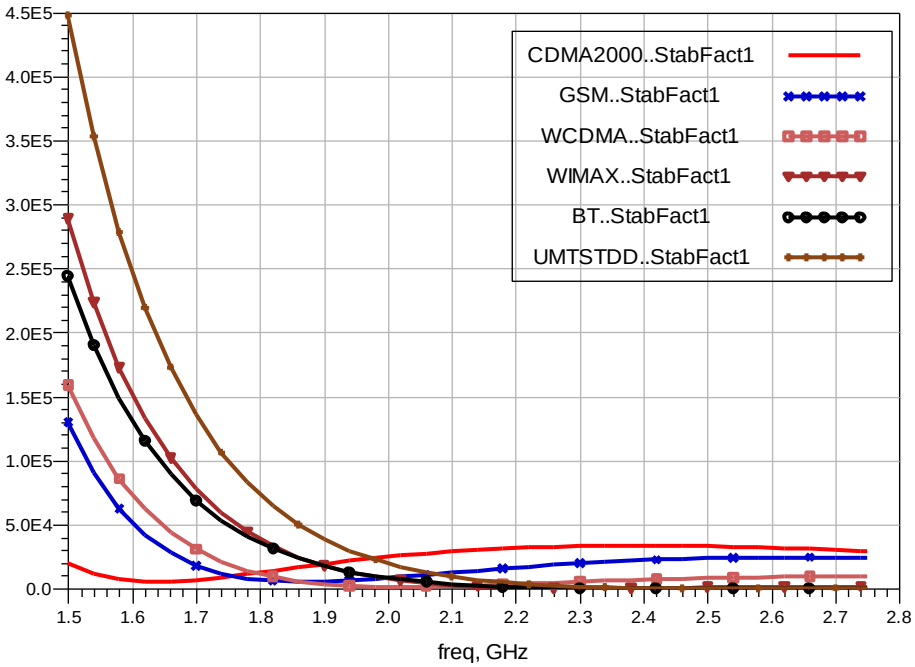

Fig 14: Stability Factor

Table 3: Performance summary of the proposed LNA for all six standards

Standard	Power Gain (S_{21}) dB	Noise Figure (NF) dB	Input Matching (S_{11}) dB	Output Matching (S_{22}) dB	Reverse Isolation (S_{12}) dB	Power (mW)
CDMA2000	14	1.3	- 8.5	- 12.6	- 99	7.408
GSM	15	1.5	- 13.5	- 13.5	- 97	7.408
WCDMA	19	1.55	-8	- 10.7	- 92.5	7.86
WiMAX	27.5	1.75	- 15	- 19.6	- 82.5	7.968
BT	33	1.8	- 10	- 20.4	- 78	7.968
UMTS-TDD	27.5	1.9	- 11	- 20.6	- 81	7.968

Table 4: Comparison of simulation results of the proposed LNA with recently reported LNAs

References	Standard	Power Gain (S_{21}) dB	Noise Figure(NF) dB	Power (mW)
[8]	GSM	24.7	1.61	53.3
	WCDMA	20.6	1.73	28.5
	BT	16.2	1.77	25.3
	WLAN	22.3	1.64	30.5
[9]	GSM (0.9 GHz)	18	4.6	32.4
	BT	24	4.4	32.4
	WLAN	24	4.4	32.4
[10]	GSM (0.9 GHz)	16.8	1.98	12
	BT	31	1.92	12
This Paper	**CDMA2000**	**14**	**1.3**	**7.408**
	GSM	**15**	**1.5**	**7.408**
	WCDMA	**19**	**1.55**	**7.86**
	WiMAX	**27.5**	**1.75**	**7.968**
	BT	**33**	**1.8**	**7.968**
	UMTS-TDD	**27.5**	**1.9**	**7.968**

4. CONCLUSION

In this paper, a multi satandard LNA with current reuse technique for power reduction and gain enhancement is presented. An active inductor is used to tune the proposed LNA so that it can be used for various standards such as WiMAX, CDMA2000, GSM, WCDMA, UMTS TDD, BT. The proposed LNA is designed using 90 nm CMOS technology and its performance is analyzed by performing simulation using Agilent ADS simulator. The achieved power gain is greater than 13 dB while reaching its maximum value at the center frequency corresponding to each standard. The achieved noise figure is well less than 2.68 dB for the desired standards. The input and output matching are well below – 12 dB and – 14 dB respectively. The presented LNA claims lowest noise figure while achieving a high power gain with low power consumption. The proposed circuit also has less design complexity. The tunability is attained by the active inductor which leads into lesser area.

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