A Novel Latch design for Low Power Applications

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ABSTRACT
Low power device design is now a vital field of research due to increase in demand of portable devices. This research paper proposes novel design of 8-transistor latch. Design comparison with the conventional design is performed at 65nm and 45nm to show technology independence. Comparative simulation results show that area and power efficient latch design is better choice for portable applications.

Keywords
Level converting Flip Flop, Portable Applications, Latch, Sub-threshold Region, and Low Power applications.

1. INTRODUCTION

The operation of low frequency circuits in the sub-threshold region stands out as the optimal method of power reduction [1]. Supply voltage scaling reduces both active energy dissipation and leakage power. When applied aggressively, voltage scaling leads to sub-threshold (sub- V_T) operation [2]. In this regime, severely degraded on/off current ratios and increased sensitivity to process variations are the main challenges for sub- circuit design [3] in 65nm technologies and below.

Sub-threshold circuit operation is driven by currents much weaker than standard strong-inversion circuits, and so is characterized by longer propagation delays and limited to lower frequencies. Due to the exponential dependency on the value of V_{TH}, sub-threshold circuits are very sensitive to process variations and temperature fluctuation. These, and other factors, have to be taken into consideration when designing circuits for sub-threshold operation.

Latches and Flip-Flops are the most complex, power consuming and indispensible components among the various building blocks in digital designs. About 30%-70% of the total power in the system is dissipated due to clocking network, and the flip-flops [4]. The logic gate delays in a clock period is reducing by 25% per generation in high-performance microprocessors, and is approaching value of 10% or below beyond 0.13µm technology [5]. As a result, latency of the flip-flops or latches is becoming larger portion of the cycle time. Several FF designs have been proposed for power reduction. Although many of these methods have been shown to considerably reduce the power consumption, they are not necessarily suitable for operation in the sub-threshold region. In addition, some of these designs require a large number of transistors for implementation, resulting in a large area, not necessarily suitable for small, low-priced systems.

Flip flop and Latch are the most commonly used sequential elements whose purpose is synchronizing data signals. A latch is a three-terminal element, having two inputs, data (D) and clock (clk) and one output (Q). The data must be stable before the falling edge of the clock (called the setup time t_{setup}) and after the falling edge of the clock (called the hold time t_{hold}) for the data to be correctly stored in the latch. For timing requirements, level sensitive latches are widely used in high performance ICs where timing analysis is more critical and challenging [6-8]. The conventional edge-triggered flip-flop (FF) design methods using clock synchronization are very practical, since only the timing constraints defined by a given clock frequency are optimized. However, clock skew that has a strong influence on clock frequency design prevents the FF design because of the variations. Thus, level-triggered latch design method has been proposed as alternatives to FF-based design methods.

The total energy dissipation E_T of static CMOS circuits operating in sub-V_T regime is modeled as

$$E_T = E_{dyn} + E_{leak} + E_{sc}$$

$$E_T = \alpha C_{tot} V_{DD}^2 + I_{leak} V_{DD} T_{clk} + I_{peak} t_{sc} V_{DD}$$

Where, E_{dyn}, E_{leak}, and E_{sc} are the average energy dissipation due to switching activity, the energy dissipation resulting from integrating the leakage power over one clock cycle T_{clk}, and the energy dissipation due to short circuit currents, respectively. The energy dissipation E_{sc} has been shown to be negligible in the sub-V_T regime [9]. The dynamic power dissipation, since the input and voltage and the supply voltage are less than the threshold voltage of the transistor, is also very less as compared with the super-threshold operation of the device. The dynamic and leakage power dissipation is only results from sub-threshold currents [10].

The critical path delay in CMOS devices is given by [11]

$$T_{clk} = k_{crit} \frac{C_{inv} V_{DD}}{I_o e^{-\frac{V_{DD}}{nV_T}}}$$

Where, k_{crit} is the critical path delay, n denote the slope factor and and V_T the thermal voltage. The total energy dissipation E_T assuming operation at the maximum frequency is

$$E_T = C_{inv} V_{DD}^2 [\mu_e k_{cap} + k_{crit} k_{leak} e^{-\frac{V_{DD}}{nV_T}}]$$

It is found that the sub-V_T model predicts the energy dissipation with less than 3.8% error [12].

There are three main sources of power dissipation in the latch [13]:

- *Internal power dissipation* of the latch, including the power dissipated for switching the output loads
- *Local clock power dissipation*, presents the portion of power dissipated in local clock buffer driving the clock input of the latch
- *Local data power dissipation*, presents the portion of power dissipated in the logic stage driving the data input of the latch

Total power parameter is the sum of all three measured kinds of power. Lot of research is going on to develop low power VLSI applications [14-15].

In this paper, the new design of latch with 8-transistor is proposed. The design is compared with the conventional design of 10-transistor latch. The proposed and the conventional designs are simulated and analyzed at 65nm and 45nm technologies to show the technology independence. The designs are observed keeping the power dissipation, delay and area as parameters.

This paper is organized as follows: the next section describes about the proposed design of latch along with the conventional latch. In the next section, the two designs are simulated and simulation data is analyzed followed by conclusions and references.

2. LATCH DESIGN

Latches, flip-flops, RAMs, and other sub-circuits with memory impose specific timing requirements such as setup and hold times on data, and minimum pulse widths on clock inputs.

Conventional 10-transistor Latch is a primarily used in sequential memory related applications (Fig. 1). The transmission gate at the input side contains the data input, which is transmitted through this gate only when clock signal is high. A transmission gate must not be called a logic gate but rather resembles a contact that makes and breaks a conducting path under the direction of a control voltage. Bistable circuit behavior is obtained by connecting two inverting gates so as to form a positive feedback loop. The two stable states of equilibrium then naturally correspond to two memory states. Two complementary transmission gates open the loop and admit the voltage at data terminal D into the loop while CLK = 1. The conventional latch is positive level triggered flip flop.

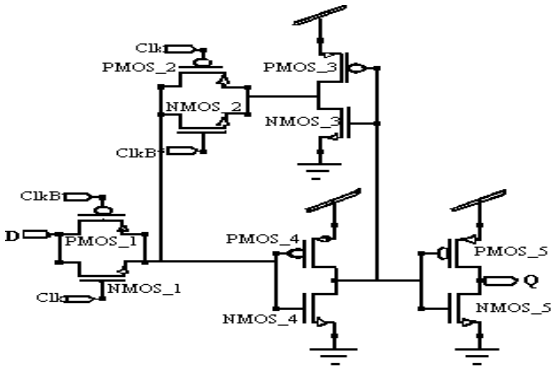


Fig. 1 Conventional 10 Transistor Latch

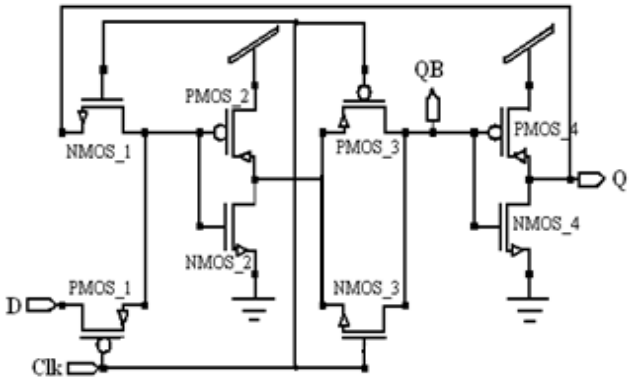


Fig. 2 Proposed 8-Transistor Latch Design

The proposed 8 transistor static latch uses the pass transistor logic instead of transmission gate, and thus two transistors are less. In this design, the transistor PMOS_1 at the input side takes the data input and passes when the clock signal is low. The NMOS_1 is forming the feedback loop. The transistor NMOS_3 is passing the signal when clock signal is high and transistor PMOS_3 is passing the intermediate signal when clock signal is low. NMOS transistors are weak '1' and PMOS transistors are weak '0', thus pass transistor logic gives threshold loss problem but this can be overcome by the inverters in the circuit. Output 'QB' suffers with some threshold loss problem and that is verified during simulation, but output inverter compensates this problem and output waveform of 'Q' is not showing any threshold loss. The proposed 8T latch is negative level triggered.

3. SIMULATION AND ANALYSIS

In low power applications area, power consumption, and delay introduced by the device are the main technological aspects to prefer a design over the other contending designs. The proposed 8T latch is area efficient design because it is producing the better results with less number of transistors. The conventional and the proposed designs are simulated using Tanner Tools v12.5 and power consumption and delay produced are measured at various temperatures, supply voltages and frequencies. For fair comparison of the designs, the aspect ratio of all the transistors is taken '1' in both proposed and conventional design. The designs are compared at two different technologies, 45nm and 65nm, to show the technology independence of the proposed design. The waveform of the proposed latch shows that it is a negative level triggered latch (Fig. 3). The output changes at negative level of the clock and remains constant during the positive level of the clock.

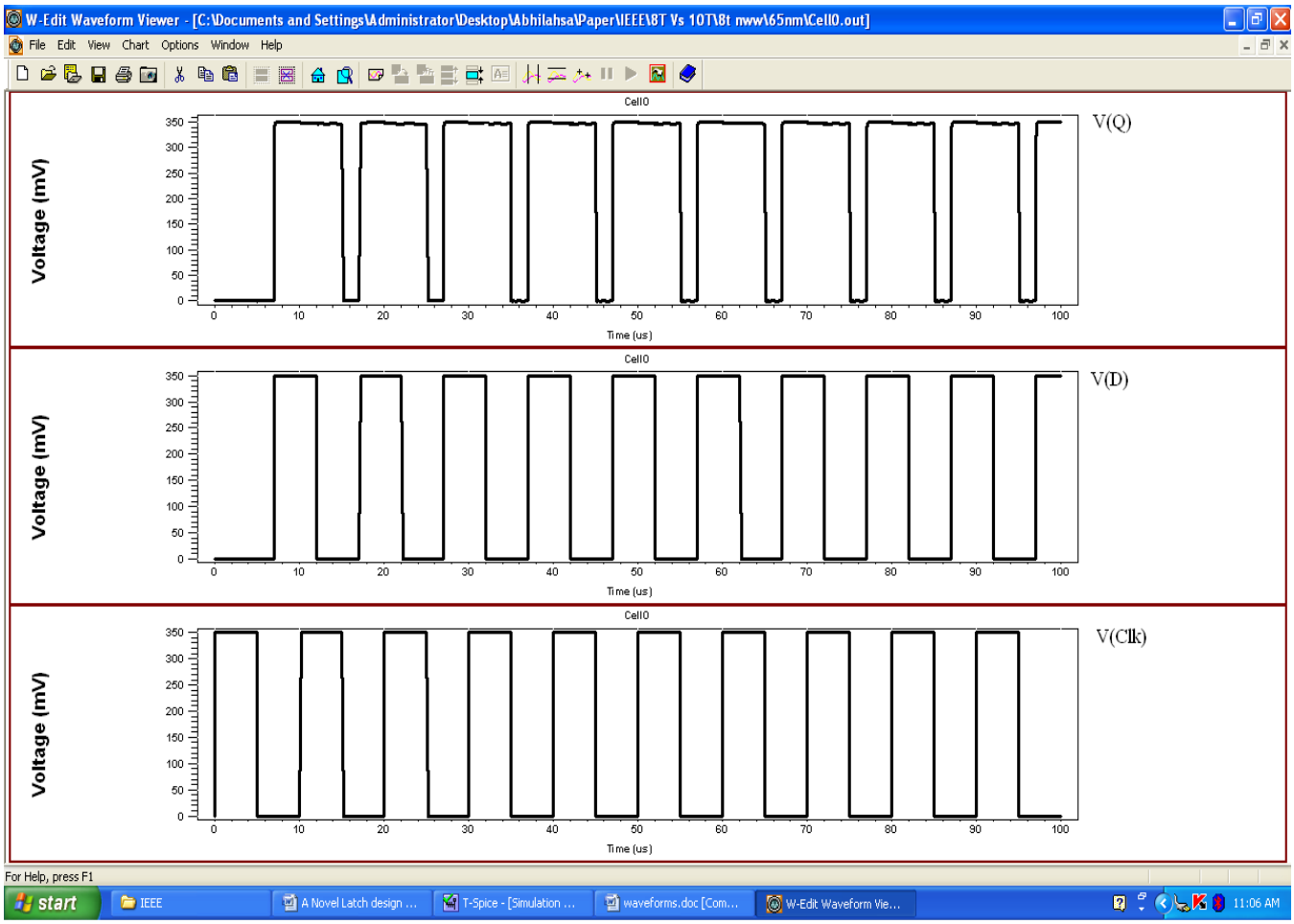


Fig. 3 Output waveform of the proposed 8T latch

Slight distortions are observed in the output waveform but these are acceptable within the noise margin. Since the latch is operating in the sub-threshold region, the power consumption will be very low.

In the conventional design, output change occurs, when clock signal is at positive level. During the calculation of the parasitic and input/output capacitances and voltages at various nodes of conventional design, clock level is set to high value. Output change occurs when the clock signal is at low level for the proposed design. So while checking voltages and capacitances at various nodes in proposed design the clock signal is set at zero level. Square waveform of frequency 1 MHz with initial value of 0.35 V at temperature of 25^{o}C is applied at the input data terminal of both the designs. Then we performed the dc analysis of the two circuits.

Table 1. Input and output resistances of the two designs

	8T	10T
Input (M Ω)	0.23387	0.10162
Output (M Ω)	0.64276	0.64751

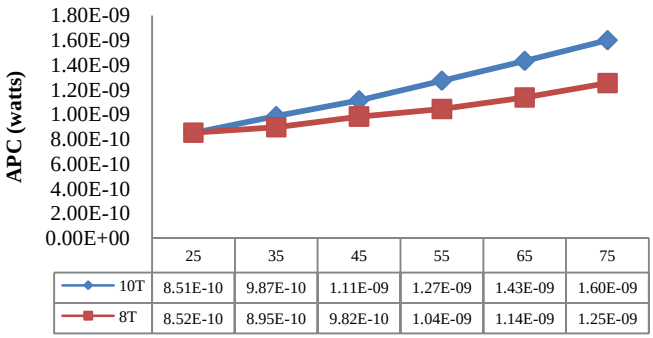
For the better operation of the device, large input resistance and small output resistance is required. The input resistance of the proposed design is larger and output resistance is smaller than the conventional design (TABLE I).

Table 2. Setup and Hold time of the two designs

	8T	10T
Setup time (µs)	0.101177	0.209185
Hold time (µs)	0.0685118	0.129437

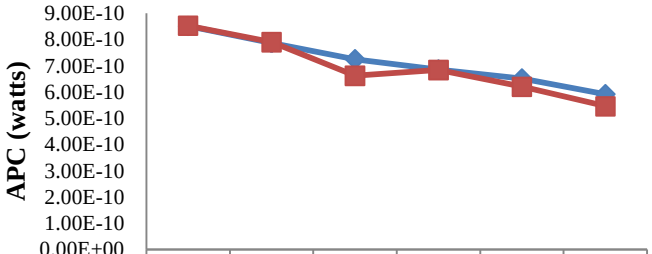
Whenever there are setup and hold time violations in any flip-flop or latch, it enters a state where its output is unpredictable. This state is known as meta-stable state (quasi stable state). For the correct operation of the flip-flop, the input value has to be maintained constant just before setup time (t_{setup}) and just after hold time (t_{hold}) of the triggering edge of the clock. For correct operation, it is easy to verify that the clock period has to be greater than the sum $t_{setup} + t_{hold}$.

During setup violation, the input is perceived as an average voltage value on the input capacitor. The average value is integration of the input voltage due to source over the time interval equal to setup time. This value might be meta stable value which will lead to undesirable outputs changing the mode of the operation transistors. For the output capacitor to get charged, it would take some finite amount of time, which is defined as hold time. Setup and hold time of the proposed design is less than the conventional design (TABLE II). The setup and hold time limits also the maximum operating frequency of the device and it is more in case of the proposed design.



	25	35	45	55	65	75
10T	8.51E-10	9.87E-10	1.11E-09	1.27E-09	1.43E-09	1.60E-09
8T	8.52E-10	8.95E-10	9.82E-10	1.04E-09	1.14E-09	1.25E-09

Fig. 4 Average power consumption at various temperatures (^{o}C) in 65nm technology

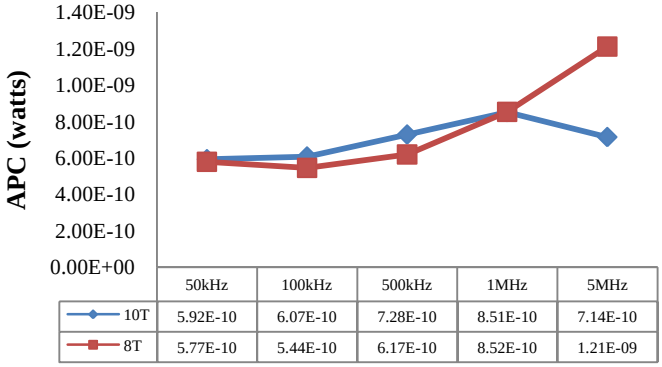


	0.35V	0.34V	0.33V	0.32V	0.31V	0.30V
10T	8.51E-10	7.86E-10	7.24E-10	6.85E-10	6.51E-10	5.91E-10
8T	8.52E-10	7.89E-10	6.61E-10	6.83E-10	6.19E-10	5.45E-10

Fig. 5 Average power consumption at various supply voltages (V) in 65nm technology

The average power consumption (APC) by the 8T design at various temperatures (25 ^{o}C to 75 ^{o}C) is less than the 10T latch (Fig. 4). From the figure it can be noticed that as the temperature increases the power consumption difference between the two designs increases, which shows that the proposed design is better at higher temperatures.

The supply voltage and the input voltages are kept always less than the threshold voltage of the NMOS and the PMOS transistors, thus to operate in sub-threshold region. The average power consumption by the 8T latch is found to be less than the conventional latch at supply voltages less than the threshold voltage (Fig. 5).



	50kHz	100kHz	500kHz	1MHz	5MHz
10T	5.92E-10	6.07E-10	7.28E-10	8.51E-10	7.14E-10
8T	5.77E-10	5.44E-10	6.17E-10	8.52E-10	1.21E-09

Fig. 6 Average power consumption at various frequencies in 65nm technology

Sub-threshold circuit operation is driven by currents much weaker than standard strong-inversion circuits, and so is characterized by longer propagation delays and limited to lower frequencies. Thus for low power applications, the devices work up to medium frequencies. The two designs are compared up to the 5MHz frequency and proposed design consumes less power (Fig. 6).

Delay increases with the increase in the temperature as can observed from the Table III. Delay variation is less in 10T latch as temperature increases but delay introduced is always less in the proposed latch at all the temperatures. Delay is proportional to the supply voltage and as its value increases, the delay increases. The delay is 100 times less in the proposed latch (Table IV).

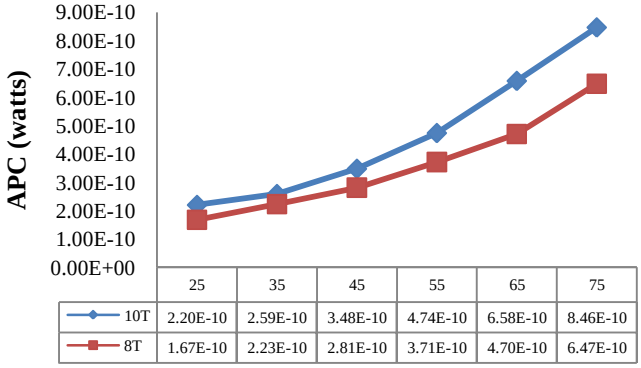
Similar results are obtained when the designs are compared using 45nm technology. The average power consumption by the proposed latch at various temperatures, supply voltages and frequencies is always less than the conventional latch (Fig. 7-9) in 45nm technology. Similarly the delay introduced in proposed design is hundred to thousand times less than the contending design (Table V-VI).

Table 3. Delay (in sec.) at various temperatures (^{o}C) in 65nm technology

Temperature (^{o}C)	10T	8T
25	5.0435e-007	3.0888e-009
35	5.0440e-007	3.2304e-009
45	5.0446e-007	3.4630e-009
55	5.0454e-007	3.7710e-009
65	5.0463e-007	4.1339e-009
75	5.0474e-007	4.5149e-009

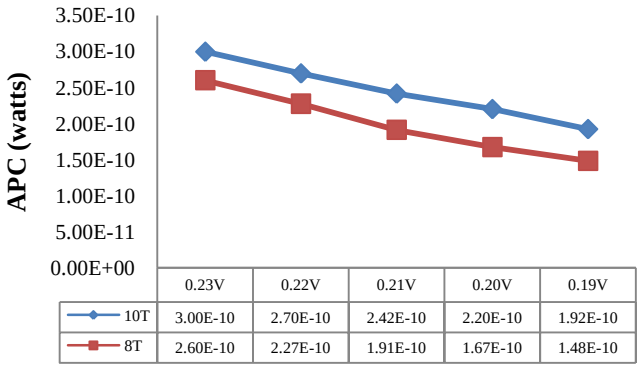
Table 4. Delay (in sec.) at various supply voltages (volt) in 65nm technology

Supply Voltage	10T	8T
0.35V	5.0435e-007	3.0888e-009
0.34V	5.0467e-007	3.8455e-009
0.33V	5.0492e-007	4.9182e-009
0.32V	5.0515e-007	4.4817e-010
0.31V	5.0573e-007	3.5308e-010
0.30V	5.0757e-007	2.8649e-010



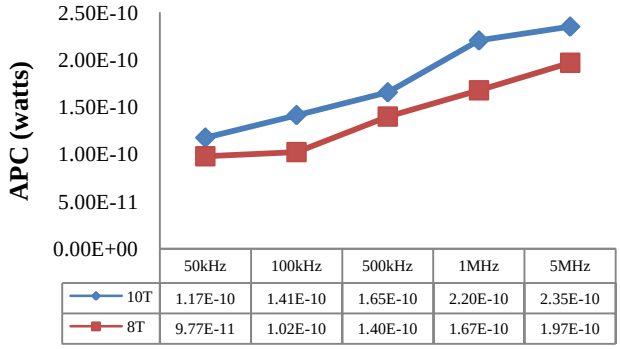
	25	35	45	55	65	75
10T	2.20E-10	2.59E-10	3.48E-10	4.74E-10	6.58E-10	8.46E-10
8T	1.67E-10	2.23E-10	2.81E-10	3.71E-10	4.70E-10	6.47E-10

Fig. 7 Average Power Consumption at various temperatures (^{o}C) in 45nm technology



	0.23V	0.22V	0.21V	0.20V	0.19V
10T	3.00E-10	2.70E-10	2.42E-10	2.20E-10	1.92E-10
8T	2.60E-10	2.27E-10	1.91E-10	1.67E-10	1.48E-10

Fig. 8 Average Power Consumption at various supply voltages in 45nm technology



	50kHz	100kHz	500kHz	1MHz	5MHz
10T	1.17E-10	1.41E-10	1.65E-10	2.20E-10	2.35E-10
8T	9.77E-11	1.02E-10	1.40E-10	1.67E-10	1.97E-10

Fig. 9 Average Power Consumption at various frequencies in 45nm technology

Table 5. Delay (in sec.) at various temperatures (^{o}C) in 45nm technology

Temperature (^{o}C)	10T	8T
25	5.5553e-007	3.2987e-008
35	5.2888e-007	2.8742e-008
45	5.1818e-007	2.4455e-008
55	5.1704e-007	2.0920e-008
65	5.1646e-007	1.8026e-008
75	5.1479e-007	1.4421e-008

Table 6. Delay (in sec.) at various supply voltages (volt) in 45nm technology

Supply Voltage	10T	8T
0.23V	5.1892e-007	2.0715e-008
0.22V	5.2894e-007	2.3595e-008
0.21V	5.4411e-007	2.7832e-008
0.20V	5.5553e-007	3.2987e-008
0.19V	6.0102e-007	4.9428e-008

From the earlier mentioned comparisons, it is clear that the one of the parameter in VLSI design, i.e., power delay product of the proposed design is always better than the conventional design irrespective of technology used or parameters (e.g., temperature, supply voltage and frequency) incorporated.

4. CONCLUSION

The proposed design of 8-transistor latch is compared and found better than the conventional latch of 10-transistor in terms of power consumption, delay and power delay product at the variation of the parameters, i.e., supply voltage, frequency and temperature. The proposed design is also technology independent as it operates better in two different technologies, i.e., 45nm and 65nm. The tremendous decrease in delay reported in the proposed level triggered design during the simulation makes it better than the conventional design. The 8T design uses two less transistors and thus area efficient too. This design will certainly improve the performance of the low power devices.

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