FPGA Implementation of Voltage Sharing Strategy for Series Connected Sepics

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ABSTRACT
The paper orients to develop a strategy, with a view to ensure that the output voltage is equally shared among a number of Single Ended Primary Inductance Converters (SEPICs), in addition to ensuring regulation of the load voltage. It attempts to exploit the robustness of a Variable Structure Controller (VSC) to offset the circuit parasitic and extract a stable output irrespective of the variations in input voltage, circuit parameters and/or load. The methodology envisages characterizing the desired time response and acclaiming an acceptable steady state and transient results. It involves the use of a Field Programmable Gate Array (FPGA) to implement the proposed scheme and illustrate its practical viability. The performance evaluated through MATLAB based simulation is adequately validated using a suitable prototype to project its applicability over a preferred operating range.

General Terms
DC-DC Converter, Multiple Connection, Control Strategy

Keywords
SEPIC, VSC, Voltage sharing, Time response, FPGA

1. INTRODUCTION
DC-DC converters continue to find wide spread use in industrial, residential and aerospace domains. The extensive automation prevalent in the industry calls for higher output voltages besides requiring the power supplies to inherit higher power densities. However it may be difficult for a single entity to withstand the high output voltage and high input current stresses [1].

Owing to the rapid expansion of high-speed traction systems, industrial drives, and undersea observatories, series connected converters appear to emerge as a practical configuration in the present day power supply system[2].The immediate advantages of multiple connections are the ease of thermal design, enhanced overall system reliability due to reduced thermal and electrical stresses on the power devices and components, lowered cost of the system and a facility to expand the capability of the system [3].

The intrinsic variations in the parameters in appropriately connected identical converters are likely to produce an unbalanced output voltage in addition to creating a nonlinear behavior for the circuit variables. The non-uniform distribution of output voltages may cause one or more of the converters to suffer from thermal stresses and end up in the unreliable operation of the multiple connected systems. Though unified approaches of voltage distribution control are available for such architectures [4] & [5], a series-connected converter power system still augurs the need for more refined methodologies to ensure a robust, stable and reliable performance.An Input-parallel and output-series (IPOS) modular based DC-DC converter with one common filter has been suggested. It has been found to enjoy the advantages of low cost, high efficiency and rapid dynamic response [6].The performance of the IPOS (input parallel and output series) full bridge DC-DC converters with different module parameters has been studied and the sensitivity of the output voltage error to the maximum parameter variance of circuit components analyzed [7].

The control strategies aimed at achieving proper sharing of the voltage and/or current at the input or output sides in DC-DC conversion systems have been discussed and the relationship between sharing of input voltages/currents and that of output voltages/currents presented [8]. A novel control strategy, using which DC-DC converter modules connected in series at the input side for higher input voltages and in parallel at the output side for higher output currents has been developed. It has been found to ensure that each module equally shares the total input voltage and the output current [9].A generalpurpose sliding-mode controller that provides robustness and higher speed of response against supply, load and parameter variations has been described [10]. A new control strategy through which the dynamic current reference has also been derived to mitigate the large load/input voltage variation effects in a Buck converter has been explained [11]. An adaptive nonsingular terminal sliding mode control scheme has been proposed to facilitate the response of the converter reach steady state within a limited time [12].The design and implementation of a power management strategy for a Buck converter has been realized through an FPGA processor[13].

However the role of nonlinear control strategies evinces a renewed interest in its attempt to establish a better platform for the sophistication of the power electronic utilities.

2. PROBLEM FORMULATION
The primary objective echoes to evolve a control algorithm that enables to share the load voltage equally among the SEPICs connected in series at the output through structural modifications. The scope includes implementing the strategy through a FPGA based prototype to extricate its suitability for use in the practical domain.

3. PROPOSED STRATEGY

The series connection facilitates the use of lower rated power converters in order to tailor it to meet the growing power demands. The SEPIC system under study is constituted of number of identical units connected in series at the output. Each individual converter as seen from Fig.1 is powered from a separate DC source and can be used to serve in either the Buck or Boost modes.

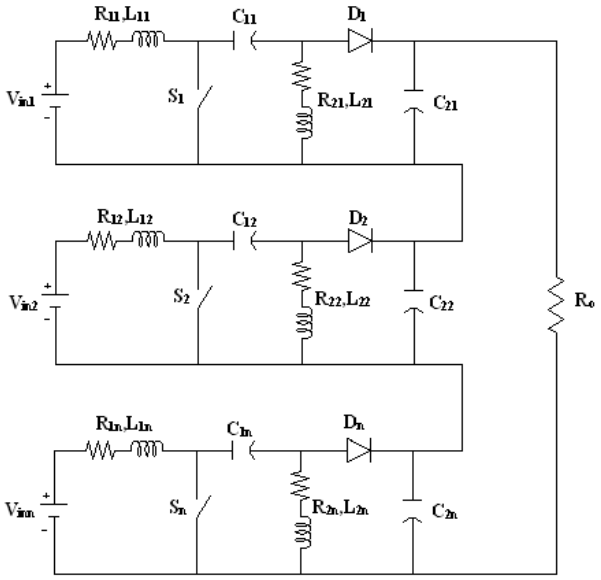

Fig.1 Power Module

The first inductor seen in each unit of the multiple connected power module are charged from the input voltage source when the power switch in all the series connected units is turned ON, while the second set of inductors draw energy from the initially charged first capacitors. The load current however in this mode is provided by the set of second capacitors in each individual converter.The stream of the first set of inductors charges the first bunch of capacitors in addition to jointly supporting the load, in the event of the power switches being allowed to turn OFF. It enables the energy stored in the second set of inductors to be transferred to the set of second capacitors besides augmenting the needs of the load.

4. MODELING

Power Electronic Converters include circuits that necessitate specific modeling through differential equations to express the cohesive operational behavior. It is essential to include the effects of discontinuities and the consequent non-linearities in the process of designing a control algorithm. The mechanism facilitates to perform a detailed evaluation of its modes and associate the required corrective measures to suit the application demands. The state space model of Series connected SEPIC can be described by

$$\left.\begin{aligned}
\dot{i_{1j}} &= -\frac{R_{1j}}{L_{1j}} i_{1j} - \frac{1}{L_{1j}} V_{c1j} - \frac{1}{L_{1j}} V_{oj} - \frac{1}{L_{1j}} V_{inj} \\
\dot{i_{2j}} &= -\frac{R_{2j}}{L_{2j}} i_{2j} - \frac{1}{L_{2j}} V_{c1j} + \frac{1}{L_{2j}} V_{oj} \\
\dot{V_{c1j}} &= \frac{1}{C_{1j}} i_{1j} + \frac{1}{C_{1j}} i_{2j} \\
\dot{V_{oj}} &= \frac{1}{C_{oj}} i_{1j} - \frac{1}{C_{oj}} i_{2j} - \frac{1}{R_{oj}\, C_{oj}} V_{oj}
\end{aligned}\right\} \quad \text{.... (1)}$$

Where

i_{1j}, i_{2j}, V_{c1j} and V_{oj} are the state variables

j = 1, 2…n

The capacitor voltage in each of the units can be represented by

$$V_{oj} = \frac{1}{n-1} \sum_{\substack{k=1 \\ k \neq j}}^{n} V_{ok} \quad \text{..... (2)}$$

j=1, 2 …..n

5. CONTROL ALGORITHM

The classical control appears to be ill suited on account of the fact that the coefficients of the control law are pre-tuned for a specific equilibrium point. Therefore the role of a Variable Structure System (VSS) that is characterized by a discontinuous action is sought to effect a structural change in the system upon reaching a set of switching surfaces [14]. The significant merit is that under certain conditions it is invariant, more than being robust, with respect to system parameter variations and external disturbances [15].

TheVSC theory revolves around two phases to ensure that the system reaches steady state in a finite time. While the first phase develops an equilibrium surface to characterize the state trajectory, the second invokes a discontinuous control law to force the variables to move on the sliding surface.The switching instants are determined through an appropriate design of sliding or switching surface to be guaranteed of asymptotic stability.

The switching function for the proposed control is given by

$$\sigma(X) = \sigma^{\cdot}(X) = 0 \text{..... (3)}$$

The control of series connected converters requires a strategy with the ability of regulating the output voltage and equally sharing it among the series connected converters. The discontinuous control law u_j of the j th converter module that turns ON the power switch through a sliding surface defined by

$$\sigma_j \left(e_V, \dot{e_V}, e_{V_{oj}} \right) = \frac{1}{c} i_c + \alpha e_V + \beta_j e_{V_{oj}} \text{..... (4)}$$

Where the gain constants α and β_j are required to be greater than one to guarantee the stable operation of the converter.

$e_{V_{oj}}$ is the j[th] voltage error defined by

$$e_{V_{oj}} = \frac{1}{n}\left\{(n-1) * V_{oj} - \sum_{\substack{k=1 \\ k\neq j}}^{n} V_{oj}\right\} \quad \text{..... (5)}$$

Where j = 1,2, ….n

n is the number of series connected converters

The discontinuous control law is stated as

$$U_j = \begin{cases} 1 & \sigma_j < 0 \\ 0 & \sigma_j > 0 \end{cases} \quad \text{..... (6)}$$

Where U_j is the j[th] component of control

σ_j is the j[th] component of the n sliding surfaces

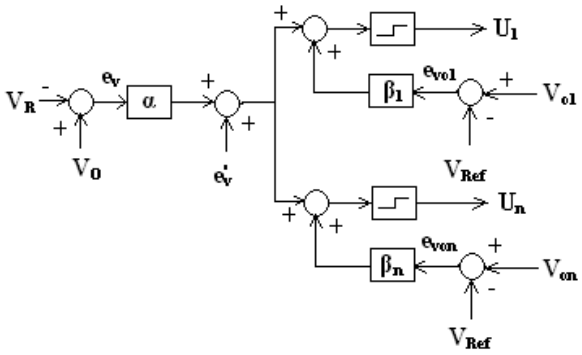

Fig. 2 Control Algorithm

The proposed technique illustrated in Fig.2 is governed by

$$V_{Ref} = \frac{1}{n}\sum_{k=1}^{n} V_{ok} \quad \text{..... (7)}$$

The sliding mode exists if all the state trajectories are directed towards the surface. The mathematical form for such a condition is given by

$$\lim_{\sigma_j \to 0+} \frac{\partial \sigma_j(X)}{\partial X} < 0 \quad \text{... (8)}$$

$$\lim_{\sigma_j \to 0-} \frac{\partial \sigma_j(X)}{\partial X} > 0 \quad \text{... (9)}$$

The above equations (8) and (9) can be alternatively stated as

$$\lim_{\sigma_j \to 0} \sigma_j \dot{\sigma_j} < 0 \quad \text{..... (10)}$$

The expression in equation (10) explains the condition for the existence of sliding regime on the surface
$\sigma_j = 0$

6. SIMULATION RESULTS

The performance of two Buck/Boost SEPICs connected in series at the output is examined through simulation on a MATLAB – SIMULINK platform. The identically rated converters are constituted of elements with the following specifications R_1 = 0.1Ω, L_1 = 200 µH, R_2 =0.2Ω, L_2 = 510 µH, C_1 = 47 µF, C_0 = 200 µF. The study envisages arriving at a stable output of 230 V from an input supply of 350 V for Buck converter and 350 V in the case of Boost from a fixed input of 230 V. It is proposed to test the converter over a range of resistive loads when the power switches are operated at a switching frequency of 50 KHz.

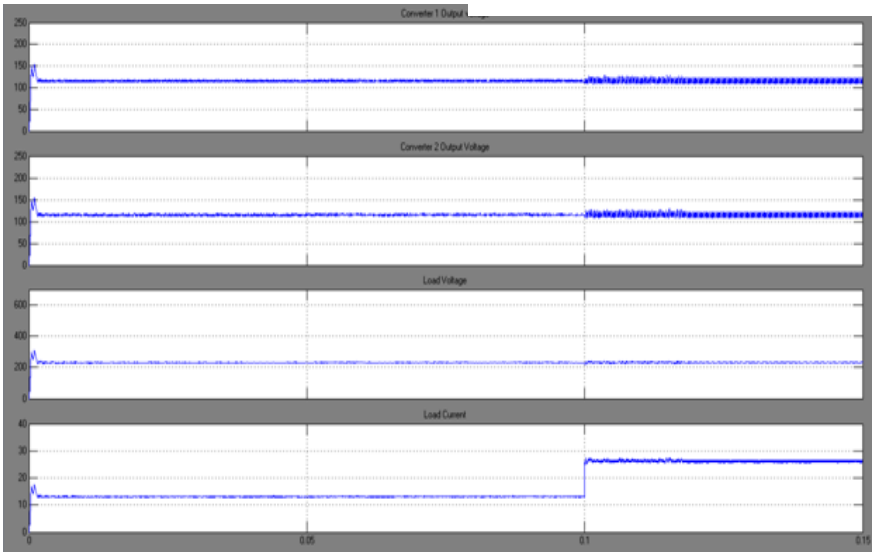

Fig.3. Steady State and Transient Response in BUCK Mode

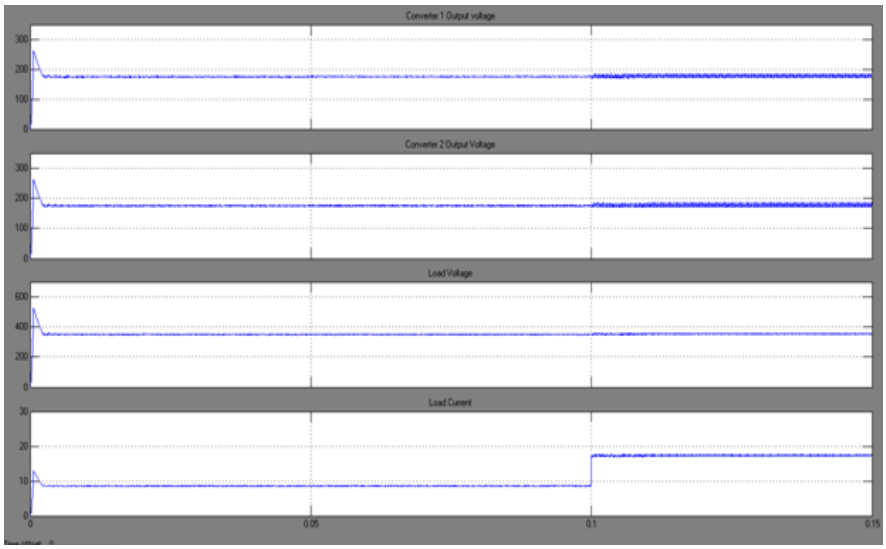

Fig.4. Steady State and Transient Response in BOOST Mode

The closed loop individual output voltage of converters, load voltage and load current of the series connected Buck and Boost converters corresponding to a load power of 3 KW are shown in Figs. 3 & 4 respectively. The regulating phenomena and the equal sharing of the output voltage between the two units are brought out both in the event of sudden changes in supply and load introduced at 0.05 and 0.1 seconds respectively. The VSC encompasses with it the mechanism to choose the appropriate value of the duty cycle to restore the desired load voltage.

The figures 5 through 12 relate the time response characteristics of both Buck and Boost modes of the series connected SEPIC system. It follows that the VSC offers a lower overshoot, smaller rise, peak and settling times than that of the Average Voltage Controller (AVC) over the entire operating range. Owing to the fact that the VSC enables the SEPIC system to enjoy a superior performance, allows it to claims its use in critical applications.

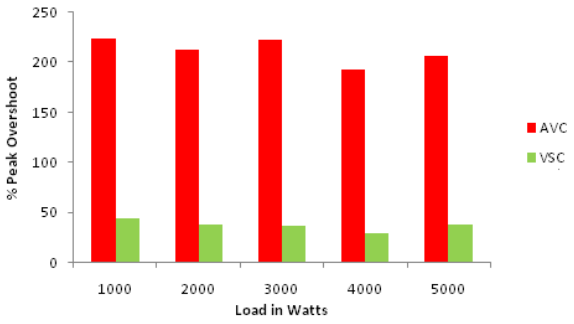

Fig.5. Load Vs % peak over control

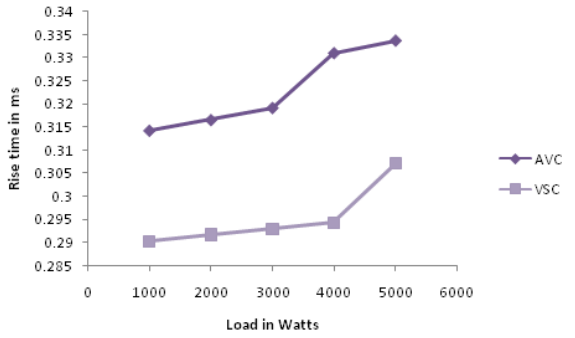

Fig.6. Load Vs Rise time

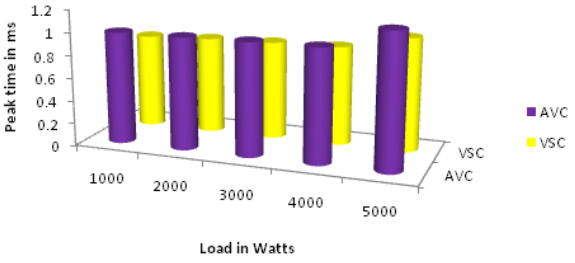

Fig.7. Load Vs Peak time

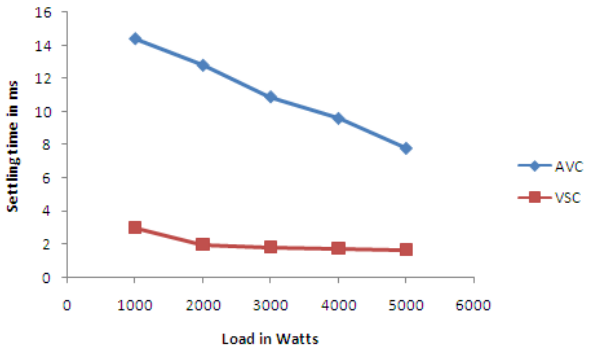

Fig.8. Load Vs Settling time

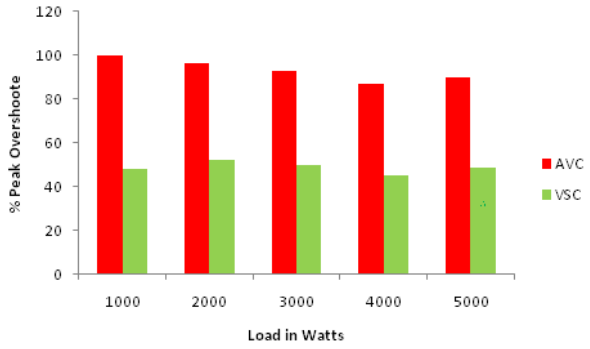

Fig.9. Load Vs Peak over shoot

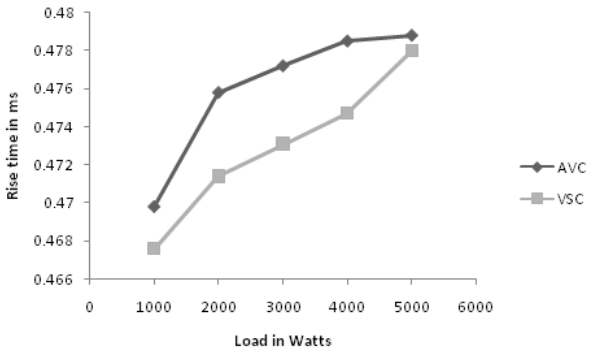

Fig.10. Load Vs Rise time

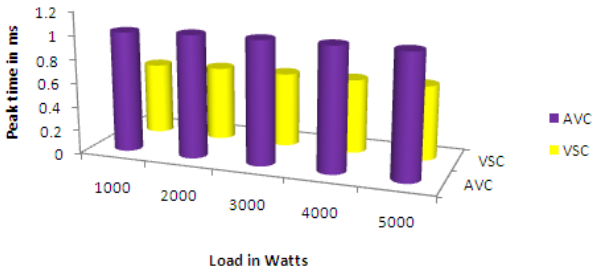

Fig.11. Load Vs Peak time

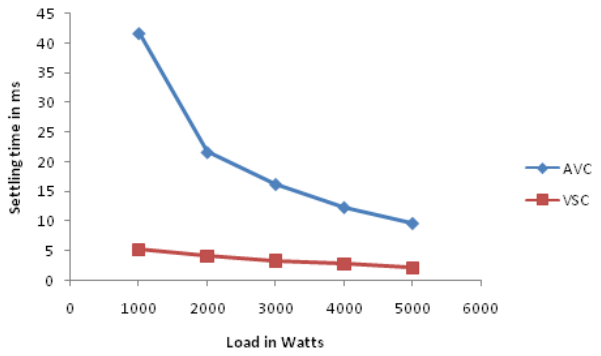

Fig.12. Load Vs Settling time

7. HARDWARE IMPEMENTATION

The proposed methodology is investigated using an experimental arrangement over similar ratings as that used in simulation through the same operating range. It acquires the role of a FPGA processor to generate the PWM pulses for the IGBT switches in tune with the design of the control strategy. The VSC algorithm is invoked to elaborate equal sharing of output voltage among the series connected string besides regulating the load voltage. FPGAs contain programmable logic components called logic blocks and a hierarchy of reconfigurable interconnects that extend the blocks to be wired together. The logic blocks include memory elements and can be used to create any logical function that an ASIC performs. The field programmable configuration is generally specified using a hardware description language and enjoys the facility to serve multiplicity of functions in system specific applications. It is designed using VHDL in a Xilinx integrated service environment and the VSC algorithm coded with the help of a SRAM-FPGA-based Xilinx family Spartan-3 XC3S400-4-pq208.The flow schematic involving the generation of appropriate firing pulses for the IGBTs is outlined through Fig.13

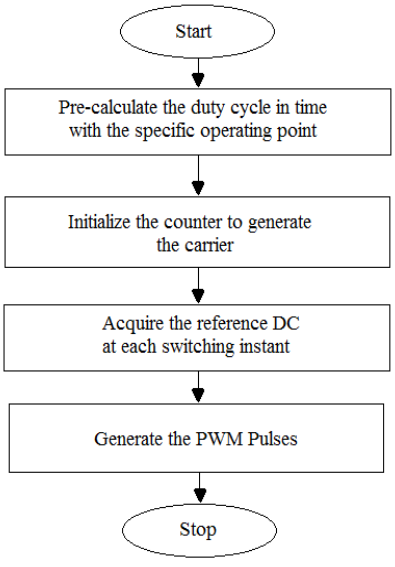

Fig.13 Flow Chart

Fig.14.Prototype

The photograph displayed in Fig.14 explains the hardware module constructed for testing the applicability of the scheme. The PWM pulses for both the IGBT switches captured through RIGOL Digital Storage Oscilloscope (DSO) for both Buck and Boost modes at the same operating point of 3 KW are displayed in Figs.15 &16 respectively. The load voltage and equally shared output voltage waveforms of both the converters obtained for the same operating point using an attenuator probe of 1:10 in the Buck and Boost modes of operation are depicted in figs.17 and 18.

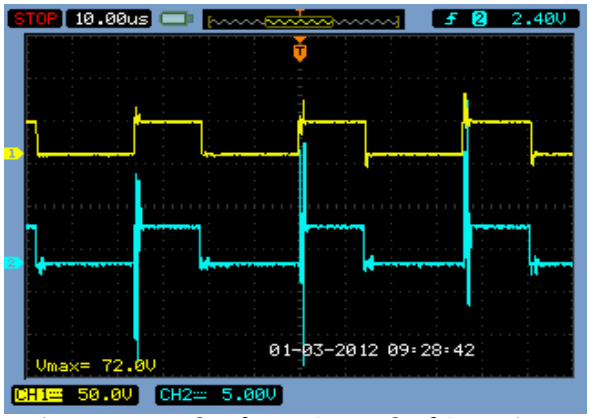

Fig.15. PWM Pulses for BUCK Mode of Operation

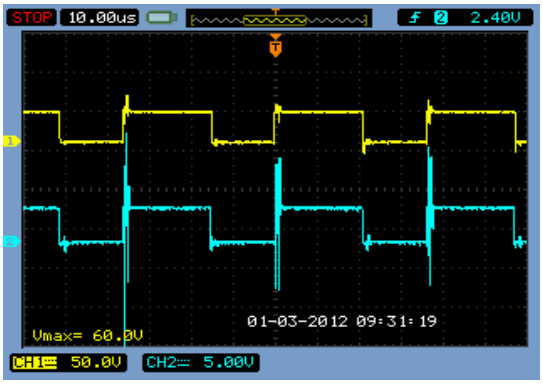

Fig.16 PWM Pulses for BOOST Mode of Operation

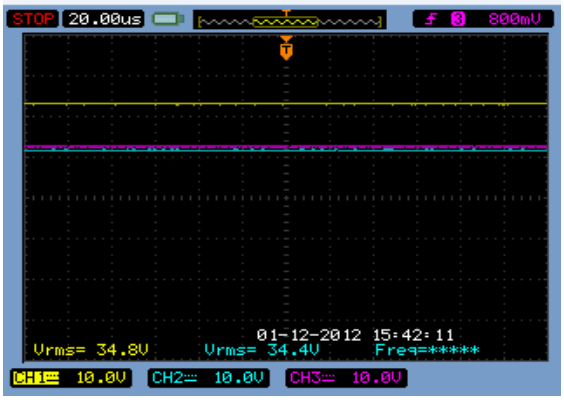

Fig.17 Converter 1, Converter 2 and Output Voltages in BUCK mode

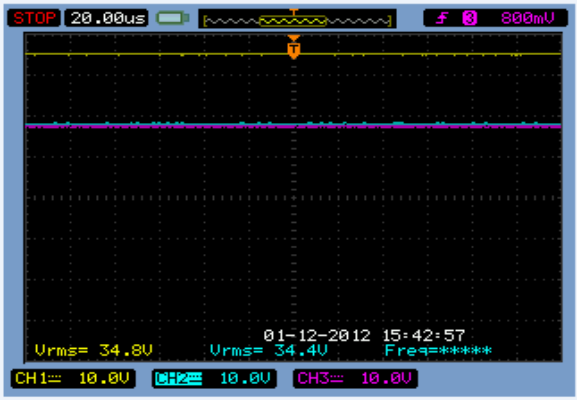

Fig.18 Converter 1, Converter 2 and Output voltages in BOOST mode

With the load power allowed to vary the readings measured in simulation and using the prototype are compared in Tables1 & 2 for Buck and Boost modes to validate the MATLAB results and justify the superior performance of the SM controller. It is observed that values are in close agreement with each other and the voltages sharing phenomena are highlighted across the entire operation range.

Table 1. Performance Comparison for BUCK mode

LOAD (KW)	CONVERTER 1 OUTPUT VOLTAGE (Volts)			CONVERTER 2 OUTPUT VOLTAGE (Volts)			LOAD VOLTAGE (Volts)			LOAD CURRENT(Amps)		
	SIMULATION		HARD WARE	SIMULATION		HARD WARE	SIMULATION		HARD WARE	SIMULATION		HARD WARE
	AVC	VSC		AVC	VSC		AVC	VSC		AVC	VSC	
1000	114.95	115.00	114.50	114.95	115.00	114.50	229.90	230.00	229.00	4.347	4.359	4.30
2000	114.90	114.96	114.00	114.90	114.96	114.00	229.80	229.92	228.00	8.699	8.703	8.60
3000	114.85	114.90	113.40	114.85	114.90	113.40	229.70	229.80	226.80	13.060	13.071	12.80
4000	114.78	114.87	113.00	114.78	114.87	113.00	229.56	229.74	226.00	17.436	17.444	17.40
5000	114.73	114.82	112.20	114.73	114.82	112.20	229.46	229.64	224.40	21.805	21.824	21.50

Table 2. Performance Comparison for BOOST mode

LOAD (KW)	CONVERTER 1 OUTPUT VOLTAGE (Volts)			CONVERTER 2 OUTPUT VOLTAGE (Volts)			LOAD VOLTAGE (Volts)			LOAD CURRENT(Amps)		
	SIMULATION		HARD WARE	SIMULATION		HARD WARE	SIMULATION		HARD WARE	SIMULATION		HARD WARE
	AVC	VSC		AVC	VSC		AVC	VSC		AVC	VSC	
1000	174.95	175.00	174.50	174.95	175.00	174.50	349.90	350.00	349.00	2.857	2.859	2.80
2000	174.89	174.95	174.10	174.89	174.95	174.10	349.78	349.90	348.20	5.717	5.720	5.60
3000	174.83	174.90	173.60	174.83	174.90	173.60	349.66	349.80	347.20	8.581	8.586	8.40
4000	174.76	174.83	173.20	174.76	174.83	173.20	349.52	349.66	346.40	11.448	11.451	11.30
5000	174.70	174.76	172.30	174.70	174.76	172.30	349.4	349.52	344.60	14.322	14.326	14.40

8. CONCLUSION

A VSC based methodology suitable for a multiple connected SEPIC has been articulated to illustrate uniform sharing of output voltage among the converters connected in series in addition to regulating its load voltage. The merits of the strategy have been realised in terms of an improved time response performance. The ability of the variable structure approach to transcend the desired transient response has been elucidated through simulation results. The use of FPGA to espouse its suitability for such methodologies has been substantiated. The scheme implemented through an appropriate hardware has been used to display the credibility of the proposed approach for use in modular operations and will go a long way in enlarging the scope of such converter systems.

9. ACKNOWLEDGEMENT

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