A Novel Design Method of Two-stage CMOS Operational Transconductance Amplifier used for Wireless Sensor Receiver

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ABSTRACT
Operational transconductance amplifier (OTA) is one of the most significant building-blocks in integrated discret-time filters used in analog to digital converter (ADC) for Sigma-delta converter. In this paper we designed a novel design method of two-stage CMOS amplifier in AMS 0.35µm technology. P-Spice simulation results confirm the proposed OTA circuit. In fact, we achieved a gain band width (GBW) equal to 55 MHz, Cut-off frequency of 85 KHz and 57 dB gain (Av). In addition our new method allowed us to reduce settling time (S_t) to 15.6 ns and a slew rate (SR) of 0.1 V/µs at ±1.5V supply voltage. Eventually we have also succeeded in reducing the average power consumption to 1.65 mW while driving 3 pF load capacitor.

General Terms
Microelectronic Components Circuits Devices & Systems

Keywords
Wireless sensor, Operational amplifier, CMOS OTA Design.

1. INTRODUCTION
In the last few years, wireless sensor networks [1-2] (WSNs) have increased rapidly and become one of the most interesting areas of research [3]. It is composed of a number of wireless sensor nodes which form a sensor field and a sink. To ensure high performance of these large numbers of nodes they require low-cost, low-power, and capacity of communication at short distances in order to perform limited computation and communicate wirelessly in the WSNs [4-5].

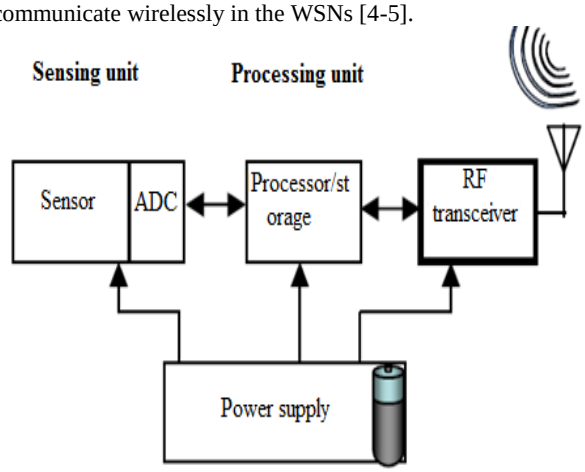

Fig. 1: Block diagram of a sensor node

Many applications are included in industrial and home automation, medical monitoring, automatic meter reading, alarms and agriculture. The fig. 1 shows the block diagram of a sensor node.

It is composed of four blocks: power supply, communication, processing unit, and sensors.

The power supply block has the purpose to power the node and usually consists of a battery. The communication block is an RF transceiver to provide a bidirectional wireless communication channel.

The processing unit is composed of an internal memory to store data, applications programs, and a microcontroller unit (MCU) to process data. The sensing unit block links the sensor node to the physical world and transmits a signal to Analog-to-Digital Converter (ADC) [6].

The paper is organized as follows.

Section II presents the conventional two-Stage operational amplifier transconductance (OTA) used for wireless sensor receiver. In section III the design of Modified tow Stage Miller OTA circuit with cascode current source is presented. Modified two-stage Miller OTA with designed current source is presented in section IV, while their full comparison is given in section V in which the performance of each OTA is indicated in table 9. Conclusion is drawn in Section VI.

1.1 Receiver architectures
The main objective of a receiver for wireless communication applications is to recover the base band signals that are modulated on a carrier wave at radio frequencies. The design of a high performance, low power integrated radio frequency receiver in mainstream silicon technologies CMOS is a very challenging task involving numerous tradeoffs during the design process, especially between noise, linearity and power consumption. In this paper we introduce with a description of the direct conversion receiver or homodyne which is the most widely used receiver architecture for highly integrated and low-power consumption. This receiver architecture directly down converts the signal to base band rather than converting it into an intermediate frequency (IF) first, and image rejection is no longer necessary in this approach. The block diagram of a direct conversion or homodyne architecture is illustrated in fig. 2.

In the first, the RF signal that comes out of the antenna is filtered by the band pass filter (BPF).Then, it is amplified by the low noising amplifier (LNA) before being down converted directly to base band along parallel in-phase (I) and quadrature (Q) signals.

The frequency translation is performed by using two mixers using 0° and 90° phase shifted local oscillator (LO) signals. Finally, the I and Q base band signals are amplified and low pass filtered before the analogue to digital converter (A/D) conversion is intervened.

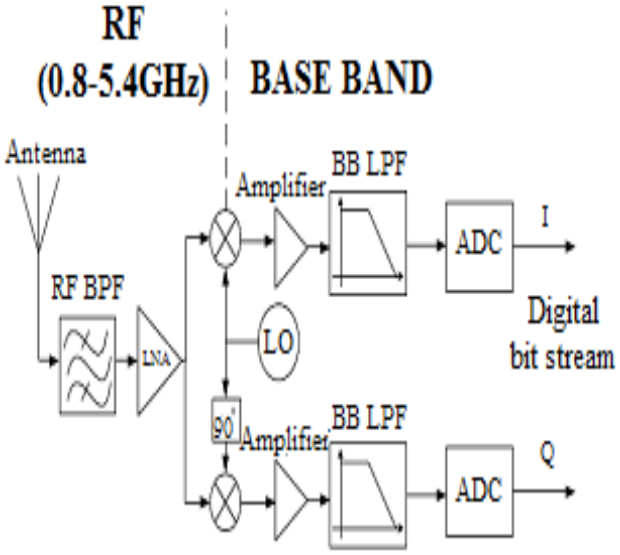

Fig. 2: Block diagram of a direct conversion or homodyne architecture

To achieve the objective cited above, all aspects of the receiver [7] and radio system need to be addressed as shown in table 1. (Base band, Modulation scheme, hopping bandwidth, data rate, Sensitivity, Noise fig., IIP3, P-1, SFDR, BDR...).

Table 1 : Sensor receiver specifications

Base band frequency (f_b)	80 KHz
Modulation scheme	BFSK
Hopping bandwidth	7 MHz (863-870) MHz
Data rate (D)	20 Kbps
BER	10-3 @ Eb/No=11dB
Direct conversion receiver	
Sensitivity (S)	-102 dBm
Noise fig. (NF)	18 dB
IIP3	≥ -8 dB
P-1	≥ -18 dB
SFDR	61 dB
BDR	84 dB

To characterise the sensor thermal noise (N_t) is given by:

$$N_t = -174 + 10\log_{10}(f_b) = -125\ dB$$

Another two elements defining sensor are SNR_{in}, SNR_{out} (Signal to Noise Ratio) which are based on the following formula:

$$SNR_{in} = S - N_t = 23\ dB$$

$$SNR_{out} = \left(\frac{E_b}{N_0}\right)_{dB} - 10\log_{10}\left(\frac{f_b}{D}\right) = 5\ dB$$

As shown in fig. 3, (Eb /N0) is equal to 11 with Noncoherent Frequency Shift Keying "NC -BFSK" to attenuate a bit error rate (BER) of 10-3 which is based on the following formula:

$$BER_{NC-BFSK} = \frac{1}{2} \times e^{-\frac{1}{2}\frac{E_b}{N_o}}$$

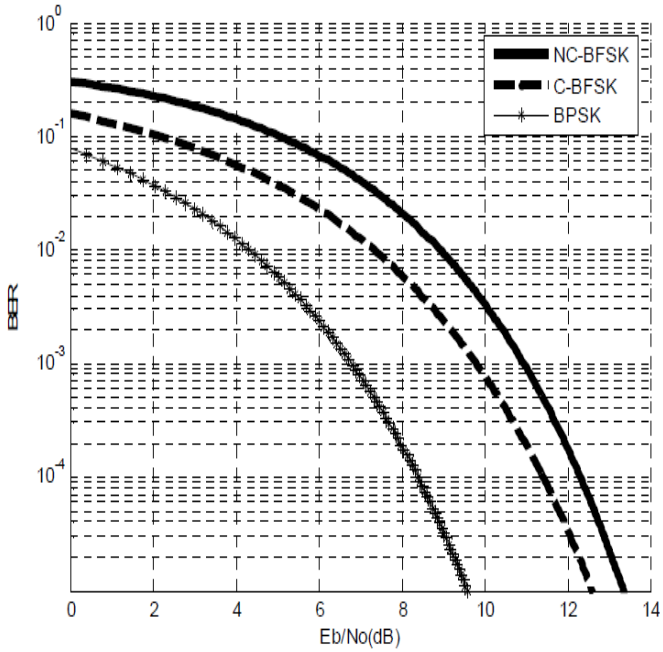

Fig. 3: Bit error rate (BER) for BPSK, C-BFSK and NC-BFSK

The Noise fig. is defined as:

$$NF = \frac{SNR_{in}}{SNR_{out}} = SNR_{in}(dB) - SNR_{out}(dB) = 18\ dB$$

The effective number of bits of sigma-delta (N_{eff}) converter is given by [21]:

$$N_{eff} = \frac{1}{2}\log_2\left[(2N-1)^2(2L+1)OSR^{2L+1}/(\pi)^{2L}\right]$$

Where N represents number of bits of the quantization circuitry (N = 1), L represents order of modulator (L = 1) and OSR means Over Sampling Ratio which is based on the following formula:

$$OSR = \frac{F_s}{2 \times f_b}$$

If we choose an OSR equal to 64, we obtain an effective number of 8.14 bits. F_s is the sampling frequency which is calculated to 10.240MHz, and f_b means base band frequency (80 KHz). The number 8.14 bits is the theoretical number because errors in the structure of parasites modulator reduce the SNR and therefore the number of bits, and to ensure low power and minimum consumption the number of bits is chosen as 8 bits.

1.2 Sigma-Delta analog to digital converter (ADC)

Sigma-Delta (εΔ) analog to digital converters (ADC) have been successful in realizing high resolution consumer. (εΔ) converters are well suited for low bandwidth, high-resolution acquisition, and low cost, making them a good ADC choice for many applications such as wireless sensor. As shown in fig. 4, Sigma-delta converters combine an analog sigma delta modulator with a more complex digital filter. Accuracy depends on the noise and linearity performance of the modulator, which uses high performance operational amplifiers transconductance.

The operational transconductance amplifier (OTA) is an important component for various analog circuits and systems. It is widely used as active element in variable gain amplifiers, data converters, interface circuits, continuous time oscillators, switched capacitor filters and sample and hold circuits. Depending on system needs, OTA circuit with high open loop gain, high slew rate and large bandwidth is highly desired. The high slew rate and bandwidth ensure a small settling time, whereas the high gain improves the settling accuracy. For this reason we design here a novel design technique of (OTA).

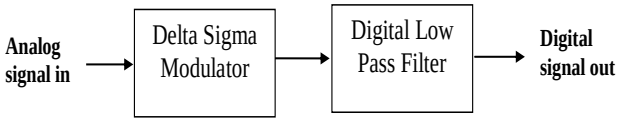

Fig. 4 : Block diagram of the A/D converter

On the one hand, dynamic range is defined as [8]:

$$DR_{dB} = 10\log_{10}\left[\frac{3}{2}\left(2^{N}-1\right)^{2}\frac{(2L+1)OSR^{2L+1}}{\Pi^{2L}}\right]$$

On the other hand, the dynamic range of an n_b-bit Nyquist rate ADC is given by [9]:

$$DR = 6.02\times n_b + 1.76$$

For an 8-Bit ADC the dynamic range from the above formula is 49.92 dB. Oversampling ratio (OSR) to achieve DR = 49.92 dB is calculated to be 59.96. To simplify the decimator design, the oversampling ratio is usually chosen in powers of 2 and hence 64 has been chosen as the oversampling ratio which is indicated in the previous paragraph.

2. CONVENTIONAL TWO-STAGE CMOS OTA

2.1 Design and performance

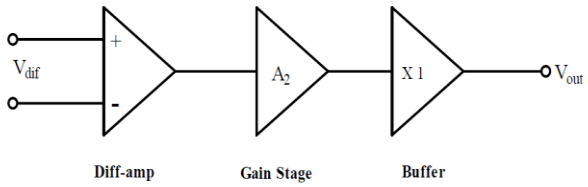

Fig. 4: Block diagram of conventional two-stage op-amp with output buffer

In order to have high performance ADC and switched capacitor filters, we need OTAs which have both high (DC) gain and a high gain bandwidth product (GBW) [10].

Generally, Operational amplifiers (op-amp) have sufficiently high voltage gain so that when the negative feedback is applied, the closed-loop transfer function can be made practically independent of the gain of the op-amp. This principle is employed in many useful analog circuits and systems. The primary requirement of an op-amp is to have an open loop gain which is sufficiently large to implement the negative feedback concept. One of the popular op-amp is a two-stage Miller op-amp shown in fig. 4. This last is made up of three stages even though it is often referred to as a "two-stage" op-amp, ignoring the buffer stage. The latter introduces an important concept of compensation. The primary goal of compensation is to maintain stability when negative feedback is applied around the operational amplifier.

The basic circuit diagram of two-stage Miller CMOS differential amplifier is often desired as the first stage in an op-amp due to its differential input to single-ended output conversion and its high gain. The input devices of the differential pair are formed by P-channel MOSFETs M1 and M2. Either N-channel MOSFET (NMOS) or P-channel (PMOS) input devices can be used. However, PMOS input devices are used more often thanks to improved slew rate and reduced 1/f noise [11]. The use of PMOS input devices also provides reduced power supply rejection thanks to the current mirrors, and low sensitivity to change in power supply voltage. This first stage of op-amp also had the current mirror circuit formed by an N-channel MOSFETs, M3 and M4. The transistor M7 serves as an P-channel common source amplifier which is the second stage of op-amp. The current Ibias of the op-amp circuit goes through current mirrors formed by P-channel MOSFETS, M8, M5 and M6. It is designed to produce a current of 350 μA.

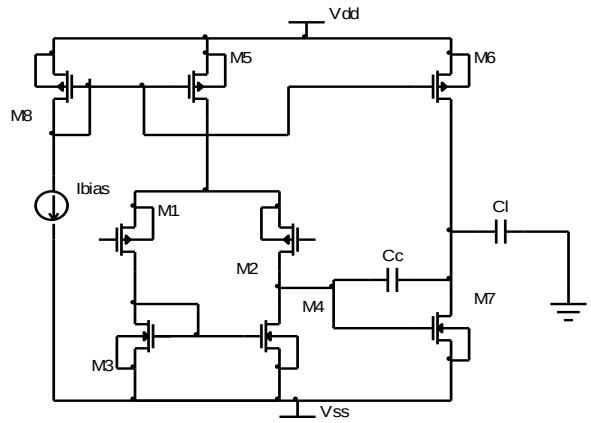

Fig. 5: Two-Stage Miller OTA [12]

2.2 Theoretical study

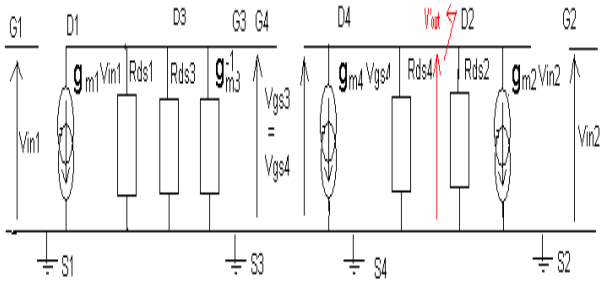

Fig.6 : Small signal equivalent circuit for two-stage op-amp

As shown in fig. 6, we present the small equivalent circuit in order to focus on the input differential stage.
We obtain a differential gain (A_{v1}) of stage 1:

$$A_{v1} = \frac{V'_{out}}{2\,V_{in}} = -\frac{g_{m2}}{g_{ds\,2} + g_{ds4}} = -\frac{\sqrt{Kp.\frac{W_1}{L_1}.I_5}}{\frac{I_5}{2}\left(\frac{1}{V_{Ep}.L_2} + \frac{1}{V_{En}.L_4}\right)}$$

Gain of stage 2 is:

$$A_{v2} = -\frac{g_{m7}}{g_{ds\,7} + g_{ds6}} = -\frac{\sqrt{2.Kn.\frac{W_7}{L_7}.I_6}}{\frac{I_6}{2}\left(\frac{1}{V_{Ep}.L_6} + \frac{1}{V_{En}.L_7}\right)}$$

The overall gain of the amplifier is $A_v = A_{v1}.A_{v2}$
The gain bandwidth is:

$$GBW = \frac{g_{m_1}}{2.\pi.C_c}$$

Where g_{m1} is the transconductance of M1,
g_{ds} = parameter transconductance drain to source
According to [13] we use the following formula:

$$\frac{1}{A_v} \le \frac{1}{2} \times q \iff \begin{cases} A_v \ge 682.66 \\ A_v \ge 56.6\ \text{dB} \end{cases}$$

Where q is the quantum of the Sigma-Delta ADC which is expressed as:

$$q = \frac{V_{Full\ scale}}{2^N} = \frac{[1.5-(-1.5)]}{2^{10}} = 0.0029$$

In this case we assume the overall gain A_v more than 57 dB and to ensure good stability op-amp phase margin should be also more than 60 degree.
In [15], It is mentioned that GBW ≥ 3 Fs, but in this work it is recommended to have GBW more than 50 MHz in order to apply the following formula [14]:

$$GBW \ge A_v \times f_b$$

Where:

$$A_v \times f_b = 682.66 \times 80KHz = 54.6MHz$$

$$\Longrightarrow\ GBW \ge 54.6\ MHz$$

f_b is the base band frequency and A_v is the overall gain.
All of op-amp has a restriction on its operating voltage range, CMR limits (Common input Mode Range) is the border of the scale range of each input op-amp, outside these limits cause output distortion. CMR can be presented by:

$$CMR_+ = V_{DD} + V_{TP} - \sqrt{\frac{2.I_5}{Kp.W_5/L_5}} - \sqrt{\frac{I_5}{Kp.W_1/L_1}}$$

$$CMR_- = V_{SS} + V_{TP} - V_{Tn} + \sqrt{\frac{I_5}{Kn.W_3/L_3}}$$

In fig. 4, two-stage op-amp transconductance can be analyzed as follows:

$$OUT_+ = V_{DD} - \sqrt{\frac{2.I_6}{Kp.W_6/L_6}}$$

$$OUT_- = V_{SS} + \sqrt{\frac{2.I_6}{Kn.W_7/L_7}}$$

$$ID_1 = ID_2 = \frac{I_{ss}}{2}\ ;\ slew\ rate\ (SR) = \frac{I_5}{C_c}$$

Where $I_{ss} = I_5$, $ID_3 = ID_4$

According to [15], we can propose a simple method based on g_m/ID to determine (W/L) for each transistor of amp-op, because most methods for analytical synthesis of analog circuits suppose that the MOS transistors are either in strong inversion or in weak inversion. Our proposed methodology allows a unified synthesis methodology in all regions of MOS transistor.
The design procedure is illustrated as follows:
First of all, it is necessary to choose the value of the compensation capacitor C_c. For 60° phase margin, we use the following relationship:

$$C_c > 0.22 \times C_L \Longrightarrow C_c = 1 \text{ pF}$$

Then the value of the bias current (I_{bias}) is determined based on the slew rate requirements: I_{bias}= 330µA. From Vgd3 = 0, transistor M3 is in saturation. Since the systematic offset condition provides that the drain voltage of M4 is equal to the drain voltage of M3.
The systematic offset condition makes the drain voltage of M1 equal to the drain voltage of M2. Consequently the condition for M2 being saturated is the same as the condition for M1 being saturated. We have Vgd8 = 0 thus transistor M8 is always in saturation. Transistors M5 and M6 form a current mirror with transistor M8.
In this case, we consider that the transistors have the same length (L= 1µm) to conserve symmetry and matching for all transistors, we require that:

W1=W2, W3=W4, W5=W8

Thus I_1, I_5 and I_7 can be expressed as follows:

$$I_5 = \left(\frac{W_5/L_5}{W_8/L_8}\right).I_{bias} \quad ; \quad I_7 = \left(\frac{W_6/L_6}{W_8/L_8}\right).I_{bias}$$

$$I_1 = \frac{I_5}{2} = \frac{1}{2}\left(\frac{W_5/L_5}{W_8/L_8}\right) \times I_{bias}$$

2.3 Technological specification

In order to realize a low power and low noise op-amp transconductance amplifier this is the most significant building-blocks in integrated discrete-time filters use for Sigma-delta analog to digital converter (Wireless Sensor Receiver). We must respond to technological specifications and requirements listed in Table 2.

Table 2 : Op Amp specifications

Specifications	Definition	Value
Technology	Austriamicrosystems (AMS)	0.35 µm
Av (dB)	Differential gain	≥ 56.6
GBW (MHZ)	Gain bandwidth product	≥ 54.6
PM (degree)	Phase margin	≥ 60
f_b (KHz)	Cut-off frequency	≥80
SR (V/µs)	Slew rate	≥ 0.1
P_{moy} (mW)	Average power consumed	< 3 mW
V_{dd} (V)	Positive power source	+1.5
V_{ss} (V)	Negative power source	-1.5
C_L (pF)	Output load capacitance	3
C_C (pF)	Compensation capacitance	1
V_{out} (V)	Output-voltage swing	-1.2V to 1.2V

2.4 Op-Amp simulation

Referring to fig. 5 and respecting the specifications and the requirements shown in table 2, the size of different devices are calculated. Table 3 presents the parameters values of op-amp miller OTA. By using Pspice, we proceed to simulate the circuit given by fig. 5. We determine various characteristics such as gain, phase margin, power consumption, noise, slew rate, and offset.

Table 3 :Op Amp parameters values

Devices	Value	
M1, M2	W=24µm	L=1µm
M3, M4	W=10µm	L=1µm
M5, M8	W=41µm	L=1µm
M6	W=220µm	L=1µm
M7	W=148µm	L=1µm
Supply voltage	V_{dd}=1,5V	V_{ss}= -1,5V
Load capacitance	C_1 = 3pF	
Compensation capacitance	C_c = 1 pF	
Bias current	350µA	

2.4.1 Frequency open loop analysis

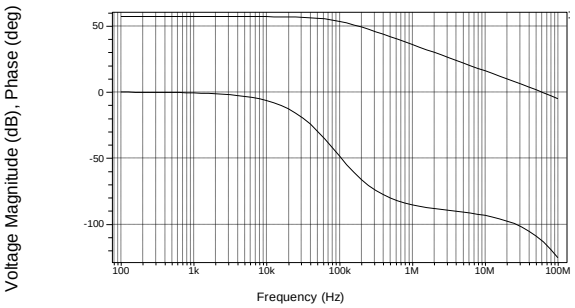

Fig. 7 : Simulated transfer function of amplifier Magnitude (dB) and phase (degree) of the Basic Two-Stage Miller OTA

The simulated output frequency response is shown in fig. 7. The bode diagram gives a high open loop gain of 57 dB with a large GBW of 59 MHz, a 90 KHz of cut-off frequency and a phase margin of 68°.

2.4.2 Unity feedback analysis

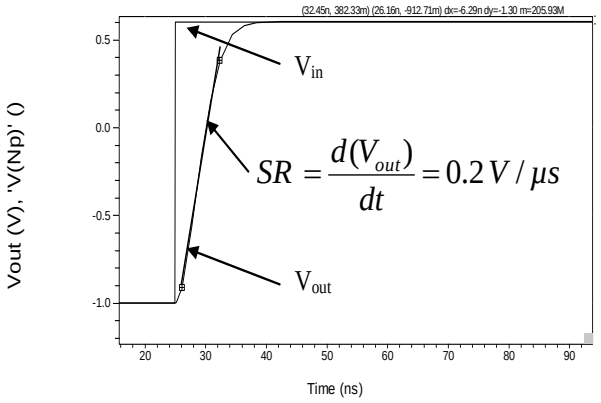

Fig. 8 : Step transient response showing the slew

-As shown in fig. 8, a step is applied from -1V to 0.6 V at the input with unity feedback configuration. As was measured, the amplifier's slew rate is 0.2 V/µs for the rising edge.

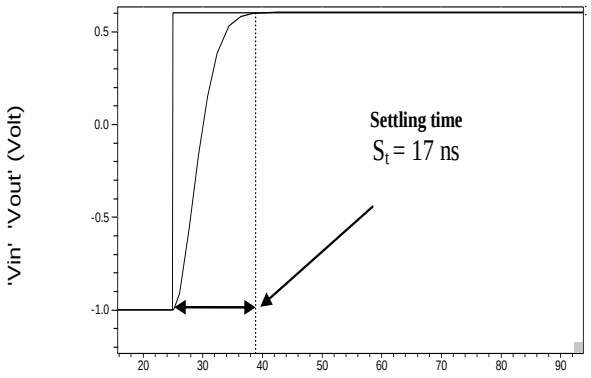

Fig. 9 : Step transient response showing the settling time of the Two-Stage Miller OTA

-The unity gain configuration is also used for settling time and peak over shoot measurement. This is the length of time for the output voltage of an op amp to approach. It remains within, a certain tolerance of its final value. The settling time equal to 17 ns is presented in fig. 9.
The output swing measured peak to peak shown in Fig. 10 is found to be -1.375 V to 1.375 V.

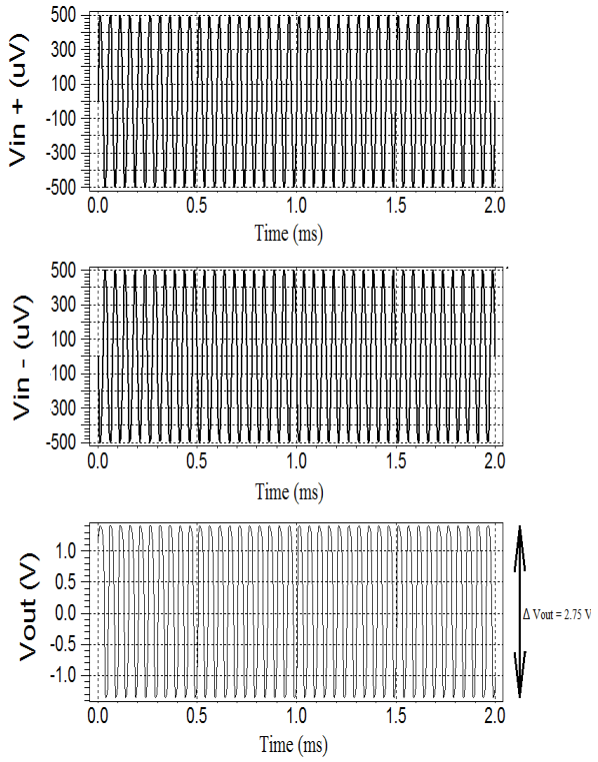

Fig. 10 : Transient Response showing the swing of 2.75 V of the OTA

2.4.3 DC sweep analysis

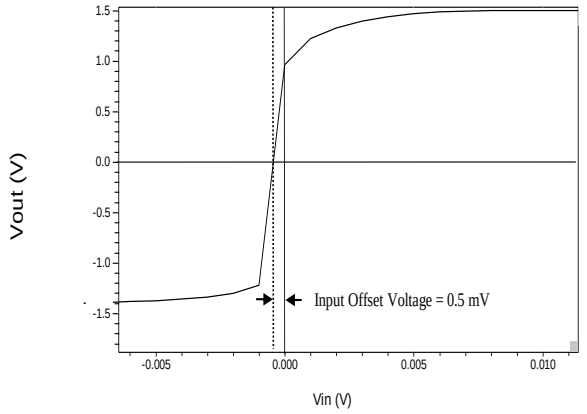

Fig. 11 : Transfer characteristics showing the input offset voltage of the of the Two-Stage Miller OTA

Fig. 11, shows the transfer characteristics obtained from DC sweep analysis. The input offset voltage is approximately calculated as 0.5 mV.

2.4.4 Summary table

Table 4 summarizes the simulation results of the of the two-Stage Miller OTA

Table 4 : Summarizes the simulation results of the of the Basic Two-Stage Miller OTA

Parameters	Value
Slew rate (SR)	0.2 V/µs
DC Offset	0.5 mV
Gain	57 dB
Gain bandwidth (GBW)	59 MHz
Cut-off frequency (f_b)	90 KHz
Phase margin (PM)	68 °
Average power consumed	3.5 mW
Output-voltage swing	-1.3 to 1.1
Supply voltage	±1.5V
Settling time (S_t)	16 ns

3. MODIFIED TWO-STAGE MILLER OTA CIRCUIT WITH CASCODE CURRENT SOURCE

3.1 Analyses and specifications

In this paper, we proposed a modified OTA in which bias circuit was actively designed by NMOS transistors. For completeness, we first, analyzed and implement a Basic two-stage Miller OTA to prove the efficiency of the proposed design OTA.

In Fig. 12, the bias circuit consisted of NMOS cascode current source which is formed of five transistors (M9, M10, M11, M12, M13).

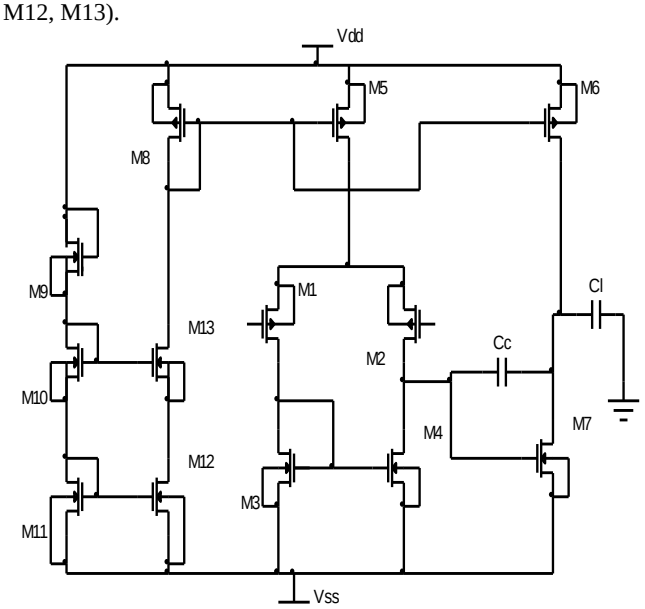

Fig. 12 : Modified Two-Stage Miller OTA with cascode current mirror

On the one hand, current source is one of the basic building blocks of analog VLSI systems. For low voltage design circuit, current source has to be with low input and output voltages. The accuracy and output impedance are the most important parameter to determine the performance of the current source. The basic simple current source with NMOS transistors (M, M') is shown in fig. 13.

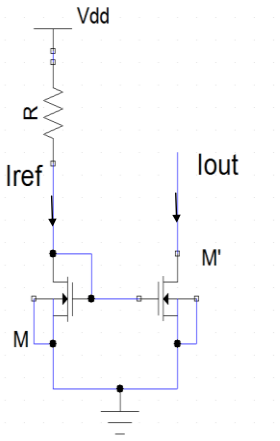

Fig. 13 : Simple Current Source

On the other hand, the basic current source needs to be stabilized over a large output voltage range, a high output impedance current source might needed. This is accomplished by putting two current sources in "cascade" to each other.

The most popular current source circuit known as the cascode current source is shown in Fig. 14. Here, cascode current mirror can be used for the duplication of current I_{ref} to provide higher output resistance and lower symmetric error. The NMOS cascode mirror consists of four transistors (M10, M11, M12, M13). It has high output impedance, and provides a low systematic transfer error.

It is well known that CMOS active resistors are very important blocks in VLSI analog designs, mainly used to replace the large value passive resistors, with the great advantage of a much smaller area occupied on silicon. As shown in fig. 13, the gate and drain terminals are connected together on a transistor M9 in order to replace an active resistor R.

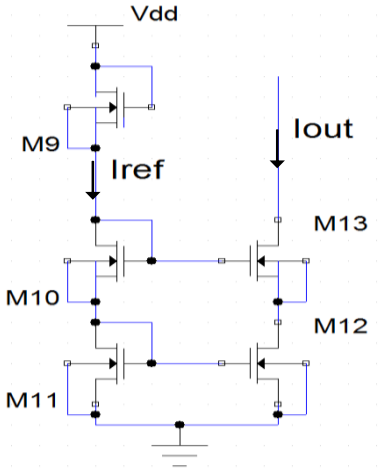

Fig. 14 : Cascode Current Source

Cascode current source has higher output resistance [16] than the simple current mirror. The expression of input and output impedance (R_{in}, R_{out}) can be analyzed as follows:

$$R_{in} = \frac{1}{gm_{10}} + \frac{1}{gm_{11}}$$

$$R_{out} = \frac{gm_{13}}{go_{13}.go_{14}}$$

Where gm is a transconductance and go is the output conductance of M13, M14.
In fact, Cascode current source is used in many designs, including [17]–[18], to increase the current source output resistance by a large factor.
Each cascode stage increases the output resistance by a factor of $(1+gm.r_{out})$ where r_{out} is the output resistance. Increased output resistance, however, is achieved at the expense of reduced voltage. It also increases the power dissipation in saturated transistors. For this reason we use a simple cascode current source to assist the system designer in achieving low power consumption. Then the use of cascode current source provides high output impedance, which is also one of the major issues in microelectronic, to replace a current source of 350 µA in order to design low power operational transconductance amplifier circuit used for wireless sensor receiver. Using the Pspice simulation, Table 5 presents the parameters values of op-amp modified Miller OTA.

Table 5 : Op Amp parameters values of the modified Two-Stage Miller OTA with cascode current source

Devices	Value	
M1, M2	W=32µm	L=1µm
M3, M4	W=14µm	L=1µm
M5, M8	W=41µm	L=1µm
M6	W=220µm	L=1µm
M7	W=148µm	L=1µm
M9, M10, M11, M12, M13	W=14µm	L=1µm
Supply voltage	V_{dd}=1.5V	V_{ss}= -1.5V
Load capacitance	C_1 = 3pF	
Compensation capacitance	C_c = 1 pF	

3.1.1 Simulations results

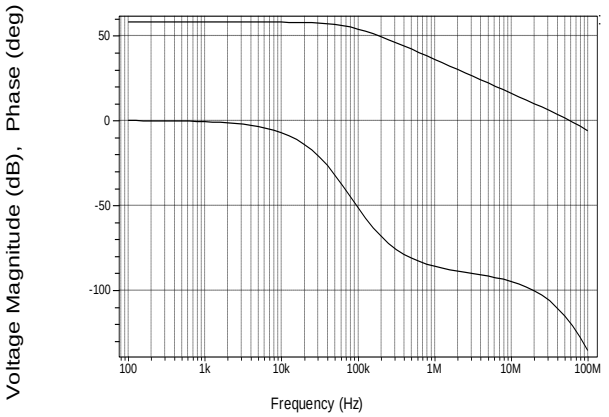

Fig. 14 : Simulated transfer function of amplifier Magnitude (dB) and phase (degree) of the modified Two-Stage Miller OTA with cacode current source

As shown in fig. 14, we present the simulated output frequency response. Where the bode diagram gives a phase margin 62°, a high open loop gain of 57 dB with a large GBW of 58 MHz and a cut-off frequency f_b of 82 KHz.

3.1.2 Summary table

Table 6 summarizes the simulation results of the modified tow stage Miller OTA circuit with cascode current source.

Table 6: Summarizes the simulation results of the modified Two-Stage Miller OTA with cascode current source

Parameters	Value
Slew rate (SR)	0.13 V/µs
DC Offset	0.5 mV
Gain	57 dB
Gain bandwidth (GBW)	58 MHz
Cut-off frequency (f_b)	82 KHz
Phase margin (PM)	62 °
Average power consumed	2.27 mW
Output-voltage swing	-1.4 to 1.2
Supply voltage	±1.5V
Settling time (S_t)	17 ns

4. MODIFIED TOW-STAGE MILLER OTA WITH DESIGNED CURRENT SOURCE

4.1 Description

fig. 15, in which bias circuit was actively presented by designed current source. This last is consisted of four PMOS transistors (M9A, M10A, M11A, M12A) which formed cascode mirror with weak supply voltage [20].
In this case cascode current mirror can be used for the duplication of current to provide higher output resistance and lower symmetric error. Then the input NMOS transistor (M14A) is based on input voltage (V_{in}) which is 0 V to obtain low power voltage consumption. On the other hand, after the current goes through PMOS cascode current mirrors, the output obtained is a current value (I_{out}) by the transistor (M13A), as shown in fig. 16.

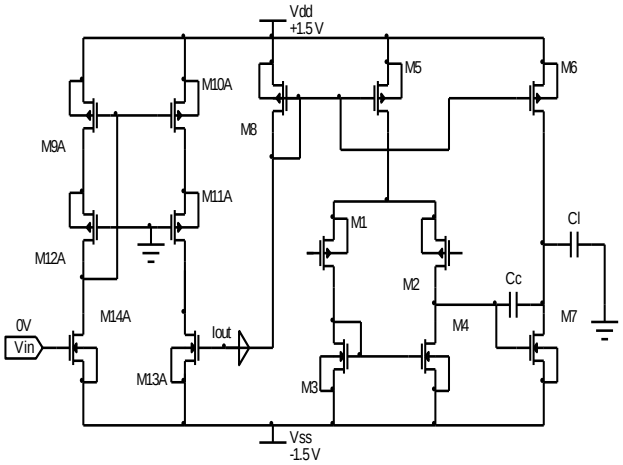

Fig. 15 : Modified Two-Stage Miller OTA with designed current source

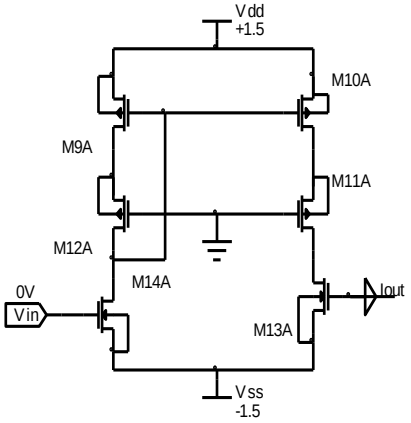

Fig. 16 : Proposed current source

Table 7 presents the parameters values of op-amp Miller OTA with designed current source.

Table 7: Summarizes the simulation results of the Two-Stage Miller OTA with designed current source

Devices	Value	
M1, M2	W=44µm	L=1µm
M3, M4	W=13µm	L=1µm
M5, M8	W=41µm	L=1µm
M6	W=220µm	L=1µm
M7	W=128µm	L=1µm
M9A, M10A	W=4µm	L=0.35µm
M11A, M12A, M13A, M14A	W=1µm	L=0.35µm
Supply voltage	V_{dd}=1.5V	V_{ss}= -1.5V
Load capacitance	C_l = 3pF	
Compensation capacitance	C_c = 1.1 pF	

4.1.1 Simulations results

The DC analysis of our designed current source is presented in fig. 17, in which the value of current is equal to 28 µA for different values of voltage. In this can we choose input voltage as 0 V to obtain low power consumption.

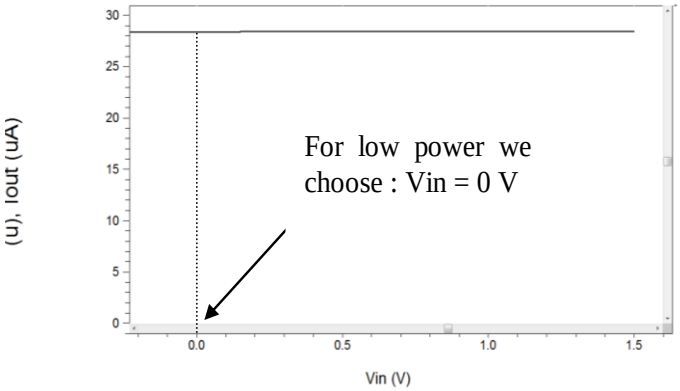

Fig. 17 : DC analysis showing Iout VS input voltage V_{in} of the designed current source

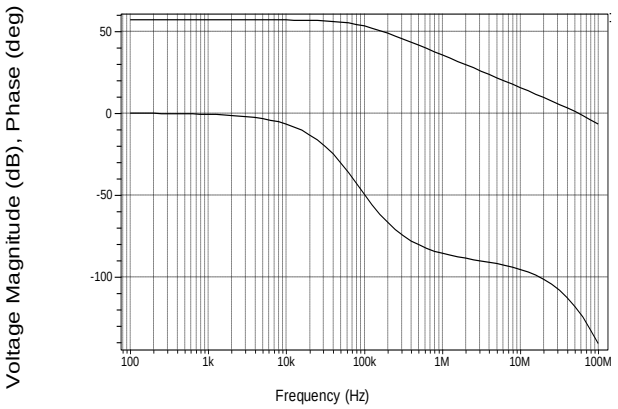

Fig. 18 : Simulated transfer function of amplifier Magnitude (dB) and phase (degree) with the designed current source

As shown in fig. 18, we present the simulated output frequency response. Where the bode diagram gives a phase margin 60°, and a high open loop gain of 57 dB with a large GBW of 55 MHz .

4.1.2 Summary table

Table 8 summarizes the simulation results of the of the Basic Two-Stage Miller OTA

Table 8: Summarizes the simulation results of the of the Basic Two-Stage Miller OTA with designed current source

Parameters	Value
Slew rate (SR)	0.1 V/µs
DC Offset	0.5 mV
Gain	57 dB
Gain bandwidth (GBW)	55 MHz
Cut-off frequency (f_b)	85 KHz
Phase margin (PM)	60 °
Average power consumed	1.66 mW
Output-voltage swing	-1.3 to 1,3
Supply voltage	±1.5V
Settling time (S_t)	15.6 ns

5. COMPARATIVE ANALYSIS

Table 9 gives a characteristic comparison between our proposed method and others conventional two-stage OTA. Using 0.35µm technology, the modified two-stage OTA with designed current source consumes less power than other types and gives a 50% consumption gain. But at the same time it has a large bandwidth of 55 MHz, a Av gain of 57 dB and a Cut-off frequency of 85 KHz, which are necessary for our application.

Table 9: Comparison between differents types of Two-stage OTA with technology 0.35µm

Parameters	Two-stage Miller OTA [19]	Modified Two-stage OTA with cascode current source (Fig. 12)	Two-stage Miller OTA (Fig. 5)	Modified Two-stage OTA with designed current source (Fig. 15)
Technology	TSMC 0.35µm	AMS 0.35µm	AMS 0.35µm	AMS 0.35µm
A_v gain	48 dB	57 dB	57 dB	57 dB
Average Power consumed	3.4 mW	2.2 mW	3.5 mW	**1.66 mW**
Phase margin	61°	62°	68°	60°
Slew rate	26 (V/µs)	0.13 (V/µs)	0.2 (V/µs)	0.1 (V/µs)
GBW	10 MHz	58 MHz	59 MHz	55 MHz
Cut-off frequency	167 Khz	82 KHz	90 KHz	85 KHz
Supply voltage	3.3 V	±1.5 V	±1.5 V	±1.5 V
Application	Sigma-Delta modulator of Digital-Audio	Sigma-Delta Converter of wireless sensor receiver	Sigma-Delta Converter of wireless sensor receiver	Sigma-Delta Converter of wireless sensor receiver

6. CONCLUSION

Design of OTA is vital importance in integrated discret-time filters used for design Sigma-Delta converter.

This work presents a novel design method of two-stage CMOS OTA which has been designed and compared with a basic two-stage CMOS OTA. Behavioural simulation indicated that phase margin is 60° to ensure a good stability, gain of 57 dB for ±1.5V without using a gain boosting technique, and GBW of 55 MHz is sufficient to design the ADC converter. The applied technique leads to a significant preservation in gain bandwidth product (GBW), gain (Av), slew rate (SR), and decrease power consumption. The design technique proposed in this paper combines better performance with simplicity of design and suitability for high frequency operation with few modifications on conventional two-stage CMOS OTA and at low power consumption.

These parameters are very important for high frequency, fast settling applications especially in integrated discrete-time filters used for design Sigma-Delta ADC converter.

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