Efficient Switching Activity Reduction Technique for Fault Tolerant Data Bus

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ABSTRACT
In Deep-submicron (DSM) systems, the crosstalk effect on on-chip data buses and interconnects dictates the overall performance and reliability of the highly integrated systems. In many digital processors and SoC the reliable transfer of the information over the data bus is crucial for the proper operation of a particular system. Hence ECC techniques are used on data buses for reliable transfer of the information. Employing the ECC on data buses eventually increases the switching activity that affects the power consumption and delay of the system. Reducing the power dissipation of the VLSI chip is one of the major challenges in the DSM technology. One of the best techniques to reduce the transitions is to use encode and decoder along with the ECC on the data bus. Hence an efficient switching activity reduction technique is proposed for fault tolerant data bus which can reduce the overall transitions. The proposed encoding technique reduces the switching activity by 18% to 22.5%. Its efficiency is 8% to 15% more compare to others encoding techniques.

General Terms
VLSI, Data bus, Reliable, transitions.

Keywords
Crosstalk, ECC, DSM, Interconnects, fault tolerant data bus, power dissipation.

1. INTRODUCTION
As the transistors are taking the nanometer and sub-nanometer dimensions through CMOS integration technology, it poses many challenges to design and test engineers. The scaling of VLSI integrated circuits has increased the sensitivity of CMOS based systems to cause large power dissipation, propagation delays and various noise mechanisms such as power supply noise, crosstalk noise, leakage noise, etc. The power consumption and crosstalk has become a major concern because of continuing decrease in the minimum feature size and the corresponding increase in chip density and operating frequencies [1]. Unfortunately in nanometer and sub nanometer technologies the coupling effect influences the performance of the data buses. The characteristics of data buses and long interconnects such as wire spacing [2], wire length, wire material, wire width, driver strength, coupling length and signal transition time, etc. influences the coupling effect. This increased coupling effect on on-chip buses and on long interconnects not only increase the power dissipation but also deteriorate the signal integrity due to the coupling capacitance. As a results these busses and interconnects becoming more sensitive and prone to errors caused by crosstalk noise and delay faults [3], [4], [5]. To increase the performance and reliability of the systems the data bus has to be fault tolerant. This can be achieved by employing the hamming encoder and decoder on the data buses [3]. Since the power consumption of the fault tolerant bus increase due to hardware overhead of ECC and increased switching activity overall power consumption of the system also increases. Hence it is necessary to reduce the switching activity to decrease the power dissipation on the fault tolerant buses.

Reducing the transition activity or switching activity on the on-chip data buses is the one of the attractive way of reducing power dissipation on fault tolerant data bus. Switching activity on the data bus can be reduced by employing bus encoding techniques. Several bus encoding techniques have been proposed to reduce power consumption during bus transmission in literature. These techniques mainly relay on reducing the data bus activity by reducing the self transitions or reducing the coupling transitions. Reducing power dissipating transition by encoding the data on the data buses leads to reducing the bus activity hence overall power consumption is reduced.

Over the past few years, a number of coding techniques have been proposed for reducing the transitions on a data bus. For data buses, one popular coding scheme is the bus invert coding technique proposed by Stan and Burleson [6]. In this method it compares the successive data bus values and determining if inverting a data on data bus word would results in fewer bit transitions than not inverting the word. This technique is suitable for uncorrelated data patterns and is based on the Hamming distance. It calculates the number of bits that change state from one data word to next data word. If the number of bit transitions is greater than the half of the total number of bus lines, then the inverted data is transmitted over the bus, other wise original data is sent. This method effectively reduces the maximum number of transitions to one half of the number of data bits. Other variants of the bus invert coding schemes include a decomposition approach [7] and partial bus coding technique [8].Both these techniques have an area overhead to determine the suitable partition of the data bus. In addition, the decomposition approach [7] can require up to p-1 extra lines on the bus where p is the number of partitions of the original data bus. The energy dissipated due to coupling capacitance is analyzed in [9], [10]. For instruction buses Gray code [11], T0 code [12], the Beach code [13] have been proposed which reduces the transitions there by reducing the power dissipation. Dynamic coding method takes even and odd line as bus sub-group and finds the coupling transitions and then invert the sub-bus group which decreases the coupling transitions [14].Shift

invert coding shift the data right by one position, left by one position and invert the total data. It calculates the coupling transition for all four combinations and selects the least one and sends it by appending two bit combination [15]. In Novel Coding Technique the data bus is sub divided into even and odd bit groups. Hamming distance between even sub group, odd sub group, inverted data and present data is compared with the data on the bus respectively. The sub-group whose hamming distance is lesser that subgroup's data is inverted and transmitted with two redundant control bits for decodes purpose. One of the disadvantage of this technique is coupling transitions occurs due to redundant bits also [16]. In almost all above mentions methods only coupling transitions are considered and self transitions either neglected or can not be reduced. All these methods are use on data bus but not on fault tolerant data bus The proposed method Bus regrouping with Hamming distance considers the reduction of both coupling as well as self transition which results to a more save in power dissipation not only on data bus [17]but also on fault tolerant data buses.

2. SELF AND COUPLING TRANSITIONS

Self transition on the data bus is defined as transition on the capacitance between a data bus line and the substrate. Coupling transition on data bus is defined as transition on capacitance between adjacent bus lines [10]. Dynamic power consumption of data bus in CMOS technology in DSM technology is give by $P = (\alpha_l\ C_l + \alpha_c\ C_{c)}\ V^2_{dd}\ f$, where α_l is average self transition on the data bus, α_c is average coupling transition on the data bus, C_l is load capacitance, C_c is coupling capacitance, V_{dd} is operating voltage and f is operating frequency. In most cases, designers have no influence on C_l, C_c, V_{dd} and f. In general α ($=\alpha_l + \alpha_c$) is termed as Switching activity (α). Switching activity is the better parameter that can be controlled and optimized at high level design. By reducing the switching activity (i.e. α_l and $\alpha_{c)}$ overall power consumption can be reduced. A self transition is said to occur whenever a data bus wire makes a transition from 0 to 1 or from 1 to 0. When this occur the substrate capacitance either charges from GND to V_{dd} or discharge from V_{dd} to GND respectively. The coupling transition activity depends on the switching activity between two adjacent data bus bit lines which can be explained as follows. If the signals on data bus paths changes as (00→11 or 11→00) switching occurs in both of the adjacent wires but to the same resulting state. If the signals on data bus paths changes as (10→00 or 01→00 or 01→11 or 01→11) switching occurs in one of the adjacent wires but to the same resulting state. If (00→00 or 11→11) no switching activity occurs. In all above cases the power consuming transitions are zero and the dynamic power consumption is not effected by C_c. The transitions (00→01or 00→10 or 11→10 or 11→01 etc.) occurs when single line switching occurs and the resulting state is different from the other. In this case only one power consuming transition occurs and the dynamic power consumption is affected by C_c. The transitions (10→01 or 01→10) occur when both the adjacent wires change their states to opposite logic levels. In this case two power consuming transitions occur and the dynamic power consumption is effected by C_c [18].

3. FAULT TOLERANT DATA BUS

Fault tolerant of a data bus is usually implemented by incorporating redundant information using error detecting and correcting codes such as Hamming codes, dual rail codes etc.[3]. In Hamming code N- information bits are applied to the encoder which produces K-check bits. Code word is generated which consist of M-bits equals to N+K bits. This codeword is transmitted over the data bus to the receiver. At the receiver end of the bus the decoder detects and corrects the possible errors which might have occurred on the data bus when these are being transmitted. From the simulation results it is observed that the total transitions on the fault tolerant data bus are increased than with out error detecting and correcting codes. As a consequence the power dissipation on fault tolerant data bus increases which poses a serious problem in DSM technology. Hence this increased power dissipation can be decreased by employing the bus encoding techniques.

4. EFFICIENT SWITCHNING ACTIVITY REDUCTION SCHEME

The proposed encoding technique for fault tolerant data bus is based on the number of coupling transitions occurring on the fault tolerant data bus when a new data is to be transmitted. For a signal transmission through a two-wire bus, all coupling transitions between possible bit patterns are shown in Table 1. In the following analysis assume n=38-bit data words. By using the following algorithm coupling transitions and self transitions can be reduced. The proposed algorithm for 38-bit fault tolerant Data bus is given as follows:

Let 38-bit fault tolerant data bus be represented by

$a_0\ a_1\ a_2\ a_3\ a_4\ a_5\ a_6\ a_7\ a_8\ a_9\ a_{10}\ a_{11}\ a_{12}\ a_{13}\ a_{14}\ a_{15}\ a_{16}\ a_{17}\ a_{18}\ a_{19}\ a_{20}\ a_{21}\ a_{22}\ a_{23}\ a_{24}\ a_{25}\ a_{26}\ a_{27}\ a_{28}\ a_{29}\ a_{30}\ a_{31}\ a_{32}\ a_{33}\ a_{34}\ a_{35}\ a_{36}\ a_{37}$

1. Calculate the number of power consuming CT (coupling transitions) of the present data on fault tolerant data bus with previous data.

Table 1. Coupling transitions

Bit Pattern	00	01	10	11
00	0	1	1	0
01	0	0	2	0
10	0	2	0	0
11	0	1	1	0

2. Calculate the number of power consuming ST (Self transitions) of the present data on fault tolerant data bus with previous data.

3. If CT >= (n/2) then

3.1 Consider the grouping of the present bus data. Arrange the data on the data bus as

Odd Group: $a_0a_2a_4a_6a_8a_{10}a_{12}a_{14}\ a_{16}a_{18}a_{20}a_{22}a_{24}a_{26}a_{28}a_{30}a_{32}a_{34}a_{36}$

Even Group: $a_1a_3a_5a_7a_9a_{11}a_{13}a_{15}a_{17}a_{19}a_{21}a_{23}a_{25}a_{27}a_{29}a_{31}a_{33}a_{35}a_{37}$

Note: here odd group means, data in odd bit positions, even group means data in even bit positions.

3.2(a): The Hamming Distance between odd group of present data and odd group of previous data is calculated. This is represented as OHD = Odd bits Hamming Distance.

3.2(b): The Hamming Distance between even group of present data and even group of previous data is calculated. This is represented as EHD = Even bits Hamming Distance

3.3: Transmit the data by following the below conditions:

If OHD > EHD, flip the data in odd bit positions and append bit '1' on the left and bit '0' on the right side of the encoded data.

If EHD > OHD, flip the data in even bit positions and append bit '0' on the left and bit '1' on the right side of the encoded data.

If OHD = EHD, flip the entire data and append bit '1' on the left and bit '1' on the right side of the encoded data.

Step 4: If CT<n/2 is true then transmits the data as it is, append bit '0' on the left and bit '0' on the right side of the encoded data.

Step 5: Calculate the self transitions of transmitted encoded data with present transmitting encoded data.

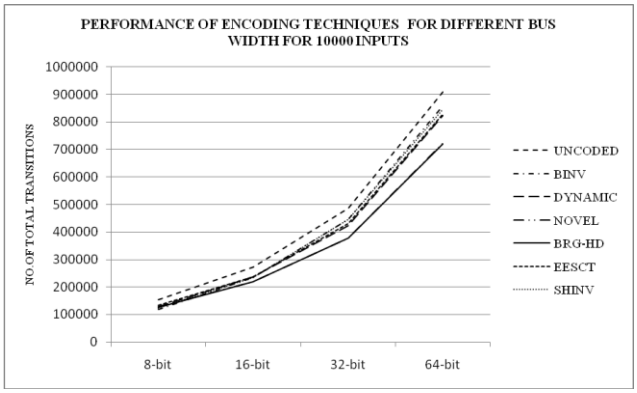

Fig 1: Comparison of Total Transitions of different encoding techniques with change of bus width.

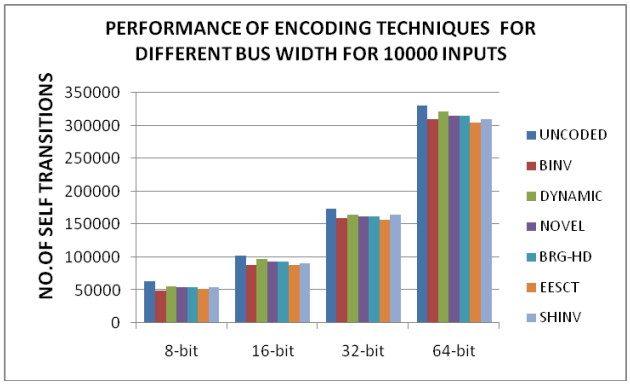

Fig. 2: Comparison of Self Transitions of different encoding techniques with change of bus width.

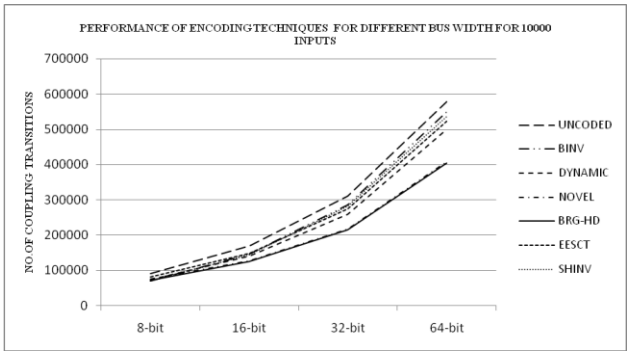

Fig 3: Comparison of Coupling Transitions of different encoding techniques with change of bus width.

5. PERFORMANCE OF THE PROPOSED TECHNIQUE

The effectiveness of proposed technique is evaluated by using a VHDL code. The simulations is performed on 12-bit,21-bit,38-bit and 71-bit data buses with three groups of 1000,2000, 5000 and 10000 data vectors. Self transitions and Coupling transitions are considered as metric parameters. Power consuming self and coupling transitions are separately calculated for each method. The methods that are considered are Bus invert (Binv), dynamic [14], Novel [16], Shift Invert (SHINV)[15], Energy Efficient spatial coding (EESCT)[19] and Bus regrouping with hamming distance (BRG-HD).The performance of the techniques is evaluated by varying bus width and number inputs. Fig-1, Fig-2 and Fig-3 shows the performance variation of the different encoding techniques with respect to coupling transitions, self transitions and total transitions respectively. Bus invert [6] method is the best method to reduce the self transitions for all four bus widths. This technique is best suitable for 12-bit data bus for reducing overall transitions. The proposed method is an efficient method to reduce the switching activity except for 12-bit data bus only. For 21-bit, 38-bit and 71-bit the proposed method is an efficient method to reduce coupling and overall transitions.

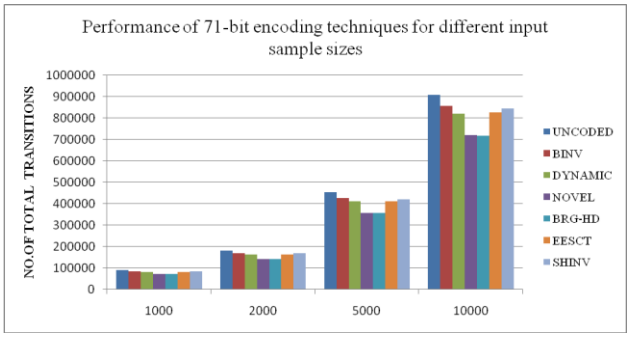

Fig. 4: Comparison of 71-Bit encoding technique with respect to Total Transitions

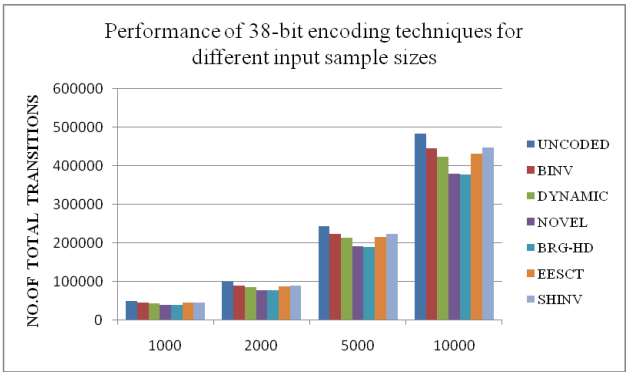

Fig. 5: Comparison of 38-Bit encoding technique with respect to Total Transitions

The reduction in the number of coupling transitions achieved is high compare to all other techniques except for 12-bit bus. Fig-4, Fig-5 and Fig-6 shows that the proposed method is an efficient encoding technique to reduce the overall transitions for 71-bit, 38-bit and 21-bit fault tolerant data bus respectively. The proposed technique fails for 12-bit data bus as shown in Fig-7. Simulation results from the table 2, 3, 4 and 5 shows that about 18% to 22.5% reduction in switching activity is achieved by the proposed technique. In tables TT stands for Total transitions. Comparing with Bus invert, Dynamic, Shift invert, EESCT and Novel coding techniques proposed technique is 8% to 15% is more efficient. Since switching activity is reduced, the power dissipation on the data bus can also be reduced.

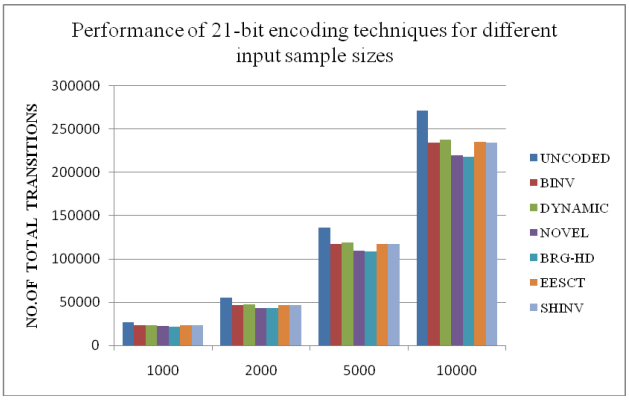

Fig. 6: Comparison of 21-Bit encoding technique with respect to Total Transitions

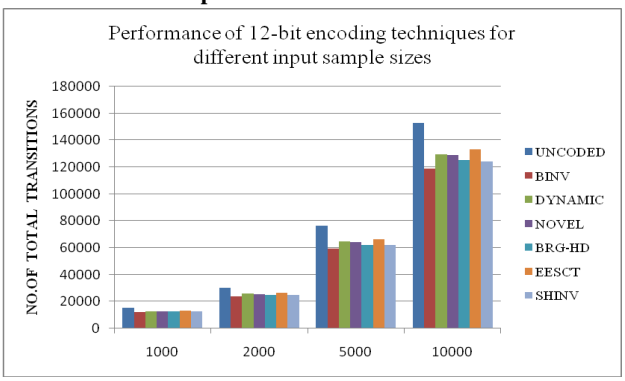

Fig. 7: Comparison of 12-Bit encoding technique with respect to Total Transitions

Table 2. Efficiency of Encoding Techniques for 71-bit Fault tolerant data-bus

Method	Uncoded TT	Coded TT	Efficiency in %
BINV	455709	427490	6.192328877
DYNAMIC	455709	411030	9.804282996
NOVEL	455709	358952	21.23218984
BRG-HD	455709	357124	21.63332302
EESCT	455709	411732	9.650237323
SHINV	455709	421547	7.496450586

The efficiency of different coding method is calculated by using the following formula:

Efficiency= (Unencoded data – Coded Data) / Unencoded data x100

Here efficiency indicates how many coupling transitions are reduced after encoding with respect to the normal data

Table 3. Efficiency of Encoding Techniques for 38-bit Fault tolerant data-bus

Method	Uncoded TT	Coded TT	Efficiency in %
BINV	243682	222867	8.541870142
DYNAMIC	243682	212747	12.69482358
NOVEL	243682	190203	21.946225
BRG-HD	243682	188742	22.54577687
EESCT	243682	214532	11.96231154
SHINV	243682	223103	8.445022611

Table 4. Efficiency of Encoding Techniques for 21-bit Fault tolerant data-bus

Method	Uncoded TT	Coded TT	Efficiency in %
BINV	136531	116845	14.41870344
DYNAMIC	136531	119211	12.68576367
NOVEL	136531	109064	20.11777545
BRG-HD	136531	108434	20.57920912
EESCT	136531	117370	14.03417539
SHINV	136531	117043	14.27368143

Table 5. Efficiency of Encoding Techniques for12-bit Fault tolerant data-bus

Method	Uncoded TT	Coded TT	Efficiency in %
BINV	76212	59372	22.09625781
DYNAMIC	76212	64630	15.19708182
NOVEL	76212	64350	15.56447803
BRG-HD	76212	62381	18.14806067
EESCT	76212	66408	12.86411589
SHINV	76212	62027	18.61255445

6. CONCLUSIONS

The proposed efficient switching activity reduction technique for fault tolerant data bus encoding scheme reduces the coupling transition as well as the self transitions on fault tolerant data bus transmission in deep sub-micron buses. The main aim of the proposed technique is to reduce the switching activity which can save the energy dissipated due to the transitions on data buses. Fault tolerant data buses buses have extra hardware overhead due to ECC. Hence the proposed technique can able to reduce the overall energy dissipation. Next the over all fault tolerant data bus energy has to be calculated and compare with the energy saved due to switching activity. By employing ECC delay also increases. Hence proposed technique has to be evaluated by considering the delay.

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