FPGA based Design and Implementation of Higher Order FIR Filter using Improved DA Algorithm

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ABSTRACT

Aerospace applications contain accelerometers that are realized with FIR filter using DA (distributed arithmetic) algorithm. When the DA algorithm is directly applied in FPGA to realize FIR filter, it is difficult to achieve the best configuration in the coefficient of FIR filter i.e. the storage resource and the computing speed. To overcome the above difficulty we proposed an improved DA algorithm. This algorithm uses splitted LUTS which results usage of small memory and operational speed increases. The specifications of decimation FIR filter will be derived from the specifications of a third-order single bit sigma-delta modulator. We propose higher order decimation FIR filter i.e. 48th order implementing with less hard ware complexity. The hardware model for the filter was realized using verilog HDL.

KEYWORDS

Fir filter, DA Algorithm, CIC Filter, Verilog, FPGA

1. INTRODUCTION

Micro Electro Mechanical Systems (MEMS) is the process of producing and combining miniaturized mechanical elements, sensors, actuators and electronics. MEMS make technology possible by developing smart products, increasing the computational ability of micro electronics with the quality and control capabilities of micro sensors and micro actuators and increase space of importance in design and application. MEMS are called "Micro machines" in Japan and "Microsystems Technology" in Europe.

In the Inertial Navigation system the Accelerometer has shown in Figure 1.1 measures acceleration of a moving object and also detects the tilt.

Accelerometer [14] is a device that detects acceleration and tilt. Accelerometers detect impact and deploy automobile airbags as well as retract the hard disk's read/write heads when a laptop is dropped.

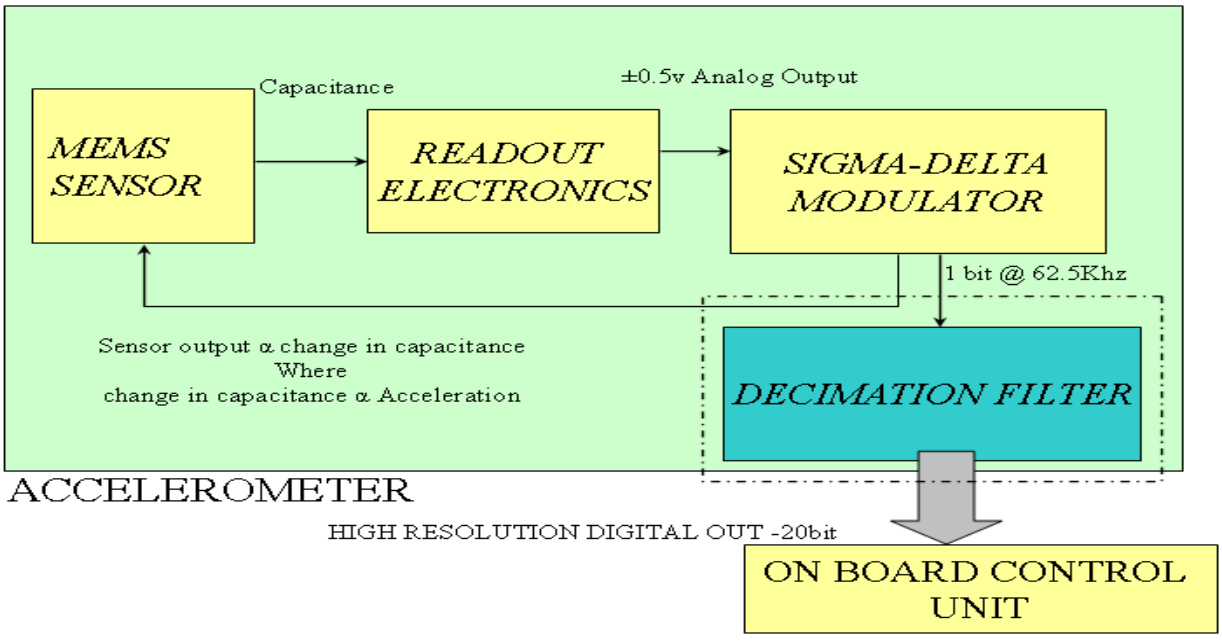

Figure 1: Block diagram of accelerometer application

Accelerometers are used in washing machines to detect excessive vibration and in pedometers for more accurate distance measurement. They also enable a handheld display to be switched between portrait and landscape modes when the unit is turned. Want to try out accelerometers and gyroscopes for yourself but don't have the resources to build them yourselves. Digital cameras employ them in their image stabilization circuits. The Figure 1 consists of 4 main blocks

1. Mems Sensor/Transducer.
2. Readout Electronics.
3. Sigma delta-Modulators.
4. Decimation Filter

1.1 MEMS Sensor

The MEMS Sensor measures changes in a differential capacitance and change in capacitance is directly proportional to acceleration.

1.2. Read out Electronics

This device is converting the continuous-time capacitance to voltage. This is made up of Op-Amp based design and feed to 3rd order Sigma-delta modulator.

1.3 Sigma-Delta Modulators

To increase speed and capability of the DSP cores. There is a need of increasing speed and accuracy of the converters associated with them. Sigma-Delta modulation based analog-to digital conversion technology is a cost effective alternative for high-resolution converters (more than 12 bits), which can be ultimately integrated on digital signal processor ICs. The basic concepts of Delta modulators and Sigma-delta converters are the use of feedback for improving the effective resolution of a quantize. The concept came up in 1954 and the patent was granted in 1960 to cutler. His system was based on generating and subtracting from the input signal the quantization error of the low-resolution quantizer placed in the forward path of a feedback loop. In 1962, it was proposed by the I nose yasuda and Murakami to add the loop filter to front end of the delta modulator and then move it inside the loop. For a Simple case of the integrator used as a loop filter, the resulting system contained an integrator in the forward path, followed by the 1-bit quantizer and the feedback loop contained only a 1-bit digital to analog converter (DAC). Since the system contained a delta modulator and the integrator, they named it as delta-sigma modulator, where sigma denoted summation performed by the integrator. It was often called Sigma-Delta modulator by later works. Today both names are in use. The output of the modulator contains the original input signal plus the first difference of the quantization error, as was the cause of the error feedback coder. Thus the both delta-sigma and error feedback coder are the noise shaping modulator. They suppress the error in the base band and thus achieve improved dynamic range across baseband independent of the signal frequency [8].

The sigma delta converters did not gain importance until the development of digital VLSI technology, which provides the practical means to implement the large digital signal processing circuitry. VLSI has helped to implement both analog and digital circuitry in one die .Since the sigma delta ADC are based on digital filtering techniques, almost 90% of the die is implemented in digital circuitry. The additional advantage of such approach is higher reliability, increased functionality and reduced chip cost [6]. Conventional high-resolution analog to digital converters, such as successive approximation and flash type converters, operating at the Nyquist rate (sampling frequency approximately equal to twice the maximum frequency in the input signal), often do not make use of high speeds achieved with a scaled VLSI technology. These Nyquist samplers require a complicated analog low pass filter (often called an anti-aliasing filter) to limit the maximum frequency input to the analog to digital converters, where as sigma-delta converters use a low resolution analog to digital converter (1-bit quantizer), noise shaping, and a very high over-sampling rate. The high resolution of the Sigma-Delta converters is achieved with help of decimation (sample rate reduction) filters, which are also called digital filters [6].

An Inertial Navigation System use motion sensors like accelerometer to continuously calculate the position and velocity of a moving object without the need for external references. Inertial-navigation systems are used in many different moving objects, including vehicles, aircraft, submarines, spacecraft, and guided missiles. In all these applications accelerometer measures changes in a differential capacitance which result from acceleration input (change in capacitance is directly proportional to acceleration and MEMS sensor output is directly proportional to change in capacitance). This capacitance is converted in to voltage using readout electronics (continuous-time capacitance to voltage converter) which is made up of op-amp based design and feed to 3rd order sigma-delta modulator whose one bit output is used for forced feedback. The MEMS sensor has got bandwidth of 100Hz. Because this the system which is following the sensor electronics (modulator) should have the band width of 100Hz and has the feature of shaping the frequencies above the bandwidth(noise shaping).All the specification required for the decimation filter is derived from the specification of sigma-delta modulator as well as from the requirement of inertial navigation system. The 20bit digital output from the decimation filter is given to computer of inertial navigational system which computes it's on updated position by integrating information received from the motion sensors.

1.4. Over-Sampling and Decimation

An over-sampling converter uses an over-sampling rate of Fs =N*Fs followed by a digital-domain decimation process to compute a more precise estimate for the analog input at the lower output sampling rate (Fs), which is the same as used by the Nyquist samplers. Regardless of the quantization process, over-sampling has immediate benefits for the anti-aliasing filter. Over-sampling in converters prevents the filters from having steep transition band, which will help for implementation of the filter. The decimation process can be used to provide increased resolution [6].

Practically it is not possible to implement a single filter that would meet the characteristic of decimation filter, because order of such filters would be close to 5000. It is impossible to implement such filters in hardware. So it is necessary to split the architecture of decimation filter in to two parts [2] those are CIC and FIR filters.

The DA algorithm was initially proposed by Crosier in 1973. It attracted attention again after the FPGA LUT (Look-up Table) was invented by Minx in the early 90s of last century and effectively applied in the design of FIR filters [1]. The decimation and filtering can be performed using different architectures, but it is very much important to know which is the best one and can be implemented in hardware using less resources. It is believed that the best architecture is the one which can be accommodated in hardware consuming less area and power.

Practically it is not possible to implement a single filter that would meet the characteristic of decimation filter [2], because order of such filters would be close to 5000. It is impossible to implement such filters in hardware. So it is necessary to split the architecture of decimation filter into two parts [3], CIC filter followed by two FIR stages as shown in Figure 2.

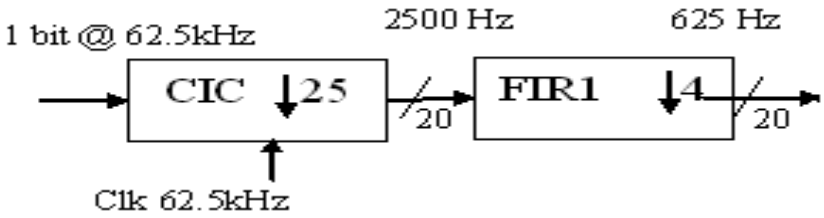

Figure 2: Architecture of decimation filter

2. CIC FILTER

Cascaded integrator-comb (CIC) digital filters were introduced to the signal-processing community, by Eugene Hogenauer [4], and mainly used in efficient implementation of decimation and interpolation. Bonus in using CIC filters, and a characteristic that makes them popular in hardware devices, is that they require no multiplication. The arithmetic needed to implement these digital filters is strictly additions and subtractions only. CIC filters are known in the field of electronics with different names, like moving average filter or recursive filter. The two basic building blocks of a CIC filter are integrator and comb. An integrator is just a single pole IIR filter with a unity feedback coefficient. This system is also called as accumulator. For decimators, the gain G at the output of the final comb section is

$$G = (RM)^N \text{ ---------- (1)}$$

Where R is rate of change and M is differential delay Assuming two's component arithmetic, the gain G is used to calculate the number of bits required for the last comb due to bit growth. If Bin is the number of input bits, then the number of output bits, Bout is

$$\text{Bit growth (Max)} = [N\log_2 RM+Bin] \text{ ---------- (2)}$$

N = Number of stages
COMB Delay = M
Input word length = Bin
R = Decimation factor

It required bit width for each stage of integrator and comb. Hardware implementation of Cascaded integrator-comb filter Decimation to a lower sampling rate is achieved by taking one sample out of every 'D' sample. The architecture for single stage CIC filter is shown in figure3. As the number of stages increases number of integrator and the comb section also increases. The order of the decimation filter is fixed to six because it has to be one more that the order of the 3rd order sigma-delta modulator plus the 2nd order MEMS sensor. When CIC filter is build six integrator section is cascaded together with six comb section and for the hardware reduction it is better to have decimation section between integrator and comb section.

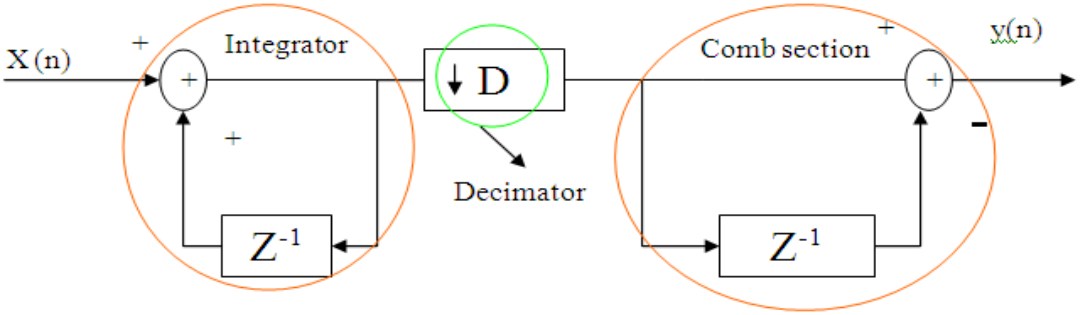

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Figure 3: Architecture of single CIC filter

3. FIR FILTER

Finite Impulse Response (FIR) Filter is one of the primary types of filters used in digital signal processing application. Since the filter does not use feedback the impulse response of the filter is finite.

3.1 FIR Filter Implementation using Distributed Arithmetic algorithm (DA)

Distributed Arithmetic (DA) is a different approach for implementing digital filters. The basic idea is to replace all multiplications and additions by a Look up Table and a shifter-accumulator. DA relies on the fact that the filter coefficients are known, so multiplying c[n]x[n] becomes a multiplication with a constant. This is an important difference and a prerequisite for a DA design. It is a powerful technique for reducing the size of a parallel multiply-accumulate hardware that is well suited to FPGA designs.

The block diagram for the DA implementation of FIR filter is shown in Figure 4. While implementing DA it is necessary to store the inputs as same as the coefficient length in buffer stage. Once it is done, the LSB of all coefficients is taken as address to LUT. That is, a 2^n word LUT is pre-programmed to accept an N-bit address, where N is number of coefficients. Individual mappings are weighted by the appropriate power of two factors and accumulated. The accumulation is efficiently implemented using a shift-adder as shown in Figure 4. For hardware implementation, instead of shifting each intermediate value by power factor which requires an expensive barrel shifter, shift the accumulator content itself in each direction one bit to the right.

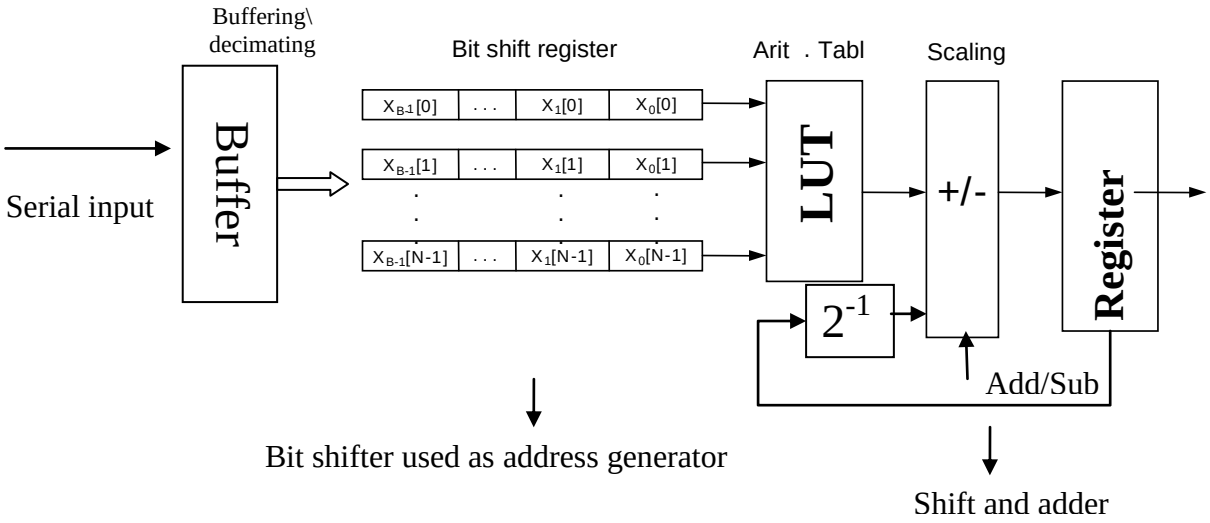

Figure 4: Block diagram of DA implementation of a FIR filter

3.2 FIR Filter Implementation using Improved Distributed Arithmetic algorithm

The Improved Distributed Arithmetic algorithm is that similar to Distributed Arithmetic with splitting of the LUTs.The number of words in Distributed Arithmetic LUT is 2^n taps which exponentially increases with n-taps. A LUT splitting method effectively reduces the memory usage. While implementing the design for decimation filter using distributed arithmetic it is not required to use poly phase structure, because it doesn't bring any benefit.

If the coefficients are small, it is very convenient to realize through the rich structure of FPGA LUT. While the coefficient is large, it will take up a lot of storage resources of FPGA and reduce the calculation speed. Meanwhile, the N-1 cycles also resulting the too long LUT time and the low computing speed. The Shunwen Xiao, Yajun Chen, presents the improvement and optimization of the DA algorithm aiming at the problems of the configuration in the coefficient of FIR filter, the storage resource and the calculating speed, which make the memory size smaller and the operation speed faster to improve the computational performance.

Figure 5 shows the Improved distributed arithmetic algorithm with Split LUT which can be used to implement a filter with higher order or coefficients is large to implement with higher order. Here it is better to use parallel tables and add the results. By using pipeline registers this modification will not reduce the speed of design, where dramatically reduces the area, because size of the LUT grows exponentially with the address space.

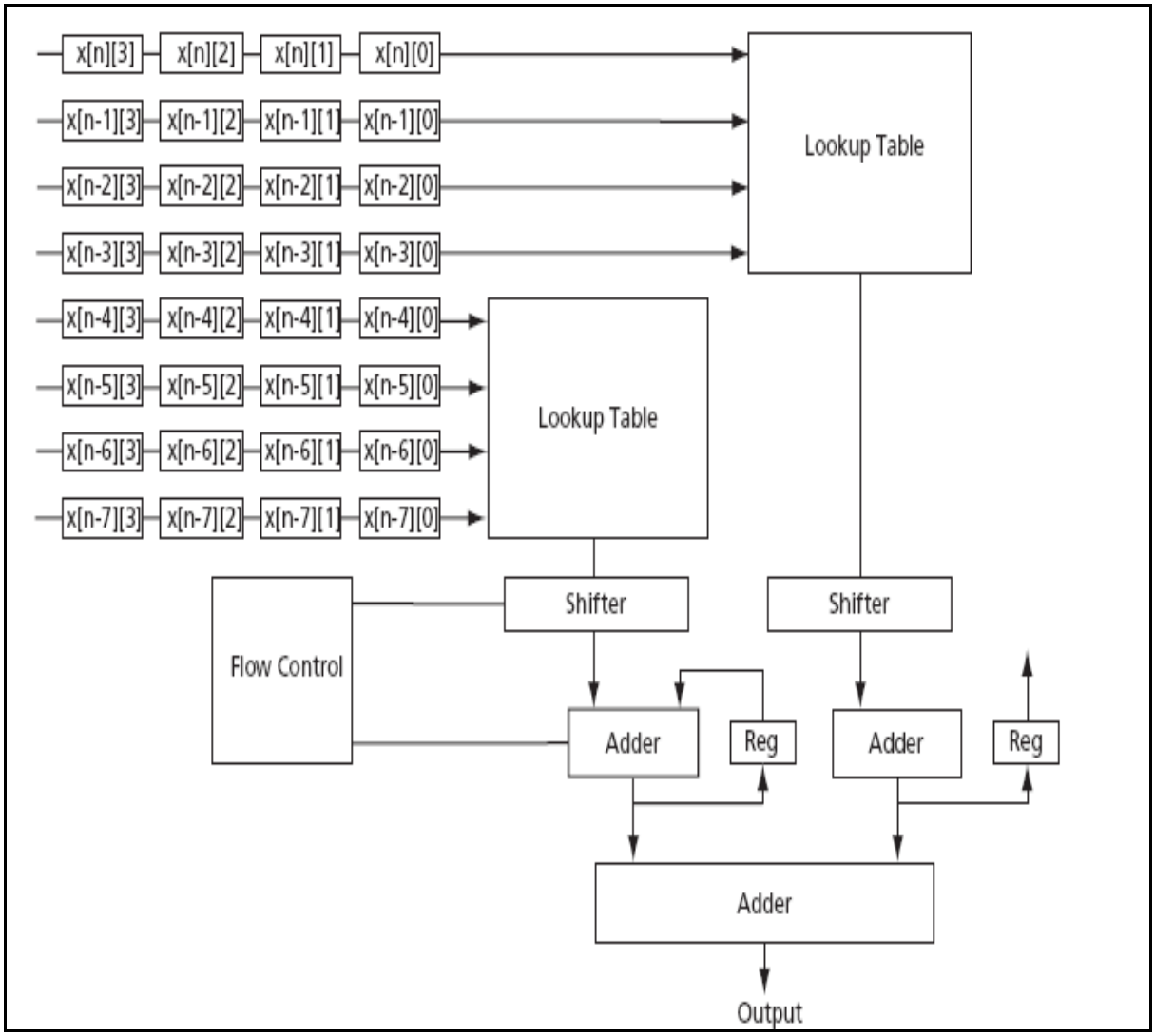

Figure 5: Block diagram of Improved Distributed Arithmetic with Split LUT

4. DESIGN SPECIFICATIONS

The specifications of the decimation filter are dependent upon the overall specification from the sigma-delta converter. So the design specifications of the sigma-delta converter is shown in table 1.

Table 1: Specifications of Sigma-delta data converter

Parameter	Symbol	Value
Signal Band width	BW	100Hz
Sampling Frequency	Fs	62.5KHz
Over sampling Ratio for 200Hz	OSR	312
Number of bits in modulator bit stream	Bmod	1

To get an SNR of 120dB, it needs OSR of 256 and above. Based on available crystal frequency (4 MHz) sampling frequency of modulator is fixed as 62.5 KHz. From the above specifications of the sigma-delta data converters, the overall characteristics of the decimation filter is as shown in Table 2.

Table 2: Specifications of decimation filter

Parameter	Symbol	Value
Pass band	Fp	100Hz
Stop band	Fstop	200Hz
Sampling Frequency	Fs	62.5KHz
Stop band ripple	Astop	120dB
Decimation factor	Df	100
Down-sampling Frequency	F_{ds}	625Hz

From the above two filters specifications now we are taking the design specifications of the CIC and FIR filters for our design of the Decimation FIR filter.

The first stage CIC is easy to implement in hardware, requiring no multiplications and it can be used to decimate the data by a large factor. One drawback of this filter is droop in the pass-band due to sin(x)/x response of the filter. Decimation factor for the CIC filter is fixed 25 based on the requirement of the intermediate frequency and order is one more that the sum of orders of sigma-delta modulator and MEMS accelerometer sensor. The specification of the CIC filter and FIR filter are shown respectively in Tables 3 & 4.

Table 3: Specifications CIC filter

Parameter	Value
Decimation factor	25
Number of sections	6
Differential Delay	1
Fs	62.5Khz

Table 4: Specifications of FIR filtering

Filter parameter	FIR filter
Sampling frequency (Fs)	2500 Hz
Pass band frequency (Fpass)	100Hz
Stop band frequency(Fstop)	200Hz
Pass band Max ripple (Apass)	0.00025 dB
Stop band attenuation (Astop)	120 dB
Decimation factor	4
Order of the filter	48

5. IMPLEMENTATION OF HARDWARE MODEL

The Top level Module of the Decimation filter and Block diagram of the Decimation filter is shown in figure 6 and 7 respectively. In which the order of the FIR filter is 48th.The Decimation architecture consists mainly CLK Divider, CIC Module and FIR Module.

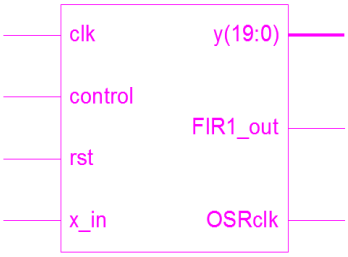

Figure 6: Top level Module of the Decimation filter

The port requirements of the hardware model are

INPUTS

CLK – 4 MHz Form Crystal Oscillator,
RST – Asynchronous Rest signal
XIN- Output Of The Sigma-Delta Modulator At The Rate Of OSR Clk

OUTPUTS

FIR2_yout – 20-bit Digital Output
FIR2_out -Output Indicator
OSR clk - OSR Clk Output for Modulator Section

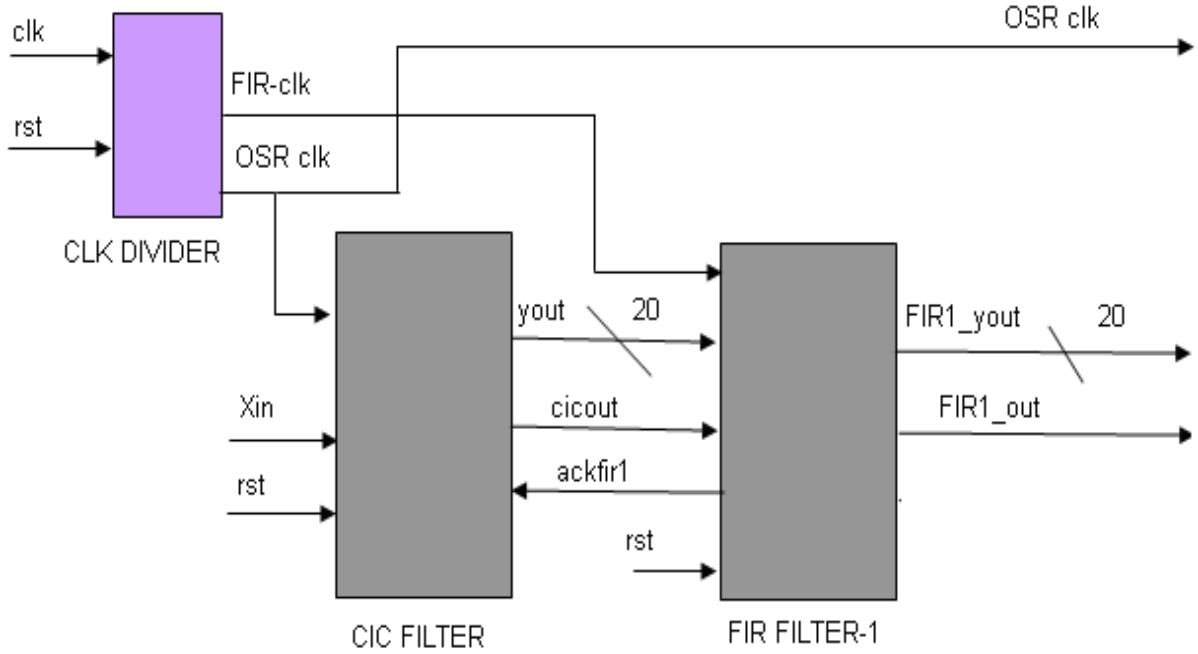

Figure 7: Hardware model Architecture of Decimation Fir filter

6. SIMULATION RESULTS

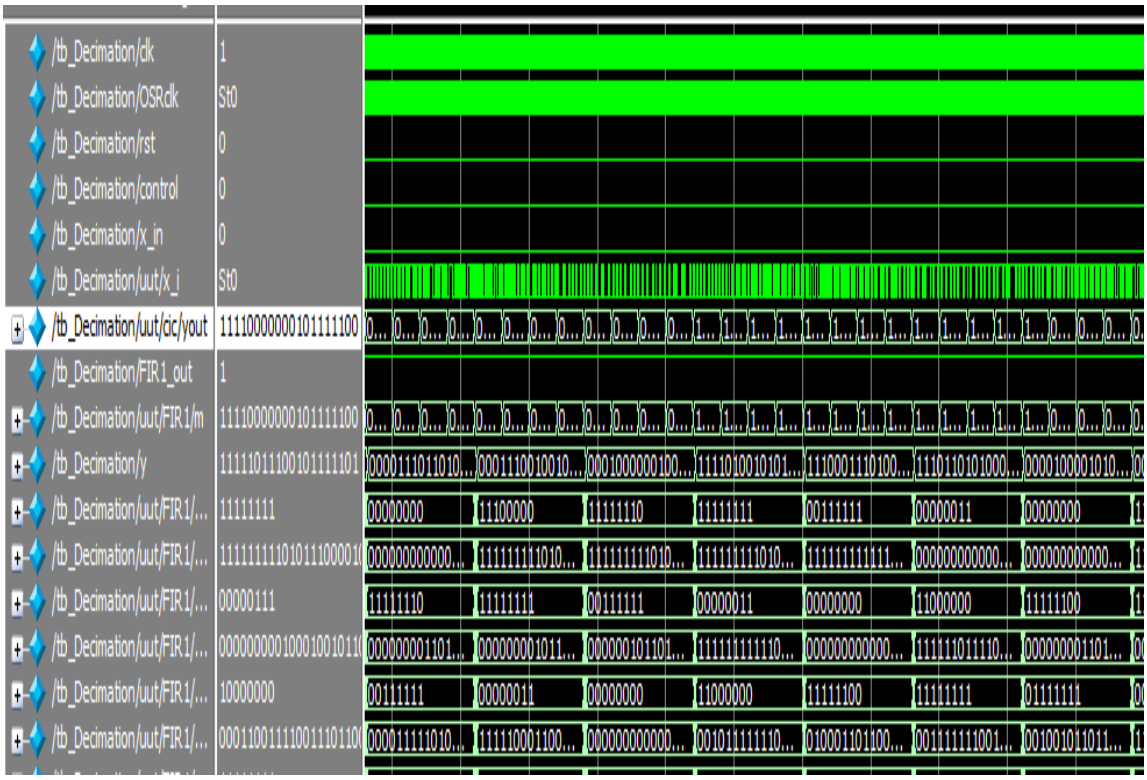

Figure 8: Simulation of CIC Filter

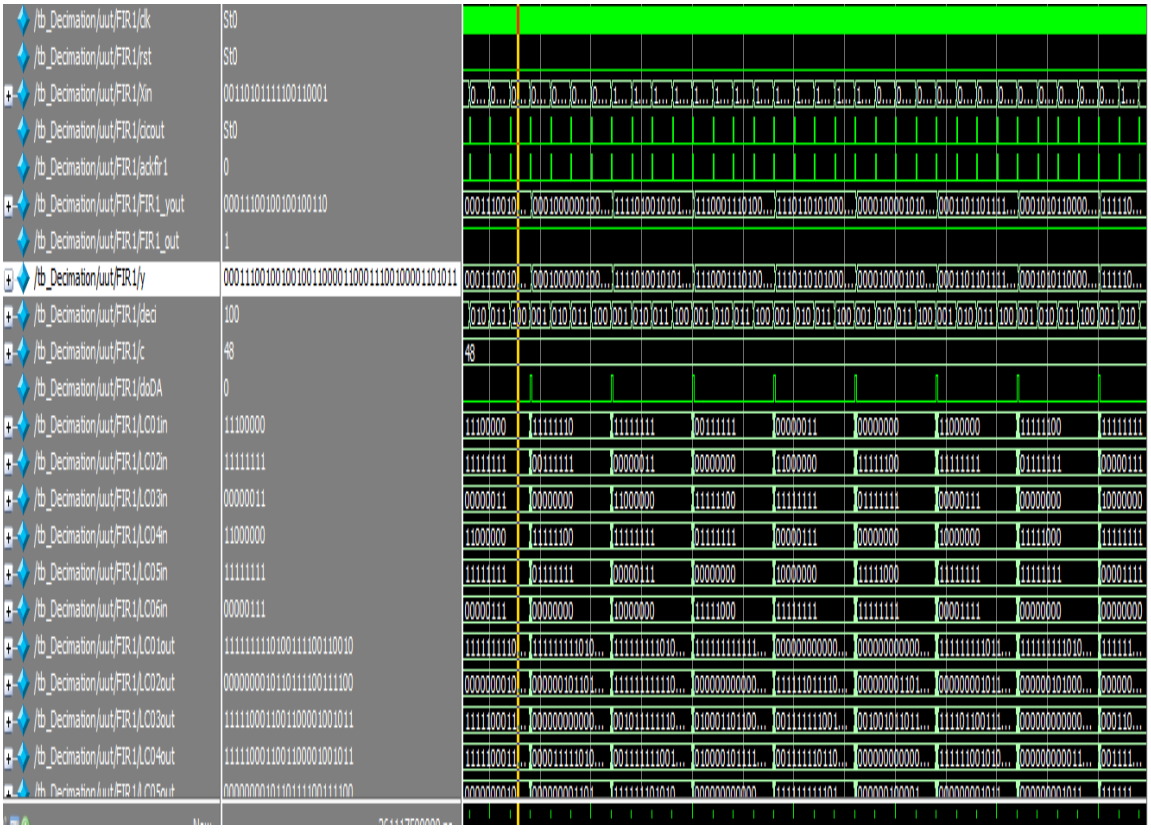

Figure 9: Simulation of FIR Filter

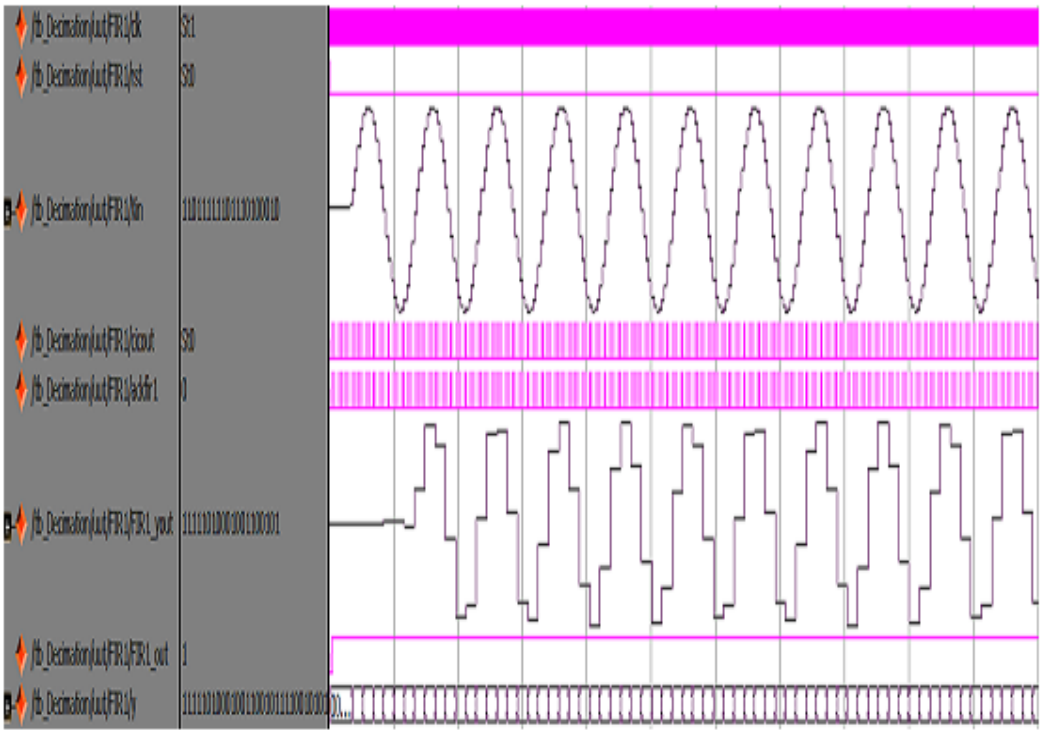

Figure 10: Simulation of CIC Filter

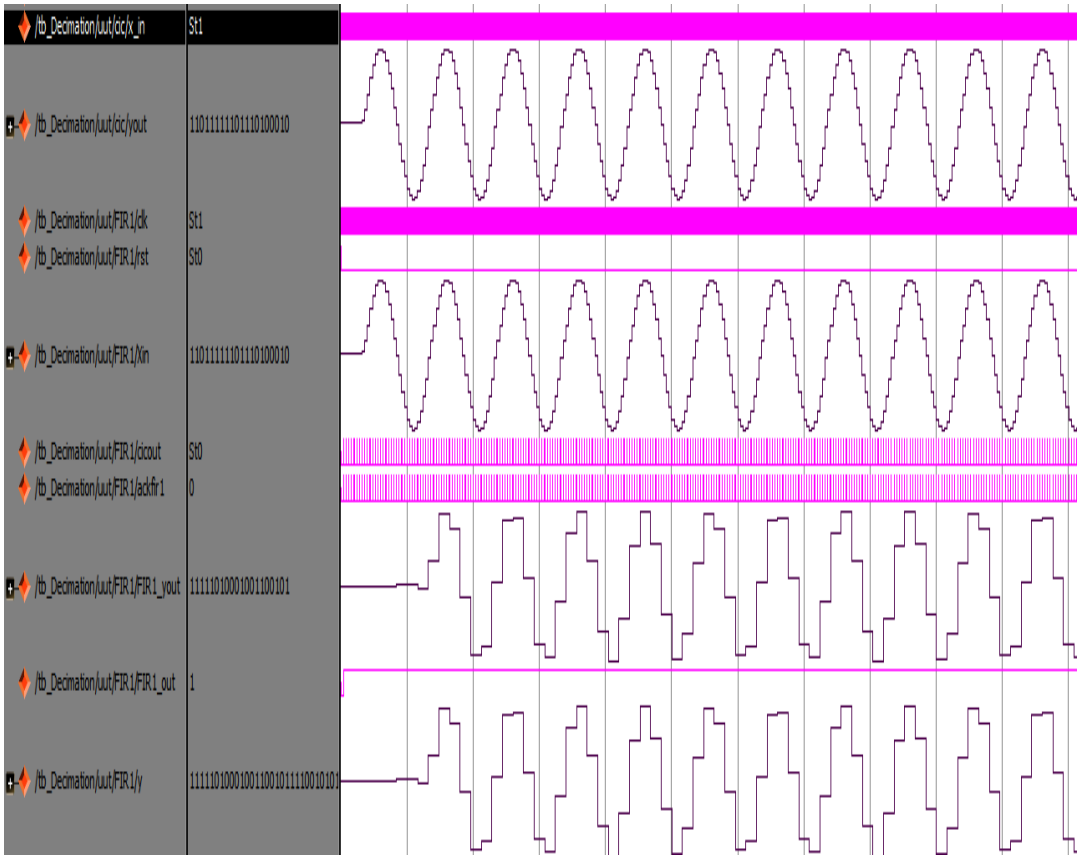

Figure 11: Simulation of FIR filter with step-input

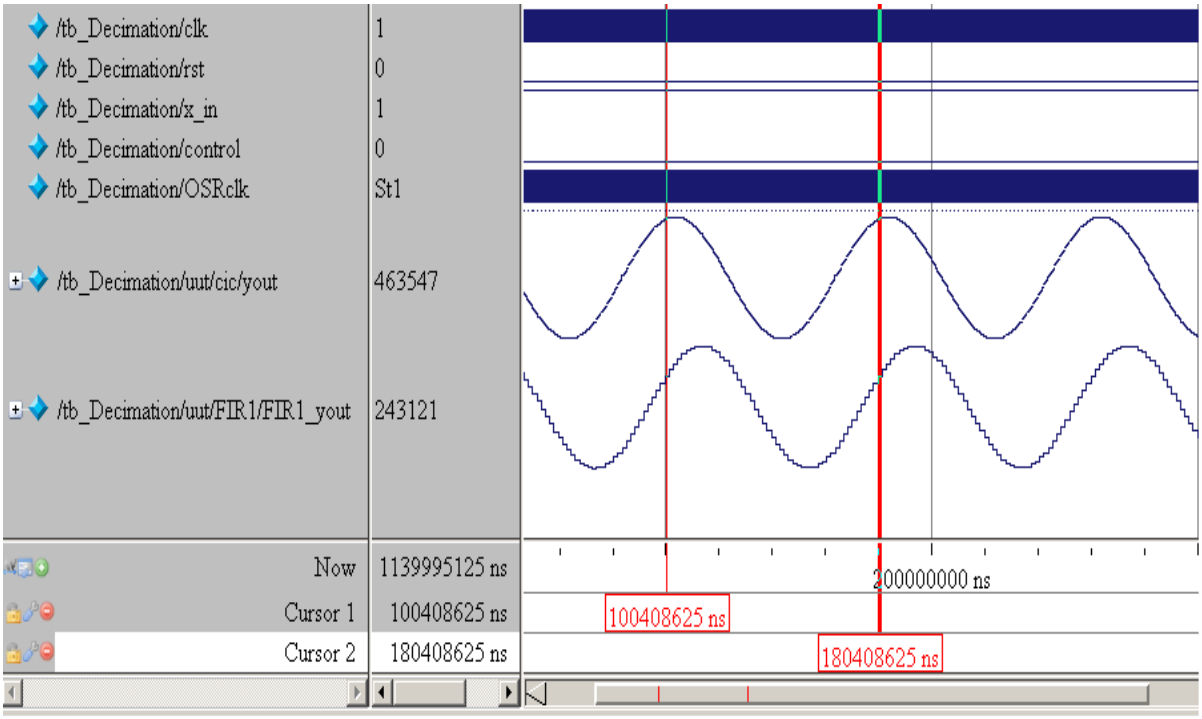

Figure 12: Sine test simulation wave form of Decimation FIR filter

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Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	3,073	9,312	33%
Number of 4 input LUTs	4,770	9,312	51%
Logic Distribution			
Number of occupied Slices	3,310	4,656	71%
Number of Slices containing only related logic	3,310	3,310	100%
Number of Slices containing unrelated logic	0	3,310	0%
Total Number of 4 input LUTs	4,782	9,312	51%
Number used as logic	4,770		
Number used as a route-thru	12		
Number of bonded IOBs	26	232	11%
Number of BUFGMUXs	4	24	16%

Figure 12: Device Utilization Summary

Table 5: Device Timing Summary

Device Timing Summary		
1	Minimum period	24.592ns (Maximum Frequency: 40.664MHz)
2	Minimum input arrival time before clock	11.729ns
3	Maximum output required time after clock	4.394ns

Figure 8 shows the simulation results of decimation FIR filter for a 12.5Hz signal at the modulator input. It is observed that output of CIC filter is 12.5Hz sine wave with higher sampling rate (2.5 KHz) and FIR filter has got the sampling frequency of 625Hz.

6. CONCLUSIONS

The Decimation FIR filter is successfully implemented and tested in software as well as in FPGA board. In this decimation FIR filter is designed and implemented in hardware using a two stage architecture (CIC filter followed by FIR filter) because it is not possible to implement the decimation filter as a single filter, due to high order of the filter. The hardware model for higher order i.e. 48 decimation filter is developed with less hardware complexity using verilog HDL.

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