Modelling of Parasitic Capacitances for Single-gate, Double-gate and Independent Double-gate MOSFET

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ABSTRACT

This paper discusses the type of capacitances for Single Gate MOSFET and Double Gate MOSFET including their quantity. The effect of parasitic capacitance makes double gate MOSFET more suitable component for the designing of digital logic switches than single gate MOSFET. Here, we introducing Independent double gate MOSFET operation based on VeSFET concept. Then introducing with the total capacitance model of Independent double gate MOSFET and compared its performance parameters with double gate MOSFET and the single gate MOSFET. Double gate transistor circuit is the first choice for reduction of short channel effect in application of MOSFET. The basic advantage of double gate MOSFET is its area required. But design CMOS double gate transistor for AND functionality suffering from high leakage current; while using Independent double gate MOSFET based on VeSFET concept reduction of that leakage current is possible. So, we can easily implement logic circuits while using CMOS design based on Independent double gate MOSFET which gives high performance.

Keywords

Junction capacitance; MATLAB simulation; DG MOSFET; VeSFET; IDG MOSFET; VLSI.

1. INTRODUCTION

The parasitic capacitances associated with a MOSFET are shown in Fig. 1 as lumped elements between the device terminals. The parasitic capacitances of Single Gate MOSFET can be classified into two major groups: one is oxide related capacitances and other one is junction capacitances. The gate oxide related capacitances are gate to drain capacitance (C_{gd}), gate to source capacitance (C_{gs}) and gate to substrate capacitance (C_{gb}). But overlap capacitance between gate to source (C_{gsp}) and gate to drain (C_{gdp}) are also included with oxide related capacitances in reality. According to the biasing of transistor; values of all oxide related capacitance will vary [1-3].

Because concept of oxide related capacitance depends upon the parallel plate formed between the polysilicon gate and the underlying structures. So it is clear that magnitude of capacitance in MOSFET related to oxide is depends upon the thickness of oxide which lies between two parallel plates and also on the length of channel and width of MOSFET. Obviously, the total gate capacitance decreases with decreasing device dimensions (W and L), yet it increases with decreasing gate oxide thickness. In submicron technologies it is defined that reduction of gate area is quite easy then reducing the gate oxide thickness.

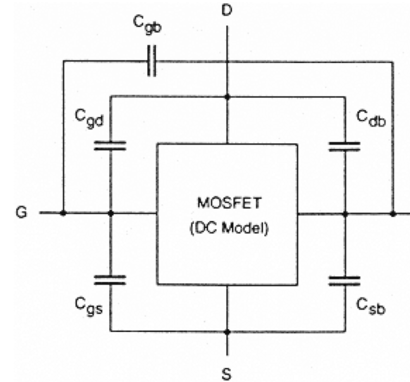

Fig 1: Parasitic MOSFET capacitances.

The second type of capacitance in MOSFET is known as junction capacitance developed between source and substrate C_{sb} other one is between drain and substrate C_{db}. These capacitances are depends upon the doping density of substrate, source and drain [2, 4]. In general DG MOSFET device had slightly thick oxides so that a very small capacitance was created with compare to SG MOSFET. The charge equation is defined by [5-7],

$$Q = C_{ox}(V_{gs} - V_{th}) \quad (1)$$

Which defined the values for the charge carrier density and also satisfied for double activated gates, the linear relationship is perfectly complied with by this charge Q where we use the term C_{ox} as total parasitic capacitance of any transistor. The drain current will defined as following equation,

$$I_{ds} = \mu_n Q V_{ds} \frac{W}{L} \quad (2)$$

Where, μ_n is the channel mobility, V_{ds} applied drain to source voltage, W and L are channel length and width respectively. Since in DG MOSFET charge Q is more as compared to SG MOSFET, due to higher capacitance values, so the drain current is higher in DG MOSFET devices. The impacts of metal-gate work function on DG MOSFET, the threshold voltage and hence on the leakage current (I_{OFF}) can be determined. If the metal-gate work function increased, threshold voltage increases and I_{OFF} decreases [8-11]. For maintaining leakage current at very low, it is necessary to increase the metal-work function or R_{OFF} should be very high as well as R_{ON} should be low, R_{ON} is defined as,

$$R_{ON} = \frac{V_{ds}}{I_d} = \frac{L}{W\mu_n Q}$$

Its low value can be achieved by the high total parasitic capacitance of MOSFET.

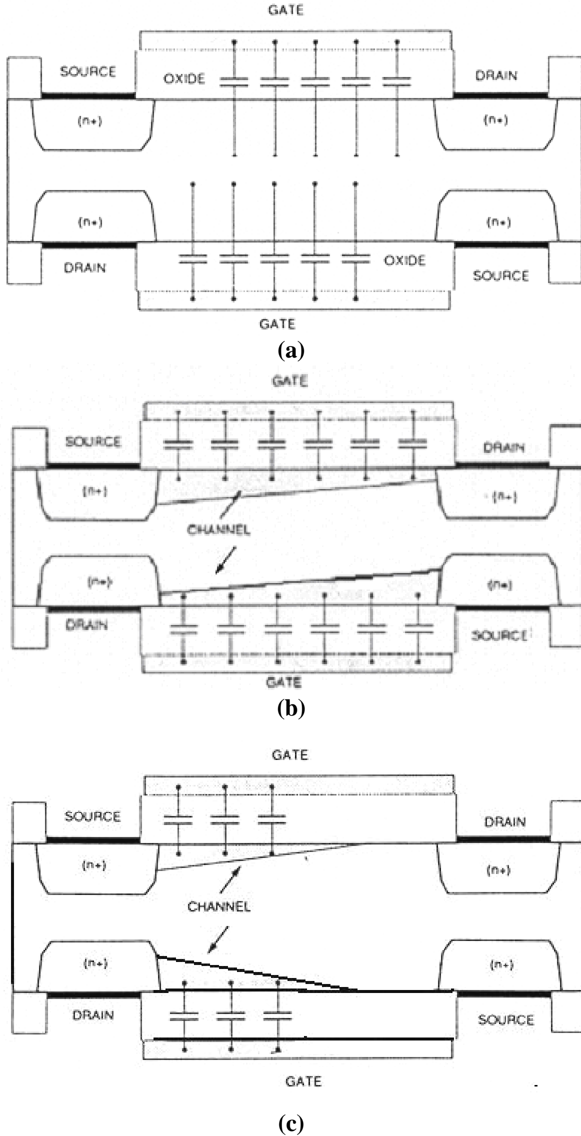

Fig 2: Schematic of DG MOSFET oxide capacitances during (a) cut-off (b) linear (c) saturation mode.

Gate to drain and gate to source overlap capacitance will perform twice in a DG MOSFET. Because they are related to the Gate and here two gates on a same substrate are designed. The gate oxide related capacitances; gate to drain capacitance (C_{gd}), gate to source capacitance (C_{gs}) and gate to substrate capacitance (C_{gb}) are also twice. According to the mode of operation of transistor values of these three capacitances varies (Fig. 2). Junction capacitance C_{sb} and C_{db} depend upon doping density of substrate (N_A) and doping density of source/drain (N_D). In DG MOSFET substrate, source and drain are common for both the gates; just because of this reason source to substrate (C_{sb}) and drain to substrate (C_{db}) capacitance are common and have same value for both gates. Rather this we know that for the region of reducing the short channel effect substrate in double gate MOSFET is lightly doped or doped negligibly [12, 13]. So, this paper explains above about the junction capacitance which depends upon doping; it should be ignored when we considering total parasitic capacitance of any DG MOSFET.

2. CAPACITANCE MODEL OF SG MOSFET AND DG MOSFET

In the previous section, the capacitances involved in the performance of single gate and double gate type transistors are connected here in a specific manner and form a capacitance model for SG MOSFET and for DG MOSFET.

2.1. SG MOSFET Capacitance

In case of linear and saturation region gate to substrate capacitance (C_{gb}) is 0. Because doping in source and drain terminals are similar to each other so that the junction capacitance C_{sb} is equal to C_{db}. In this paper $N_D = 10^{20}cm^{-3}$, $N_A = 10^{16}cm^{-3}$, $W = 10\mu m$, $Y = 5\mu m$, $L = 1.5\mu m$, $L_D = 0.25\mu m$, $X_j = 0.4\mu m$, $t_{ox} = 200Å$ and C_{ds} is negligible so it can be neglected. Similar assumptions are considered for DG MOSFET (except doping concentration) [2]. In case of saturation C_{gb} is less than that of in linear case with factor,

$$\frac{1}{2}C_{ox}WL$$

and C_{gs} in saturation is more than C_{gs} in linear region with the factor,

$$\frac{1}{6}C_{ox}WL$$

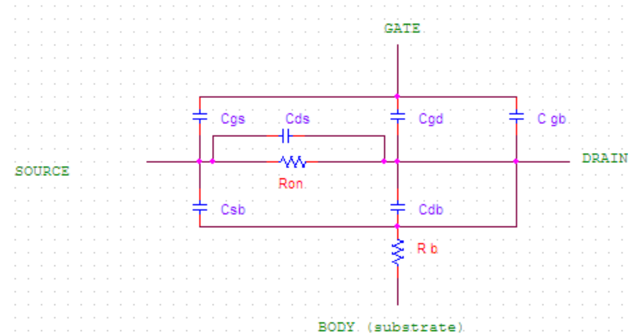

Fig 3: Parasitic Capacitance Model of a SG MOSFET.

The effective capacitance in SG MOSFET as shown in Fig. 3 is estimated as:

$$C_{SG} = \left[\frac{(C_{gs}).(C_{gb}+C_{gd})}{(C_{gs}+C_{gb}+C_{gd})}\right] + \left[\frac{C_{sb}.C_{db}}{(C_{sb}+C_{db})}\right] + C_{ds} \quad (3)$$

The ON resistance for this single gate capacitance model is the ON resistance of transistor as defined previously [14-16],

$$R_{SG} = R_{ON} = \frac{L}{[W\mu_n C(V_{gs} - V_{th})]} \quad (4)$$

So, the drain current can be observed by the ratio of drain to source voltage and ON resistance of SG MOSFET,

$$I_{d,SG} = \frac{V_{ds}}{R_{ON}} \tag{5}$$

2.2. DG MOSFET Capacitance

Here, C_{sb} and C_{db} is neglected because the value of doping profile is assumed to be 0. Also, C_{gb} is zero in saturation and linear period, neglected from model (Fig. 4). In previous section, comparison of C_{gd} and C_{gs} in linear and saturation modes are discussed they are similarly considered for DG MOSFET.

For the calculation of total R_{ON} resistance of DG MOSFET [17-20] first calculate capacitance across R_{ON1} then calculate it across R_{ON2}. Then,

$$R_{DG} = R_{ON} = \frac{R_{ON1}.R_{ON2}}{R_{ON1} + R_{ON2}} \tag{6}$$

Capacitance across:

$$R_{ON1} = \left(\frac{C_{gs1}.C_{gd1}}{C_{gs1} + C_{gd1}}\right) + C_{ds1}$$

$$R_{ON2} = \left(\frac{C_{gs2}.C_{gd2}}{C_{gs2} + C_{gd2}}\right) + C_{ds2}$$

Total capacitance of DG MOSFET,

$$C_{DG} = \frac{C_{gs1}.C_{gd1}}{C_{gs1} + C_{gd1}} + C_{ds1} + \frac{C_{gs2}.C_{gd2}}{C_{gs2} + C_{gd2}} + C_{ds2} \tag{7}$$

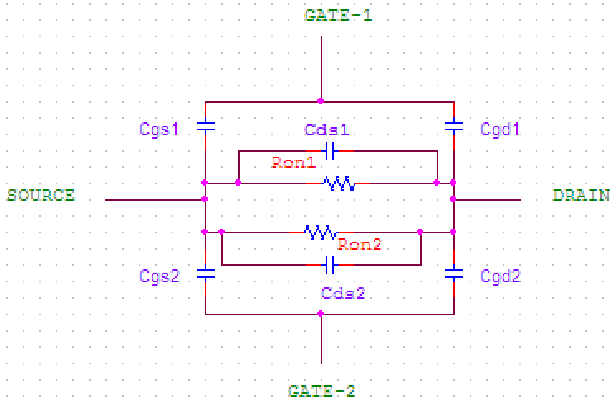

Fig 4: Parasitic capacitance model of a DG MOSFET.

If assuming that the DG MOSFET is symmetric in which both gates have the same work function and a single input voltage is applied to both gates so that the two surface channels turn on at the same gate voltage. Than, we can assume that,

$C_{gd1} = C_{gd2}$, $C_{gs1} = C_{gs2}$ and $C_{ds1} = C_{ds2}$, So,

$$C_{DG} = 2\left[\left(\frac{C_{gs}.C_{gd}}{C_{gs} + C_{gd}}\right) + C_{ds}\right] \tag{8}$$

Drain current for capacitance model shown in Fig. 4 is defined in terms of drain-source voltage as,

$$I_{d,DG} = \frac{V_{ds}}{R_{ON}} \tag{9}$$

3. COMPARISON OF DRAIN CURRENT FOR SG MOSFET AND DG MOSFET

Here, we compare drain to source current produced by one single gate MOSFET and by one double gate MOSFET with respect to drain to source voltage (Fig. 5) and with respect to their total effective capacitance of transistors (Fig. 6) which changes according to the operating region (linear and saturation) of transistor (Fig. 7). These results are obtained by assuming some parameters as an example value given in Table 1. This table also listed some calculated parameters of SG and DG MOSFET.

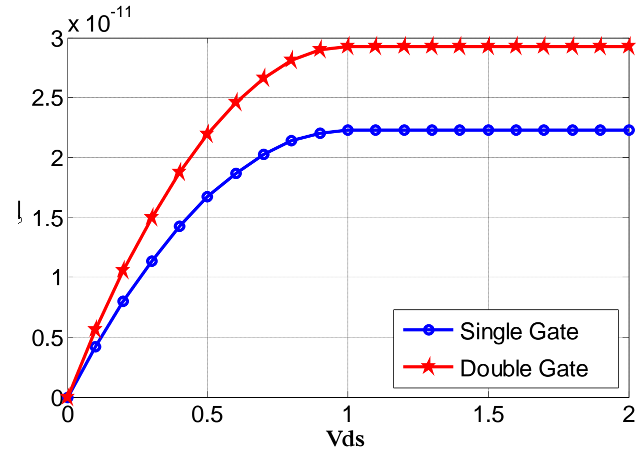

Fig 5: Simulation result of SG MOSFET and DG MOSFET for I_d Vs V_{ds}

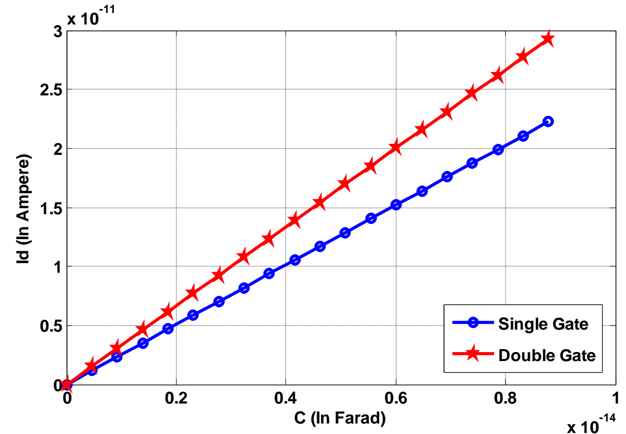

Fig 6: Simulation result of SG MOSFET and DG MOSFET for I_d Vs C (At V_{ds} = 1 Volt)

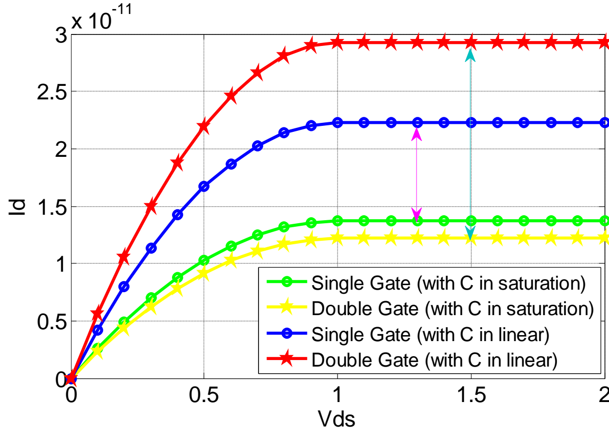

Fig 7: Simulation result of SG MOSFET and DG MOSFET operation for capacitance in linear and saturation mode.

For the DG MOSFET when both the transistors are ON, C_{sb} and C_{db} are not present so fewer signals are being coupled to the substrate as substrate is not present in this structure. So, there is no dissipation in the substrate resistance R_b. When the transistor is in the cut-off region, the increase in C_{ds1}, C_{ds2}, C_{gd1}, C_{gd2}, C_{gs1} and C_{gs2} leads to higher isolation between the source and drain, due to no capacitive coupling between these terminals. Whereas, SG MOSFET, when the transistor is ON, increasing C_{sb} and C_{db} leads to more signals being coupled to the bulk and dissipated in the bulk resistance R_b. At the transistor's cut-off region C_{ds}, C_{gd} and C_{gs} increase, which directs to lower isolation between the source and drain due to capacitive coupling between these terminals [21]. Now for Independent DG MOSFET when transistor is cut-off, the increment in C_{ds1}, C_{ds2}, C_{gd1}, C_{gd2}, C_{gs1} and C_{gs2} leads to higher isolation between the source and drain, due to no capacitive coupling between these terminals. When the transistor is ON, increasing C_{sb} and C_{db} leads to more signals being coupled to the bulk and dissipated in the bulk resistance R_b [22, 23].

Table 1. Comparison of the various circuit parameters of the SG MOSFET and DG MOSFET for the proposed model

Parameters	Results
Threshold voltage (V_{th})	1 Volt
Gate to source voltage (V_{gs})	2 Volt
Drain to source voltage (V_{ds})	0-2 Volt
Doping density of substrate (N_A)	$1x10^{16}cm^{-3}$
Doping density of source & drain (N_D)	$1x10^{20}cm^{-3}$
Oxide related gate to source capacitance (C_{gs})	$1.76x10^{-14}$ F
Oxide related gate to drain capacitance (C_{gd})	$1.76x10^{-14}$ F
Source to substrate junction capacitance (C_{sb})	$9.13x10^{-15}$ F
Drain to substrate junction capacitance (C_{db})	$9.13x10^{-15}$ F
Total effective capacitance for SG MOSFET(C_{SG})	$1.34x10^{-14}$ F
Total effective capacitance for DG MOSFET(C_{DG})	$1.76x10^{-14}$ F
ON-resistance for SG MOSFET (R_{SG})	$2.246x10^{12}\Omega$
ON-resistance for DG MOSFET (R_{DG})	$1.709x10^{12}\Omega$
Drain current of SG MOSFET (at V_{ds}=1V) ($I_{d,SG}$)	$2.23x10^{-11}$ A
Drain current of DG MOSFET (at V_{ds}=1V) ($I_{d,DG}$)	$2.93x10^{-11}$A

Since, by the calculation of capacitances with eqs. 3 and 8, we found that capacitance C_{DGM}> C_{SGM}, which shows that the isolation is better in double-gate MOSFET compared to single gate MOSFET. The relation between resistances defined as R_{DGM}<R_{SGM} which shows that the current flow from source to drain in DG MOSFET is better that SG MOSFET.

4. INDEPENDENT DOUBLE GATE MOSFET

Independent Double Gate Transistors (IDG MOSFET) are introduced here with high drain to source current and high effective capacitance with compare to previously defined SG MOSFET and DG MOSFET. IDG MOSFET can be used to implement a logic "OR" or "AND" functionality within single transistor [24].

Implementation of the "AND" functionality is rather difficult for the Independent gate configuration, as the transistor must turn "OFF" though one gate is "low" or "high", which leads in general to a significant leakage current. Circuits proposed in Chiang et al. (2006) and Mukhopadhyay et al. (2005) using transistors with the "AND" functionality suffer from these high leakage currents [25]. Vertical Slit Field Effect Transistors (VeSFET) shown in Fig. 8 can offer "OR" and "AND" functionality without suffering high leakage for the "AND" type device for the IGC [26].

In the construction of VeSFET shown in Fig. 8 square shaped unit device built on silicon on insulator (SOI) substrate, where all the transistors are isolated from each other. The four terminals are implemented by using four vertical metal pillars and the geometry based on a standard feature size in which we represent the radius by r.

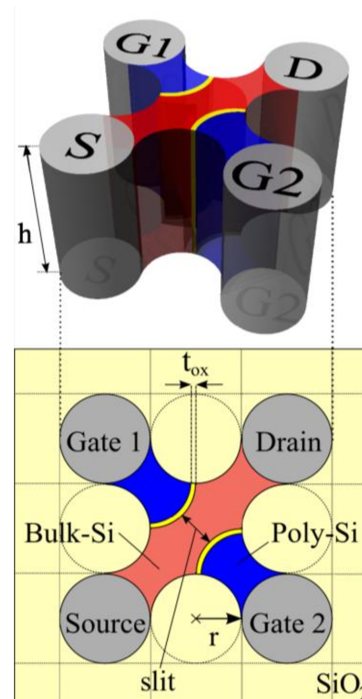

Fig 8: Vertical Slit Field Effect Transistors (VeSFET) [2].

The VeSFET is a transistor with a gate controlled bulk current using either a p- or n-type substrate for the complementary transistor types and it's a p-n junction-less transistor. It can be regarded as a hybrid of a MOSFET and a Junction Field Effect Transistor (JFET). Because its operation is based on transport of majority carriers in a bulk channel, whose effective width is controlled by depleted regions induced by two gates on both sides of this channel so it is similar to JFET. The gates, however, are separated from the channel by an insulating layer, like in a MOSFET. The current is not bound to an inversion channel but flows through the whole bulk volume between source and drain terminal this is the main difference to the MOSFET. When the transistor is off the depletion regions induced by the two gates fill the whole channel and the device is non-conducting. For a normally "OFF" transistor the gate material has to be chosen such that for a n-type transistor and the gates biased "low", the depletion widths are close to their maximum expansion, and vice versa for a p-type transistor and the gates biased "high". Conducting path from drain to source is established by applying appropriate voltages to the gates and depletion regions withdraw according to the applied voltage [27; 28].

4.1. Effective capacitance of Independent DG MOSFET

As defined with the concept of VeSFET substrate is doped and the doping concentration is depending upon the operation performed by the transistor. In IDG MOSFET, parasitic capacitances are C_{ds1}, C_{ds2}, C_{gs1}, C_{gs2}, C_{gd1}, C_{gd2} and junction capacitances are C_{sb} and C_{db} (Fig. 9). In this paper, substrate doping of $1.5\times10^{17}cm^{-3}$ for the AND-type and $5\times10^{17}cm^{-3}$ for OR-type is considered and source/drain diffusion doping is taken as 10^{20} cm^{-3} [26]. Maximum total capacitance for independent double gate MOSFET is,

$$C_{IDG} = \frac{C_{gs1}.C_{gd1}}{(C_{gs1}+C_{gd1})} + C_{ds1} + \frac{C_{gs2}.C_{gd2}}{(C_{gs2}+C_{gd2})} + C_{ds2} + \frac{C_{sb}.C_{db}}{(C_{sb}+C_{db})} \quad (10)$$

Capacitance across R_{ON1} will be,

$$\frac{C_{gs1}.C_{gd1}}{(C_{gs1}+C_{gd1})} + C_{ds1} + \frac{C_{sb}.C_{db}}{(C_{sb}+C_{db})} \quad (11)$$

Capacitance across R_{ON2} will be,

$$\frac{C_{gs2}.C_{gd2}}{(C_{gs2}+C_{gd2})} + C_{ds2} + \frac{C_{sb}.C_{db}}{(C_{sb}+C_{db})} \quad (12)$$

$$R_{IDG} = \frac{R_{ON1}.R_{ON2}}{(R_{ON1}+R_{ON2})} \quad (13)$$

Now the conclusion is that the capacitance C_{IDGM}>C_{DGM}> C_{SGM}, which shows that the isolation is best in independent double-gate MOSFET compared to single gate MOSFET. Also resistance R_{IDGM}<R_{DGM}<R_{SGM}, which shows that the current flow from source to drain in independent double-gate MOSFET is much better with respect to that of single-gate MOSFET. Here, ON-resistance (R_{ON}) of IDG MOSFET is approximately one fourth that of SG MOSFET.

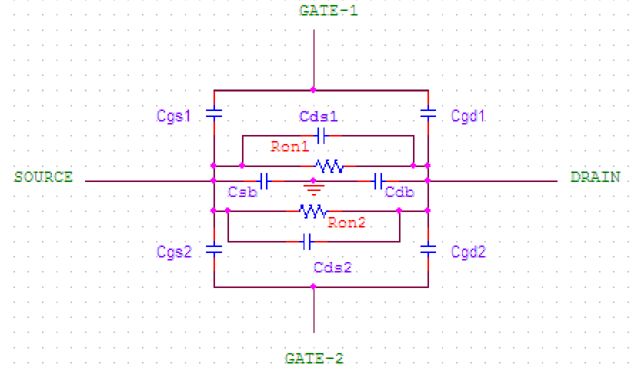

Fig 9: Model of independent DG MOSFET.

Table 2. Comparison of the various circuit parameters of the IDG, DG and SG MOSFETs for the proposed model

Parameters	**SG MOS FET**	**DG MOSF ET**	**IDG MOSFET 'AND' operation**	**IDG MOSFET 'OR' operation**
Gate/Control Voltage (V)	1.01	1.01	1.01	1.01
Number of Capacitors	5	6	8	8
Capacitance (F)	133.699 $x10^{-16}$	175.66 $x10^{-16}$	351.985 $x10^{-16}$	496.98 $x10^{-16}$
ON-Resistance (R_{ON}) (Ω)	2.246x 10^{12}	1.709x 10^{12}	0.567x 10^{12}	0.366x 10^{12}
Drain to Source Current (μA)	0.4452	0.5851	1.761	2.732

5. CONCLUSIONS

In this paper, a symmetrical SG MOSFET and DG MOSFET have been modelled and simulated by MATLAB. After designing of the DG MOSFET and SG MOSFET, we draw the layout by using OrCAD simulation. From the above results we found a better DG MOSFET compared to SG MOSFET because the total parasitic capacitance and drain to source current of DG MOSFET is greater than that of SG MOSFET i.e. shown by simulation result. So, designing of logical circuit to operate with digital signals to achieve the better isolation at lower control voltage and high switching speed is easily possible by designing the circuit with DG MOSFET rather than SG MOSFET.

Then, discuss about the Independent double gate MOSFET operation with the help of working of VeSFET, which reduces the high leakage current for the "AND" type device. After that the total capacitance model of Independent double-gate MOSFET is designed and the results are compared with the DG MOSFET and the SG MOSFET. Simulation results showed that an improved performance can be obtained. The proposed structure of IDG MOSFET offers a decrease in the short channel effect in application of MOSFET shown in Table 2. It represent mostly advantages which we consider in DG MOSFET and also reduced the problem of occurrence of high leakage current in CMOS operation. After considering its capacitance model

calculation we find that it also give a high drain to source current. So, we can easily implement logic circuits while using CMOS design based on Independent double gate MOSFET which gives high performance. However, due to high total capacitance value in the IDG MOSFET mode of operation the delay will be increased. For this reason independent double gate transistors are not fit as the first choice for high speed circuits but there main advantage is that they are perfectly used in the low power application domain.

After designing the capacitance model of the SG MOASFET, DG MOSFET and Independent DG MOSFET we can apply this for the designing of double-pole four-throw switch [29] and other applications related to the switches [30].

5. ACKNOWLEDGMENTS

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