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# Enhanced Leakage Control in Scaled 45nm nMOS Devices using $SiO_2$ and $Si_3N_4$

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## ABSTRACT
Gate-leakage reduction is the key motivation for the replacement of $SiO_2$ with alternative gate dielectrics. 45nm gate length scaled grooved and bulk nMOSFETs are evaluated to bring out the most compatible and power saving dielectric option using $Si_3N_4$ and $SiO_2$ using Silvaco ATLAS device simulator. At the scaled thickness, $SiO_2$ controls the leakage better than $Si_3N_4$, whereas at increased thickness of the dielectric $Si_3N_4$ proves better for the field scaled grooved and bulk devices with enhanced subthreshold slopes of 51.3mv/dec and 70mv/dec respectively. The field scaled device grooved at single sharp corner may be used for HP applications whereas field scaled bulk device may be used for LP and LSTP applications. This work can be helpful to device engineers working towards achieving ultra low power applications.

## General Terms
Low Power VLSI Design

## Keywords
Grooved MOSFET, bulk MOSFET, dielectric, leakage power, scaled device, dissipation

## 1. INTRODUCTION
Metal-oxide-semiconductor field effect devices need to have good performance with low cost and low power dissipation. For decades, research and development of semiconductor processing technology and device integration have focused on enhancing performance and reducing costs using $SiO_2$ as the gate dielectric and doped polysilicon as the gate electrode. The most effective way to enhance performance and reduce costs is to scale the device gate length and gate oxide [1]. Scaling the gate length results in fabricating more devices per wafer and thus reduce the cost per chip, while scaling the gate oxide enhances the drive current and reduces the short channel effects due to gate length scaling. However, as the gate oxide becomes thinner, the power to operate transistors increases because of greater gate oxide leakage current. With scaling reaching sub-50nm technology nodes, the introduction of novel materials becomes inevitable as scaling of $SiO_2$ below 3nm raises a serious concern in terms of tunneling current and oxide breakdown. The gate leakage increase of pure $SiO_2$ with EOT reduction renders inevitable the introduction of new materials like oxynitrides for the 90nm and 65nm nodes, and heightened needs for high-k in the 45nm node and below is shown in [2]. Studies towards low power multimedia applications suggest replacement of the traditional gate dielectric $SiO_2$ by the high-k dielectrics so that a thicker layer of the dielectric may be allowed without losing in gate capacitance. For a given equivalent $SiO_2$ thickness, using a high-*k* gate dielectric factor compared with $SiO_2$, achieves significant suppression of the direct-tunneling gate current and therefore results in considerable reduction in power consumption. A gate dielectric with a higher dielectric constant has been introduced at the 45nm technology which enabled more than 25X gate leakage reduction while scaling the $T_{ox}$ in [3]. Gate dielectrics such as silicon nitride ($Si_3N_4$) or oxynitride ($SiO_xN_y$), zirconium oxide ($ZrO_2$), hafnium oxide ($HfO_2$), aluminum oxide ($Al_2O_3$) and lanthalum oxide ($La_2O_3$) have been thoroughly investigated. Hafnium based dielectrics whose dielectric constants are in the range of 16-24 ensure an equivalent gate capacitance [4], but has its limitation of co integration with a polysilicon gate. For high-performance and low-operating-power logic applications, it is predicted $Si_3N_4$ or $SiO_xN_y$ will be usable through 2016[5]. This work assesses scaled grooved and bulk nMOSFETs at the 45nm node to bring out the most compatible and power saving dielectric option at the subthreshold region of operation. The subthreshold parameters obtained due to $Si_3N_4$ and $SiO_2$ at different dielectric thicknesses are compared further to analyze the static power obtained.

## 2. DEVICE SIMULATION
This work evaluates the impact of the dielectrics $SiO_2$ and $Si_3N_4$ on the field and voltage scaled grooved and bulk 45nm nMOSFET to attain better subthreshold characteristics and hence diminish the leakage power dissipation at the ultra deep submicron region. SILVACO ATLAS is used for all simulation purpose. The Devedit and Deckbuild modules of Silvaco simulator is used to obtain the results. In all simulated devices, the fixed interface oxide charge is $3x10^{10}$ $cm^{-2}$ and the operating temperature of 300K is used. The LOMBARDI CVT mobility model is used as it is a complete model including N, T, E parallel and E Perpendicular effects and Newton-Gummel method is adopted to solve the equations in this model. Arsenic is used for the source and drain to ensure shallow junctions above the oxide semiconductor interface. The important device parameters namely the gate length($L_g$), gate oxide thickness($T_{ox}$), junction depth($X_j$), silicon substrate doping

concentration($N_a$), and polysilicon gate with arsenic doping concentration($N_d$)and the supply voltage $V_{dd}$ are scaled according to constant field scaling as well as constant voltage scaling rules (**Table 1**). The uniformly doped bulk nMOS contains no type of halo doping or implants in the device. The parameters for planar devices are same as those of grooved-gate devices. The schematic of the bulk MOSFET used in this study is shown in **Figure.1.** Grooved MOSFET's with changing corner angle and applying negative junction depths are good candidates in sub-0.1-micron regime [6-8]. The device structure of the investigated grooved nMOS device used at single corner angle is shown in **Figure.2.** One of the known disadvantages of the grooved gate MOSFET structure is the thinning of gate oxide at the groove corners and consequent problems of gate oxide integrity and leakage current there. Thus enough care is taken at the vertical sharp corner inside the V groove, so that the $T_{ox}$ value may not be different than the slanted phase.

# 3. RESULTS

Thinner equivalent gate has stronger control over channel and thereby better short channel performance [9]. As various practical issues like power dissipation due to leakage, dielectric degradation and breakdown due to electrical stress, process induced defects, dopant penetration from poly-Si gate, carrier depletion in poly-Si gate, etc. limit the thickness scaling, the authors in this work consider to vary the insulator thicknesses from 1nm, 1.59nm (scaled thickness) and 6nm. The physical thickness can be increased without affecting $g_m$ as the dielectric constant of $Si_3N_4$ is almost twice that $SiO_2$, Furthermore, with higher dielectric thickness the gate leakage can be reduced and all other problems mentioned earlier are minimized. Incorporation of nitrogen at the interface suppresses dopant diffusion from gate poly-Si into the channel which can cause $V_T$ shift. Simulation Studies conducted for the field scaled as well as voltage scaled 45nm grooved and bulk polysilicon gate nMOSFETS come up with motivating results tabulated in **Table 2** and **Table 3**. Comparing with [10], the $I_{OFF}$ due to $SiO_2$ and $Si_3N_4$, at the scaled thickness $T_{ox}$=1.59nm, we find that though the S values of the field scaled and voltage scaled grooved MOSFETs are extremely depressing, those of the bulk field scaled with $SiO_2$, S=78.1mv/dec, and bulk voltage scaled with $SiO_2$, S=82.2mv/dec, the gate oxide is far more satisfactory in controlling leakage in case of the grooved device. The reason may be attributed to the fact that $SiO_2$ is an almost ideal insulating oxide, in that it has a low concentration of defects which give rise to states in the gap. This is fundamentally because it has a low coordination number, so that its bonding can relax and rebond any broken bonds at possible defect sites [11]. From **Table 3,** we find that $Si_3N_4$ thickness can be increased to 6nm to achieve both controlled leakage as well as better switching capacity. The field scaled devices endorse lower leakage current and better subthreshold slope as the electric field across the insulator is lower. When $T_{ox}$ is increased to 6.0nm, the field scaled grooved nMOSFET behaves better with an excellent subthreshold slope of 51.3mv/dec, whereas the field scaled bulk nMOSFET controls the leakage well with a comparatively high S =70mv/dec. Thus field scaled grooved at single sharp corner device may be used for HP applications whereas bulk and field scaled device may be used for LP and LSTP applications. **Figure. 3** shows the variation of static power with supply voltage applied to the devices. At $T_{ox}$=1.59, both $SiO_2$ as well as $Si_3N_4$ prove to be the power saving dielectric option for voltage scaled grooved device. If bulk devices are to be used instead of grooved ones, $SiO_2$ may be used with the supply voltage scaled to minimize static power dissipation.

**Table 1. : Standard Device Parameters according to scaling rules**

| $L_g$ (nm), | $T_{ox}$, $X_j$ (nm), $N_a$, $N_d$($cm^{-3}$), $V_{dd}$(V) **Constant Voltage Scaling** | $T_{ox}$, $X_j$ (nm), $N_a$, $N_d$($cm^{-3}$), $V_{dd}$ (V) **Constant Field Scaling** |
|---|---|---|
| 45 | 1.59, 31.5, 3.61x$10^{17}$, 3.61x$10^{20}$, 1.2 | 1.59, 31.5, 2.62x$10^{17}$, 2.6x$10^{20}$, 0.62 |

**Table 2: Leakage currents of 45nm nMOSFETS due to $SiO_2$ and $Si_3N_4$**

| 45nm nMOSFETs | $I_{OFF}$ due to $SiO_2$ [$T_{ox}$=1.59nm] | $I_{OFF}$ due to $Si_3N_4$[$T_{ox}$=1.59nm] |
|---|---|---|
| Grooved at single sharp corner and field scaled | 1.55x$10^{-15}$A/um | 1.67x$10^{-11}$ A/um |
| Grooved at single sharp corner and voltage scaled | 8.29x$10^{-16}$ A/um | 3.31x$10^{-14}$ A/um |
| Bulk and field scaled | 1.94x$10^{-12}$ A/um | 9.80x$10^{-11}$ A/um |
| Bulk and voltage scaled | 6.51x$10^{-12}$ A/um | 3.00x$10^{-12}$ A/um |

**Table 3: Subthreshold parameters of 45nMOSFETs due to $Si_3N_4$ at $T_{ox}$=6.0nm**

| 45nm nMOSFETs | $I_{OFF}$ | S |
|---|---|---|
| Grooved at single sharp corner and field scaled | 3.22x$10^{-10}$ A/um | 51.3mv/dec |
| Grooved at single sharp corner and voltage scaled | 1.33x$10^{-11}$ A/um | 100mv/dec |
| Bulk and field scaled | 4.13x$10^{-12}$ A/um | 70mv/dec |
| Bulk and voltage scaled | 7.28x$10^{-11}$ A/um | 73mv/dec |

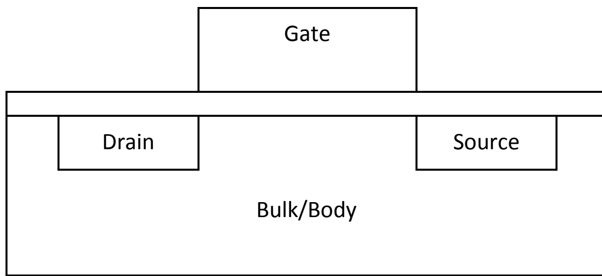


**Figure 1. Schematic of the Bulk MOSFET**

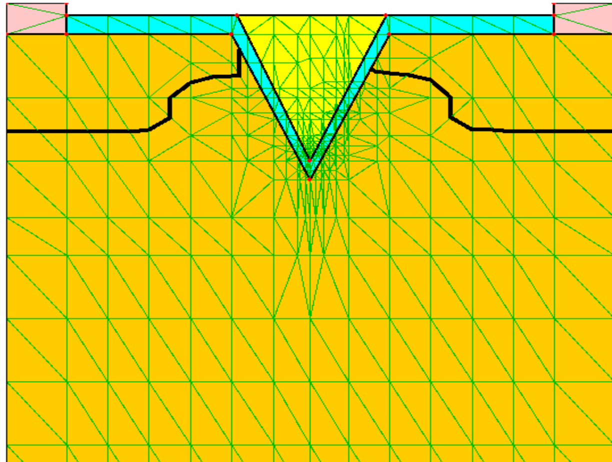

**Figure 2. Simulated structure of 45nm grooved nMOSFET**

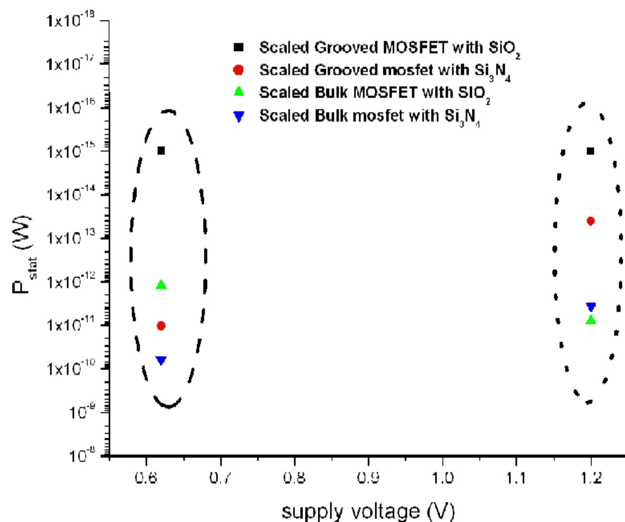


**Figure 3. Static power of Field and voltage scaled devices**

## 3. CONCLUSION

Higher K value material than the $SiO_2$ allows the actual thickness of the gate dielectric to be increased while still maintaining the same electric field in the channel. This work evaluates the impact of the dielectrics $SiO_2$ and $Si_3N_4$ on the field and voltage scaled grooved and bulk 45nm nMOSFETs to attain better subthreshold control and hence diminish the leakage power dissipation at the ultra deep submicron region. Moreover, the field scaled grooved at single sharp corner device may be used for HP applications whereas bulk and field scaled device may be used for LP and LSTP applications.

## 4. ACKNOWLEDGEMENTS

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