An Efficient Carry Select Adder Design by using different Technologies

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ABSTRACT

According to the modern research the rapid development of portable electronics is forcing the designers to elevate the existing designs for better performance. Addition is the crucial arithmetic operation used in various applications like, Digital signal processors, ALUs, math processor and in various other scientific applications. In this paper, we proposed the 1-bit CSA with gates having different values of NMOS & PMOS. Simulation results are presented at 45nm, 90nm and 180nm technologies. The performance parameters like area, power consumption and delay are observed at 45nm, 90nm and 180nm technologies using TANNER tool. In this paper, CSA are examined to study the data dependency and to recognize redundant logic operations. With the help of multiplexer, we can choose accurate output result according to the logic state of input carry signal. In this, we have removed all the redundant logic operations existing in the conventional CSA and suggested an innovative logic formulation for 1-bit CSA. The suggested CSA design comprises significantly less area and delay than in recent times suggested binary to excess-1 converter based CSA.

Keywords
Carry Select Adder (CSA), Arithmetic Unit, Low power design, SQRT CSA, Transmission Gate (TG), Ripple carry adder (RCA).

1. INTRODUCTION

Low power, area-proficient and high performance VLSI systems are increasingly used in portable and mobile devices, multi standard wireless receivers and biomedical instrumentation [5], [6]. An adder is the main constituent of an arithmetic unit. Addition is the speed limited component to make faster VLSI processors and also the most widely used arithmetic operation. As the need for higher performance processors rises, there is a continuing requirement to advance the performance of arithmetic units and to increase their functionality. A complicated digital signal processing (DSP) comprises numerous adders. A proficient adder design fundamentally improves the performance of a complex DSP system. The high speed adder architecture comprise the carry select adders, conditional sum adders, CLAs, carry skip adders and combinations of these structures[11].A ripple carry adder (RCA) uses a simple design, but carry propagation delay (CPD) is the main concern in this adder [9].The RCA is made by cascading many single-bit full adders. In RCA, when the preceding carry output signal is prepared only then every full adder can begin its operation so computation speed of RCA is slow [4]. Carry look ahead and carry select (CS) methods have been suggested to decrease the CPD of the adders.

A conventional carry select adder (CSA) is an RCA-RCA layout that produces the two outputs which are the sum and carry bits corresponding the carry input signal Cin=0 and Cin=1 and chooses one out of each pair for final-sum and final-carry [3].A conventional CSA has smaller carry propagation delay than a ripple carry adder, but conventional CSA uses a dual RCA so the design is not attractive. Few attempts have been created to circumvent the dual usage of RCA in CSA [2].

In a SQRT CSA, CSAs with increasing size are connected in a cascading structure. The main purpose of SQRT-CSA design is to provide a parallel path for carry propagation that helps to decrease the overall adder delay. The CBL-based CSA comprises significantly less logic resource than the conventional CSA. This type of CSA has more carry propagation delay, which is virtually equal to the RCA. To eliminate this problem, a square-root CSA based on CBL was proposed in. However the SQRT CSA which is designed by using CBL needs more delay and logic resources than the SQRT-CSAs which are designed by using BEC method [8]. We observe that the adder delay is depending upon the data dependence and the logic optimization depends upon the redundant operations available in the formulation. In the present designs, logic is optimized without giving any consideration to the data dependence. The logic operations comprised in the conventional and BEC-1 based CSAs are examined to study the data dependency and to recognize the redundant logic formulation for the CSA. Based on this analysis, a new CSA design is suggested which is based on the logic formulation. The main contribution in this brief is logic formulation based on data dependence and optimized carry generator and CS design [10].

Based on the suggested logic formulation, a proficient logic design for CSA is obtained. Due to optimized logic units, the suggested CSA contains significantly less ADP than the existing CSAs.

In CSA, N bits adder is separated into M parts. Every part of adder contained two RCAs with Cin=0 and Cin=1 simultaneously. According to logic state of input carry signal the accurate output result is to be selected with the help of multiplexer. The present adder stage does not need to wait for the preceding stage's output carry signal so the CSA can calculate faster. The summation result is prepared before the input carry signal accomplishes; hence in every single bit adder, an accurate computation result is arrived by waiting for only one multiplexer delay. In the CSA, the CPD may be decreased by M times than the RCA [4], [12].

In this paper, we suggested an area-proficient CSA by sharing the common Boolean logic. After Boolean simplification,

duplicated adder in conventional CSA can be removed. Congruently in every single bit adder block duplicate sum and carry out signal can be generated. Here in conventional CSA, original characteristics of parallel architecture can presented by utilize the multiplexer to choose a precise output in accordance to its preceding carry output signal. Hence circuit area, transistor count and PDP of the circuit can be decreased to a great extent[12].

In digital electronics, the research efforts of the earlier years have been focused in the direction of the low powered digital systems. The power dissipation is the most crucial design parameter specify by the need of probability and the modest enhancement in the performance of battery. The requirement of the mobility and probability is increased gradually. Also in probability, the chip area is taken into considerations. Consequently the area, power consumption and delay are the three main factors which describe the superiority of the circuit and also used to compare the numerous circuit styles.

The three main causes of power consumption in digital complementary metal oxide semiconductor circuits as shown in the below equation:-

$$P_{total} = P_{switching} + P_{short-circuit} + P_{leakage}$$

$$= (\alpha_{0 \to 1} \times C_L \times V_{dd}^2 \times f_{clk}) + (I_{sc} \times V_{dd})$$

$$+ (I_{leakage} \times V_{dd})$$

In the given equation, $P_{switching}$ indicates the power switching component, C indicates the load capacitance, f_{clk} indicates the frequency of clock signal and $\alpha_{0 \to 1}$ specifies the node transition activity factor. The $P_{short-circuit}$ is because of the direct path short circuit currents, I_{sc} which appears when NMOS and PMOS transistors together are concurrently ON and current leads directly from V_{dd} which indicates supply voltage to Gnd which is ground. Finally, leakage current $I_{leakage}$ which may appears from substrate injection and sub threshold effects is primarily determined by manufacture technology considerations. Yet the best effectual way to decrease the power consumption is supply voltage reduction and such reduction needs new design approaches for less power and low voltage ICs. Because of the glitching present the circuit, 15-20% of the total power is to be dissipated and by decreasing the glitches of the circuit low power may also be attained [1].
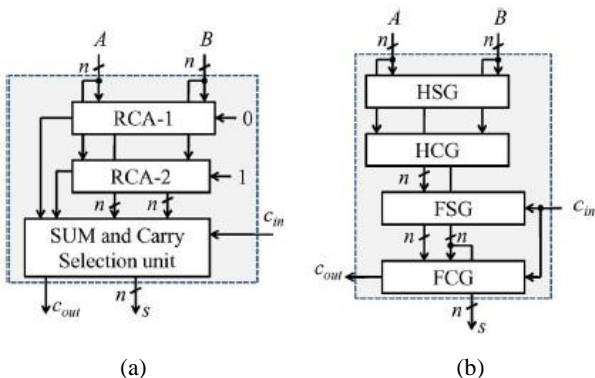

(a)

(b)

Fig 1: (a) Conventional CSA; *n* is the input operand bit-width. (b) The logic operations of the RCA is shown in split form, where HSG, HCG, FSG, and FCG represent half-sum generation, half-carry generation, full-sum generation, and full-carry generation, respectively [10].

1.1 Logic Expression of the SCG Unit of the BEC-Based CSA

As shown in Fig. 2, the RCA computes n-bit sum s01 and c0 out corresponding to cin=0. The BEC unit accepts s01 and c0 out from the RCA and generates (n+1)-bit excess-1 code. The most significant bit (MSB) of BEC characterizes c1 out, in which 'n' least significant bits (LSBs) characterizes s11.

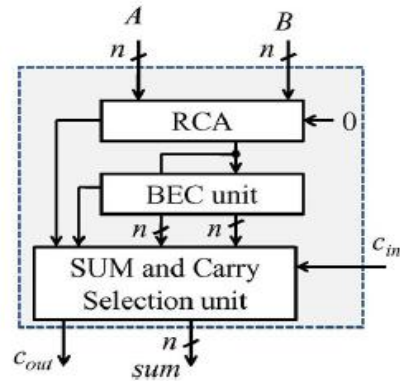**Fig 2: Structure of the BEC-based CSLA; *n* is the input operand bit-width [10].**

The CSA has two units:

1) The sum and carry generator unit (SCG) and
2) The sum and carry selection unit (SCS) [7]

The SCG unit consumes most of the logic resources of CSA and significantly contributes to the critical path. Different logic designs have been suggested for effective implementation of the SCG unit. We made a study of the logic designs suggested for the SCG unit of conventional and BEC-based CSAs of [5] by appropriate logic expressions. The main purpose of this study is to identify redundant logic operations and data dependence. Consequently, we eradicate the all redundant logic operations and sequence logic operations based on their data dependence.

2. DESIGN STYLE

The 1-bit CSA is made by 30 transistors by using the transmission gate (TG) technology. In these circuit designs, the simulation is run by using 45nm, 90nm and 180nm technologies at distinct gate width of NMOS and PMOS transistors. The minimum length used for both transistors are 0.18μm and power supply used to run the circuit is 1.7v.
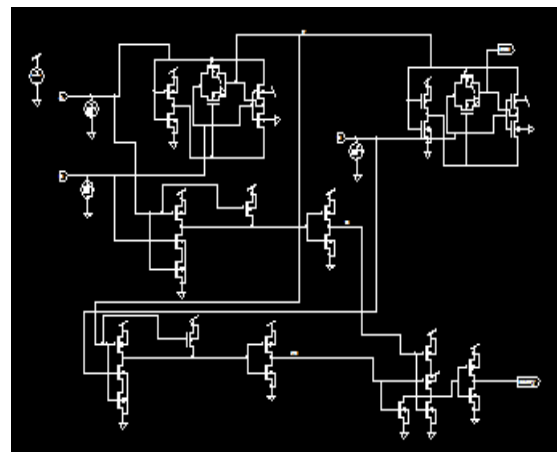

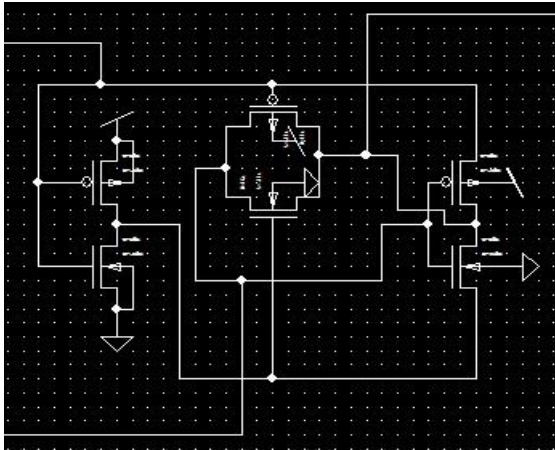**Fig 3: Circuit Diagram of 1-bit CSA by using TG Technology**
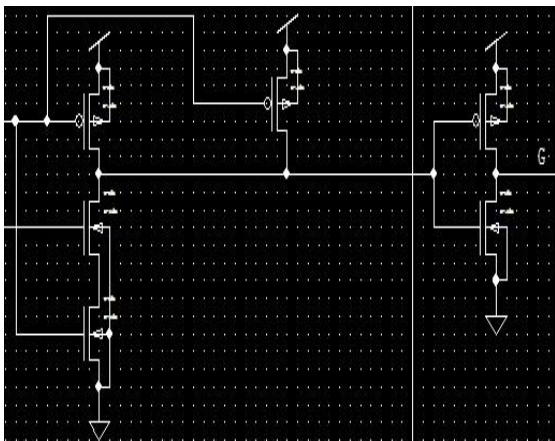
Fig 4: XOR Gate used in Circuit

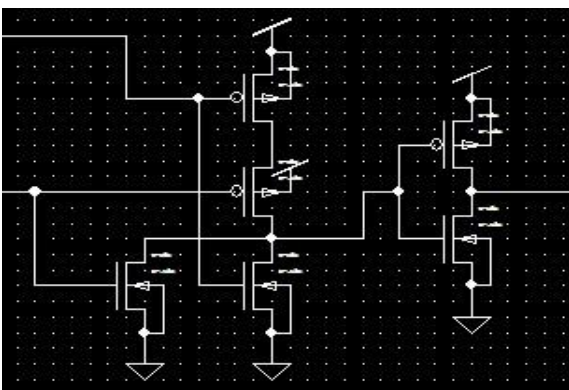**Fig 5: AND Gate used in Circuit**

Fig 6: OR Gate used in Circuit

3. FINAL RESULT

The performance parameters of 1-bit CSA are as shown below.

The below tables shown the results of 1-bit Carry select adder using 45nm, 90nm and 180nm technologies are carried at different gate widths.

Table 1. Specifications of 1 Bit CSA adder at 45nm technology

Design Style	No. of transistors	Supply Voltage (V)	Minimum Length (μm)	Width of NMOS(μm)	Width of PMOS (μm)	Avg. Power Consm. (watts)	Prop. Delay at carry(sec)
CSA	30	1.7	0.18	0.64	1.7	15.85×10^{-6}	1.2275×10^{-9}
CSA	30	1.7	0.18	1.28	3.4	16.54×10^{-6}	6.4926×10^{-10}
CSA	30	1.7	0.18	2.56	6.8	17.91×10^{-6}	3.4207×10^{-10}

Table 2. Specifications of 1 Bit CSA adder at 90nm technology

Design Style	No. of transistors	Supply Voltage (V)	Minimum Length (μm)	Width of NMOS(μm)	Width of PMOS (μm)	Avg. Power Consm. (watts)	Prop. Delay at carry(sec)
CSA	30	1.7	0.18	0.64	1.7	16.20×10^{-6}	1.1789×10^{-9}
CSA	30	1.7	0.18	1.28	3.4	17.16×10^{-6}	$5.9973^x \times 10^{-10}$
CSA	30	1.7	0.18	2.56	6.8	19.04×10^{-6}	3.1629×10^{-10}

Table 3. Specifications of 1 Bit CSA adder at 180 nm technology

Design Style	No. of transistors	Supply Voltage (V)	Minimum Length (μm)	Width of NMOS(μm)	Width of PMOS (μm)	Avg. Power Consm. (watts)	Prop. Delay at carry(sec)
CSA	30	1.7	0.18	0.64	1.7	19.01×10^{-6}	1.0903×10^{-9}
CSA	30	1.7	0.18	1.28	3.4	20.35×10^{-6}	5.968×10^{-10}
CSA	30	1.7	0.18	2.56	6.8	22.63×10^{-6}	3.2173×10^{-10}

4. CONCLUSION

The TG is an effective and widely recognized design methodology to construct CSA adders. In this paper, CSA has been compared using 45nm, 90nm and 180nm technologies. It is concluded that, the results are calculated with different widths of NMOS & PMOS. By doing this, a proficient design is achieved for the CSA. This CSA design includes less delay, area and less power consumption than in recent times suggested binary to excesss-1 converter based CSA. Because of the less output carry delay, the suggested CSA design is the best for the SQRT adder.

CSA, in this paper, is designed by sharing the CBL term; the transistor count in this CSA can be decreased to a great extent. Moreover, the power consumption and delay also reduced at a great extent. From the above tables it is conclude that when width of NMOS is 0.64**μm**& width of PMOS is 1.7**μm** then CSA consume less power and lesser delay and when width of NMOS is 1.28**μm**, 2.56**μm** and width of PMOS is 3.4**μm**, 6.8**μm** then CSA consume more power and more delay. The suggested design technique has been applied for the implementation of 1-bit CSA adder and simulation results verified its proficiency.

5. REFERENCES

[1] DJ. M. Rabaey, Digital Integrated Circuits," IEEE Trans. on VLSI Systems, 2003.

[2] O. Bedrij, "Carry Select Adder," IRE Trans. on Electronic Computers, Vol. EC-11, pp. 340-346, 1962.

[3] B. Ramkumar, H.M. Kittur, and P. M. Kannan, "ASIC implementation of modified faster carry save adder," Eur. J. Sci. Res., vol. 42, no. 1, pp. 53–58, 2010.

[4] I.-C. Wey, C.-C. Ho, Y.-S. Lin, and C. C. Peng, "An area-efficient carry select adder design by sharing the common Boolean logic term," in Proc. IMECS, 2012, pp. 1–4.

[5] K. K. Parhi, VLSI Digital Signal Processing. New York, NY, USA:Wiley, 1998.

[6] A. P. Chandrakasan, N. Verma, and D. C. Daly, "Ultralow-power electronics for biomedical applications," Annu. Rev. Biomed. Eng., vol. 10, pp. 247–274, Aug. 2008.

[7] Y. Kim and L.-S. Kim, "64-bit carry-select adder with reduced area," Electron. Lett., vol. 37, no. 10, pp. 614–615, May 2001.

[8] B. Ramkumar and H.M. Kittur, "Low-power and area-efficient carry-select adder," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 20, no. 2, pp. 371–375, Feb. 2012.

[9] T. Y. Ceiang and M. J. Hsiao, "Carry-select adder using single ripple carry adder," Electron. Lett., vol. 34, no. 22, pp. 2101–2103, Oct. 1998.

[10] Basant Kumar Mohanty and Sujit Kumar Patel, "Area–Delay–Power Efficient Carry-Select Adder," IEEE Transactions on Circuits and Systems—Ii: Express Briefs, Vol. 61, No. 6, June 2014.

[11] I. Koren and A.K. Peters, "Computer Arithmetic Alogrithms,"2nd ed. Boca Raton, FL. USA: CRC Press, 2002.

[12] Garish Kumar, Amit Grover, Gurpreet Singh and Neeti Grover, "An efficient Carry select adder design by using the 180nm technology," IJACSA, 2013.