Low Power 10T XOR based 1 Bit Full Adder

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ABSTRACT
The popularity and necessity of portable electronic systems by users have strongly influenced VLSI designers to make great effort for reduced silicon area, improved speeds, long duration battery life, and great reliability. The VLSI designers always try to save power consumption while designing a system. In this paer, an efficient methodology is presented to improve the output swing level of GDI gates. New designs of GDI based basic digital (AND, OR, XOR, XNOR) gates are presented using single pass transistors to improve swing level of GDI gates. The new design of basic gates with combination of GDI logic and pass transistor logic is called hybrid GDI technique. Compared to existing GDI technique with buffer restoration circuits, hybrid GDI implementation provides full swing output voltage in all digital circuits. Also it shows less power and less delay with about 60% area increase as compared to basic GDI.

Keywords
GDI, Full Adder, XOR, XNOR, Low power

1. INTRODUCTION
As the technology scales downs, below 100nm, reduction of power consumption and overall power management on single chip have become primary design issue. Power optimization is also important for many designs to minimize package cost and maximize battery back-up of system. Power optimization is possible at each level of design process from higher architecture level to lower physical level. At the circuit level, optimization of power has a good impact on overall power dissipation of chip [1-2]. Minimizing power consumptions calls conscious effort at different levels of the overall design process [2]. In VLSI (Very Large Scale Integration) design, CMOS (Complementary Metal Oxide Semiconductor) processes are widely used and compleletely replaced nMOS process and bipolar transistor processes for designing all digital logic systems [3]. Circuit level choices have a good impact on power dissipation of CMOS circuits. Usually, a number of approaches and topologies are available for implementing various logic and arithmetic functions.

Recently, the GDI (Gate Diffusion Input) technique is emerged as a promising alternative to Standard CMOS Logic [4]. The GDI technique has reduced power dissipation and less delay with least number of transistor counts in design of any digital system. Similar to other existing techniques, GDI also suffers from low output swing voltage problem due to low threshold voltage [4, 5]. This research work tried to overwhelm this problem by adding an additional pass transistor to GDI cell. Implementations of proposed method in few digital circuits provide better result in terms of power reduction and delay.

For designing any digital circuits, the main performance parameters are power, delay and area. Circuit which consume low power, less delay and occupies less area is considered as best circuit. Portability imposes a strict limitation on power dissipation with the demands of high computational speeds. Recently, the GDI (Gate Diffusion Input) technique is emerged as a promising alternative to Standard CMOS Logic[6-9]. The GDI technique has reduced power dissipation and less delay with least number of transistor counts in design of any digital system. Similar to other existing techniques, GDI also suffers from low output swing voltage problem due to low threshold voltage. This research work tried to overwhelm this problem by adding an additional pass transistor to GDI cell. Implementations of proposed method in few digital circuits provide better result in terms of power reduction and delay [10].The main concentration of this research is to find out the low power circuit/ transistor level technique for digital circuit design. Hence different circuit styles from traditional to existing techniques are reviewed. Various research findings and merit-demerits of all techniques are discussed [11].

The Gate Diffusion Input technique (GDI) provides the implementation of different complex functions using only two transistors. Compared to CMOS and existing PTL techniques, the GDI technique is suitable for design of fast and low power circuits using reduced number of transistors [12-13]. The GDI method is based on the use of simple cell which looks exactly like the basic inverter. The detail methodology of GDI is explained in next chapter. Here we explained few research findings about GDI technique.

The GDI approach allows implementation of a wide range of complex logic functions using only two transistors This method is suitable for design of fast, low power circuits, reduced number of transistors while allowing simple top-down design. Gate-Diffusion-Input (GDI) design technique is an efficient alternative for the logic design in standard CMOS and SOI technologies [14].

Table 1. Logic Faction Implementation with GDI Technique

N	P	G	Out	Function
0	B	A	$\overline{A}$.B	F1
B	1	A	$\overline{A}$+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	$\overline{A}$B+AC	MUX
0	1	A	$\overline{A}$	NOT

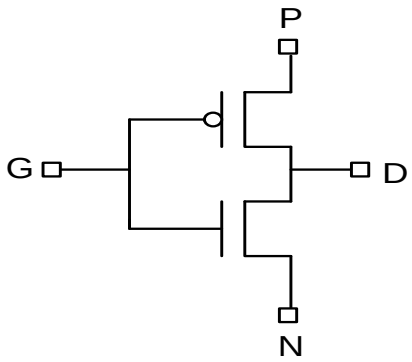

Fig.1. Symbol of GDI cell

GDI cell has four terminals input output – G node (the common gate input of the NMOS and PMOS transistors), P node (the outer diffusion node of the PMOS transistor), N node (the outer diffusion node of the NMOS transistor), D node (the common diffusion of both transistors) as shown in Fig.1. P, N and D it can be treated as either input or output nodes, depending on the circuit structure shown in Fig.1 Bulks of both NMOS and PMOS are connected to N or P (respectively), so it can be arbitrarily biased in contrast with CMOS inverter. Multiple-input gates can be implemented by combining several GDI cells [9]. GDI enables simpler gates, lower transistor count, and lower power consumption in many implementations. This technique allows reducing power consumption, propagation delay, and area of digital circuits while maintaining low complexity of logic design. The overall area and complexity of the circuit is minimized using GDI technique .Also improvements are observed in static power dissipation and logic level swing. Most of the functions which are complex (6-12 transistors) in CMOS, are very simple (only 2 transistors per function) in GDI design method.

2. STATIC ENERGY RECOVERY FULL ADDER (SERF)

A new high speed, low power and area occupation, we designed a Static Energy Recovery Full adder (SERF) cell module basically 10T. The design was inspired by the XNOR gate full adder design [10]. In non-energy recovery design the charge applied to the load capacitance during logic level high is drained to ground during the logic level low. It should be noted that the new SERF adder has no direct path to the ground as shown in Fig.2. The elimination of a path to the ground reduces power consumption, removing the Psc variable (product of Isc and voltage) from the total power equation. The charge stored at the load capacitance is reapplied to the control gates [11].

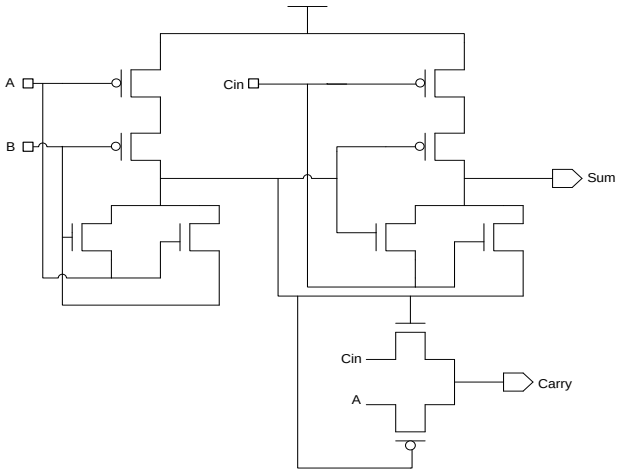

Fig.2. Schematic of SERF Full Adder

3. PROPOSED WORK

Addition forms the basis for many processing operations from counting to multiplication to filtering. As a result, adder circuits that add binary numbers are of great interest to digital system designers. In proposed full adder circuit designed using Hybrid GDI XOR and XNOR gate of 10T full adder formation, two XOR perform SUM operation and Carrey is performed by the two pass transistor as shown in Fig.3. Only 10 transistors are used to design one bit full adder. Here PMOS and NMOS transistors are added with basic GDI XOR cell to improve swing restoration. Less transistor count results less load capacitance values and hence the switching power dissipation is less in hybrid GDI based full adder compared to other techniques. Output waveform of Sum and Carrey is shown in Fig.4.

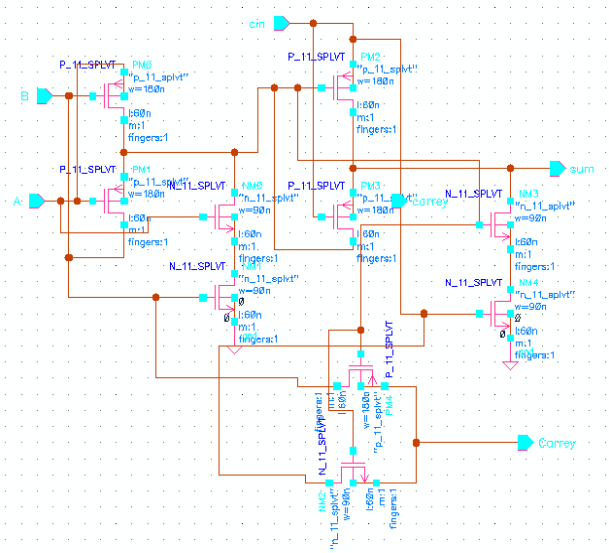

Fig.3. 10T XOR gate Full Adder

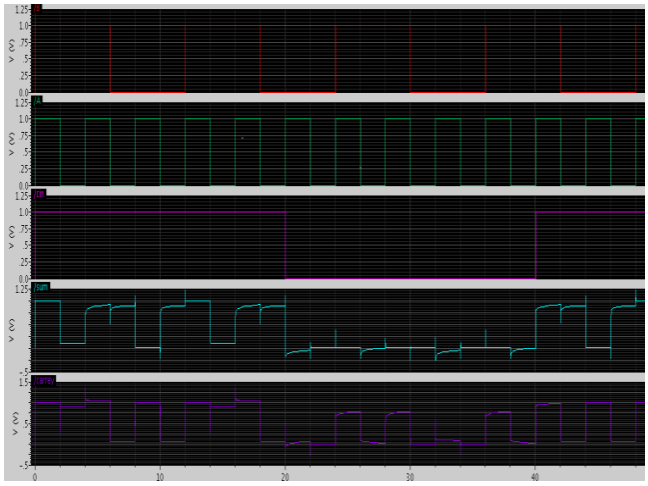

Fig.4. Output Wave Form of Proposed 10T Full Adder

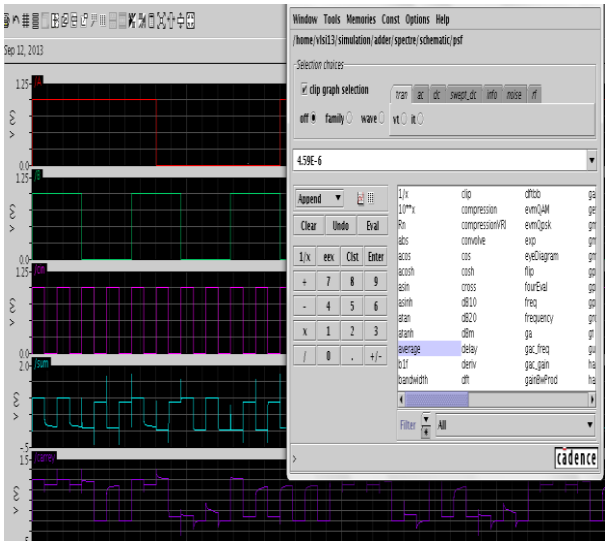

Fig.5. Power Graph of 10T XOR Gate

4. RESULTS & DISSCUSSION

All simulation of proposed XOR adder is performed in Cadence Virtuoso at 180nm CMOS technology. Supply voltage is of 1.8V at 27^0c with CL=1pf, all the parametric analysis of the circuit is shown with the variation of supply voltage 0V to 1V to analysis the variation of average power consumption of proposed adder. Simulation is carried out for Power, delay and PDP. As Shown in Table II. Proposed 11T and 10T adder consume less power, delay and PDP then other conventional and GDI adder. Average power waveform is shown in Fig.5.and in Fig.6. We analyze the behaviour of Sum and Carrey output with different supply voltage by using parametric analysis. Layout diagram of Proposed 10T adder is shown in Fig.7. it is constructed in Microwind DSCH.3.1.

Table II. Comparison of Various Adders with Proposed Adder

Parameters	Average Power(us)	Delay(ns)	PDP(fs)
28T	43.6	3.155	137.55
SERF	8.34	2.548	21.250
GDI	7.26	2.136	15.507
Proposed 11T	3.21	.03929	0.1261
8 Bit full Adder from 11T	42.23	6.028	254.56
16 Bit full Adder from 11T	86.83	2.024	175.39
Proposed 10T XOR Adder	4.59	1.241	5.696

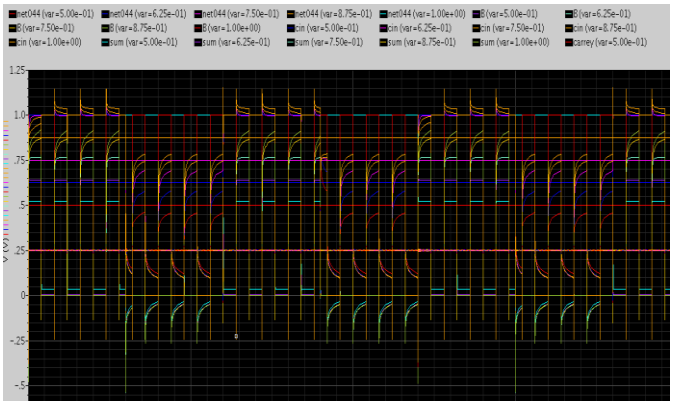

Fig.6. Parametric Analysis of Proposed 10T XOR Adder

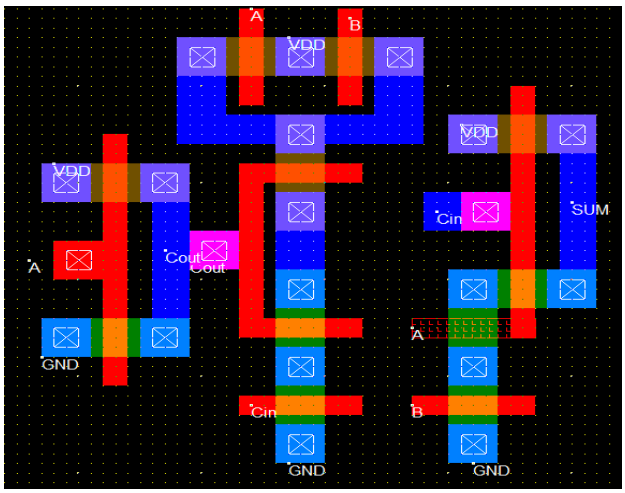

Fig.7 Layout Diagram of Proposed 10T Adder

5. CONCLUSION

The primary goal of this research work has been to present a new circuit technique to improve the swing level of GDI gate along with power efficient results in digital circuit design. The basic gates like two-input AND, OR and XOR gates are designed using conventional standard CMOS technique, other parallel techniques such as PTL, TG and existing GDI technique. The GDI technique is emerging as a strong alternative of CMOS for digital circuit design but is suffers from low threshold drop problem. Although this problem can be overcome by using buffer restoration circuits but this solution brings improvement in power and delay.

6. REFERENCES

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