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Test Scheduling of Stacked 3D SoCs with Thermal Aware Considerations

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ABSTRACT
Today's electronic designs have become prone to errors and defects due to the ever increasing complexity and compactions. This has resulted into imparting of much more importance to VLSI testing. Testing is mandatory and has to be performed on each manufactured product. Low cost and good defect coverage are the basic goals of testing, which are again determined by fault models, test volume and time. Time depends on how the tests are scheduled. Test scheduling has therefore become an important area of research. The work here is devoted to test scheduling of 3D SoCs taking into account the severe challenge it faces for its adoption i.e. the thermal management problem. 3D technology fulfils the demand of faster and compact design but there is a sharp rise in power density in such arrangement. Due to vertical stacking in 3D technology, there is a sharp rise in temperature especially for the layers far from heat sink. Consequently formation of hotspots may occur which may lead to device failure. Testing dissipates more power than the functional power because of the high switching activity that takes place during testing. All this requires thermal aware based test scheduling so that temperature does not rise above limits. The method presented here involves a thermal aware test scheduling for a 3D Soc built up using floorplan of benchmark circuit d695 and few other examples. The modeling of 3D structure is done using resistors and explores conductance mode of heat transfer. The method has been compared with sequential test scheduling since no other work on similar lines is available to the best of knowledge of authors. The method shows a marked reduction in temperature rise and consequent elimination of hotspot formation.

General Terms
Cores, floorplan, scheduling.

Keywords
Thermal awareness, hotspots, 3D SoCs.

1. INTRODUCTION
In VLSI testing, there are many aspects like generation, scheduling and application. The test requirements or the need to perform a test are many and absolutely necessary. Each manufactured product needs to undergo testing for its correct function. This warrants a test to be cheap, good and fast. Cheap means it has to be economical, as testing is cutting into the finances of manufacturing a chip or IC. It consumes as much as 50% cost of the chip. Good test means it should have a high defect coverage and fast of course, that is time consumption should be least as possible. Test scheduling refers to application of test vectors in a manner or sequence which reduces time as well as fulfills certain constraints which may be hardware related or conditions like temperature rise , voltage or frequency requirements. The test scheduling of SOCs which is the integration of a complete system onto a single IC has been taken up in this paper . Multiple ICs are integrated on a single IC which can be a CPU, a PCI , SRAM, DSP or any other as per the application, hence called a System on chip. When these functional blocks are stacked vertically they are called 3D SoCs. The advantages of system chips are many, like they can be used in complex applications, power dissipation is less in such systems, performance is very good, design time is very short and also have small volume and weight. At the same time they are characterized by a very large transistor count on a single IC , mixed technology on the same IC , have multiple clock frequencies and also the testing strategies can be different.

The challenges faced in SoC testing are many out of which power consumption during test is a main issue. The switching activity which takes place in a circuit under test are very fast and due to this the average power consumption is 3 to 10 times higher than the functional power. It is more in scan chain architectures due to generation of a large number of scan register shift-in and shift-out operations . This increases the overall chip temperature and also creates spots of localised heating called hotspots. Hotspots can cause permanent damage to silicon, high cooling costs and reliability failure. The heat has to be removed from the surface of the microprocessor die at the same rate as generation and cooling solutions have become expensive. A remarkable work in this matter has been reported in [1,2] . The problems become more aggravated in 3D SoCs.

1.1 Brief Background
The research in SoC testing can be roughly divided into the following heads: TAM optimization ,test scheduling and a standard has also been developed called IEEE P1500. A lot of work has been done under the head of test scheduling which deals with the proper application of test vectors to the circuit under test so that the testing time is minimised. Yao, Saluja and Ramanathan have provided a collection of good work on test scheduling [3]. Other noteworthy work done under this head comprises [4] the mixed integer linear programming by K. Chakraborty in ITC 2001. In VTS'03, scheduling based on simulated annealing was presented by W. Zou, Reddy and others [5] Heuristic algorithm (k-tuples) and Multi-TAM problems by S. Koranne and V. Iyengar in IEEE TCAD 2002 [6]. IEEE P 1500 standard has been reported by F. Dasilva , Y. Zorian et. al in [7]The origins of 3D dates back to 80's when James Early of Bell laboratories in [8] discussed 3D stacking of electronics and predicted that heat removal from such an integration would be the main concern. Research was also carried out by IBM, NEC, Siemens and Fraunhofer in 1990's. There has been an enormous advancement in

technology over the past decades resulting in improved performance and productivity. 3D integration is considered as a key player in technology improvement in the years to come. The transformation to 3D offers many advantages over 2D including reduced interconnect lengths, better performance and heterogeneous system integration. Many difficulties are also faced in the adoption of 3D, the major being testing issues, thermal constraints and the EDA tools. Test scheduling is one of the major area to be considered in 3D.The most important challenge for 3D includes the thermal management. A 3D circuit will have multiple layers of devices and high density of interconnects, consequently several heat generating surfaces or sources. Excessive temperature gradients can occur which can cause permanent damage and cause major setback for implementation of this technology.

Muhannad S. Bakir et al. [9] discussed many unknowns of 3D viz. How to cool? How to deliver power? How to package? Types of intrastratal interconnects, how to assemble? Bond and many more issues. Thermal analysis of vertically integrated circuits was presented for the first time by Michael Kleiner et al [10] in 1995. Test issues also assume importance in these circuits. Testing generates heat which is to be dissipated at a rate equal or faster than the heat generation. If the heat is not removed, permanent damage to the chip may be caused. The other problems of testing are encountered here also, mainly the test access, testing time and combined with the thermal problem the issue gets aggravated. Through Silicon Vias or TSVs are important components of these circuits providing power, clock signals and test access. Issues related to TSVs are also to be addressed. They have to be tested for defects and problems arising due to thermal effects. Test time minimization problems are discussed by Z. He, Z. Peng et al in [11] for 2D circuits. Very recent works are done by Millican and Saluja [12,13] in 2015 in 3D test scheduling.

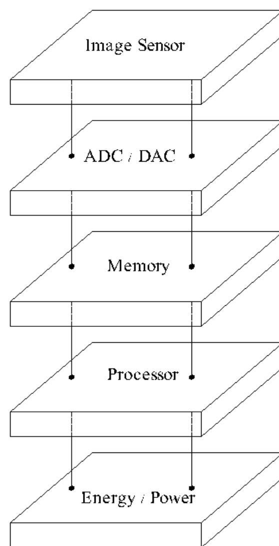

Fig 1: A 3D SoC comprising different components stacked vertically

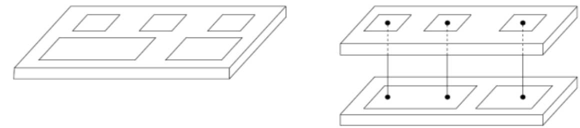

Fig 2: A 2D SoC and a vertically stacked 3D SoC

The research here is devoted to test scheduling of 3D SoCs which is an emerging technology that forms vertically stacked integrated systems. The difference with previous works is that the thermal aspects are also being covered, implies that the temperature rise of various cores which constitute the SoC is also taken into account. Temperature affects the performance, reliability and life of a chip hence it is an important aspect which requires attention right from the design, to scheduling and testing. This way, the avoidance to chip damage can be done by preventing Hotspot formation. Various materials, technologies and functional components can be stacked together as shown in the Figure1. It shows that the stack can consist of memory, processor, ADC/DAC sensors etc. stacked vertically. The Figure 2 also shows a 2D SoC which consist of many ICs . If the same are split in two and stacked vertically, we get a 3D SoC. For looking into the heat/thermal problem, we take a look at the analysis available in the literature [14,15].

1.2 Package Thermal Resistance Model

The relation between die temperature rise ΔT_{die} and P is given by [14]

$$\Delta T_{die} = (T_{die} - T_{amb}) = P.\, R_{\Theta} \qquad (1)$$

Where P is the power dissipation and R_{Θ} is the effective thermal resistance from the Si devices to the heat sink and mostly due to package material. It can be expressed as

$$R_{\Theta} = \frac{R_n}{A} \qquad (2)$$

$R_n = \left(\frac{tsi}{Ksi}\right) + \left(\frac{tpkg}{Kpkg}\right)$; where Si values are for silicon and pkg values are for package, thickness and conductivity represented by t and K.

Based on this an idea of the temperature of the die can be taken. Value of R_n available from published data is 4.75° C/ W-$cm^{2.}$. The value of power dissipation has been obtained from data by ITRS[16]. Table 1 show the temperature rise when area is changed for two cases for same power dissipation. As Area is reduced there is a sharp rise in die temperature. Approximately for the same power dissipation, increase in temperature is about 25% more.

Table 1. Relation between Power and Temperature Rise for different die sizes

P(W)	Temperature ° C 3 mm^2 die	Temperature ° C 4mm^2 die
100	158	118.75
80	126	95
75	118.75	89
70	110.83	83.12
60	95	71.25

The above data refer to the 2D circuits. The problem becomes more acute for 3D circuits. In [17] full –chip temperature calculation has been discussed. The devices in the substrate form the main source of heat generation. The interconnects also get heated up and contribute towards heat generation. Operating temperature of a VLSI chip can be calculated from

$$T_{chip} = T_a + R_n P/A \qquad (3)$$

Where T_{chip} is the average chip (silicon junction) temperature, T_a is the ambient temperature = 25ºC, P is the total power consumption in W. This is consistent with (1).

1.3 Analytical Die Temperature Model

The temperature rise of the j_{th} active layer in an n-layer 3D chip can be expressed as [14]

$$\Delta T_j = \sum_{i=1}^{j} [R_i (\sum_{k=i}^{n} \frac{P_k}{A})] \qquad (4)$$

Where n is total number of active layers;
R_i is thermal resistance between i^{th} and $(i-1)^{th}$ layers;
P_k is power dissipation in k^{th} layer.

Assuming identical power distribution between each layer and identical thermal resistances (R) between layers, the temperature rise of uppermost (n^{th}) layer in an n-layer 3D chip can be expressed as

$$\Delta T_n = \left(\frac{P}{A}\right)\left[\frac{R}{2}n^2 + \left(R_1 - \frac{R}{2}\right)n\right] \qquad (5)$$

R_1 is mostly due to package thermal resistance between first layer and heat sink. The models available so far relates to the temperature of the complete stack or die i.e. they take the temperature of a complete die as same. Practically however this is not the case as different cores dissipate different amount of heat or power. Our work is based on finding the temperature of individual cores which constitute a single stack. We have built up a 3D-SoC by stacking several layers of SoC d695[18]. The d695 consists of 10 cores. The test scheduling has been done based on temperature. Due to a large amount of heat produced, there has to be some means of heat removal. It has been highlighted in [9] by Muhannad S. Bakir, Calvn King et al. and [19] by B. Goplen et.al. This will form the basis of our future course of work on cooling methods.

2. MODELING OF 3 D STRUCTURE

It is essential to model the vertical stacks before analysis is carried out. Many models have been proposed [13,20] . An equivalent RC circuit can be used to model the 3D structure. For an integrated circuit at the die level, conduction is the main mode which determines heat transfer and consequently the temperature rise. For simplification purpose we can prepare a model of resistors for the circuit we are considering. Each block on the die will have a resistor to its neighbors [20,21].

This will include neighbors on left, right up and down. For a three dimensional case there will be six neighbors or cells which will be considered as shown in Figure 3.In this paper thermal aware test scheduling of 3D SoCs has been considered. The power dissipated by blocks under test needs to be modeled. The power profile captures the power dissipation of a block over time when applying a sequence of test vectors to inputs and/or pseudo inputs of the blocks. The temperature rise of the chip will be considered while scheduling so that the rise is not above limits leading to hotspot formation.

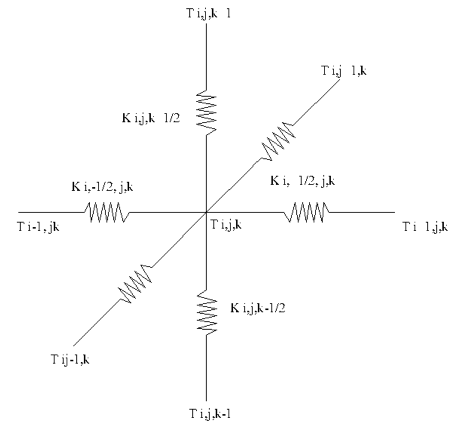

Fig 3: Modeling a 3D structure using resistors

3. PROBLEM FORMULATION

Given a stack of n layers 1, 2... n and each ith layer having k_i cores where k may have same or different values for each core in a given floorplan. The maximum power constraint P_{max} and temperature constraint T_{max} is given. It is required to find an efficient test sequence such that temperature rise should not exceed the permissible limits and there should be no hotspot formation. Here the permissible limits for temperature may be set and the power limits may be specified for different cases.

3.1. Heat Flows

There are three modes of heat transfer- conduction, convection and radiation. Conduction is the main mode of heat transfer in solids and this is the mode considered in this work. Heat flow by conduction is governed by Fourier law [20].

$$q = -k\frac{dt}{dx} \qquad (6)$$

This is the one-dimensional heat equation q is the heat flux in W/m^2, k is the thermal conductivity of the material in (W/m.K). This equation says that heat flux q, (the flow of heat per unit area per unit time) at a point in a medium is directly proportional to temperature gradient at that point. The minus sign indicates that heat flows in the direction of decreasing temperature. If q is written as Q/A where Q is the heat transfer rate, A is the conducting area, and L is the length of material, now equation becomes:

$$Q = kA\frac{(T1 - T2)}{L} \qquad (7)$$

i.e temperature drop divided by heat transfer rate, we can write an equivalent expression as

$$R_{th} = \frac{(T_1 - T_2)}{Q} = \frac{1}{k}.\frac{L}{A} \qquad (8)$$

Based on this duality between electrical and thermal quantities has been derived [21] viz. Q, the heat transfer rate or power in W is dual of current in A, temperature difference (K) corresponds to voltage difference (V), thermal resistance R_{th}

in K/W is dual of R, electrical resistance in ohms, C_{th} the thermal capacitance in J/K is analogous to C, electrical capacitance in F. On similar concepts, laws of electrical circuits can be applied to thermal circuits as well. One of the well known laws of electrical is the principle of superposition which states that total electrical current through any branch in a circuit is the algebraic sum of all the currents through that branch. Since duality between electric and thermal circuits has been established , this principle can be applied to thermal circuits as well taking heat flow and temperature rise.

4. TEST SCHEDULING

We consider test scheduling of a 3D stack built by floorplans shown in Figure 4 where stacks can be built using different floorplans.

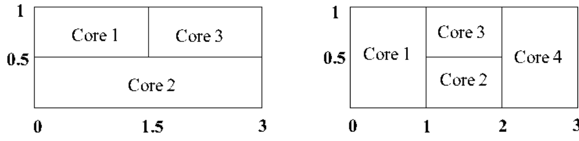

Fig 4: Floorplans of different layers

The cores on the floorplan will have neighbors on all sides. Each core can have six neighbors or even more. The effect of thermal interface material between the two stacks, heat spreader and heat sink has been taken into account. When a core is tested, heat is generated which spreads to all its neighbors both vertically and horizontally. The test scheduling approach used in this paper is based on the calculation of total heat produced during a particular testing time. Each vertical stack consists of a SoC which in turn consists of many neighboring blocks. For three dimensional case consider a cell (i,j,k) with side length Δx_i, Δy_j ,Δz_k . There will be 6 adjacent neighbors for each cell in 3D case or more depending on overlap. If we consider the diagram of Figure 3 [20], the center cell has coordinates $T_{i,j,k}$ and the right one has $T_{i+1,j,k}$ considered in x –directions i.e the variation only in the x-coordinate will occur. There will be resistances between them with conductance defined as K. The value of conductance K will be six, in all the six directions in 3D case. By this method we are considering the vertical and lateral heat conduction both. Figure 4 is a set of simple floorplans for understanding of heat spread methodology with the explanation as follows. The one on the left (a) has three cores and (b) has 4 cores. Where they are stacked one over the other, there will be overlapping between the cores. The width is 3mm and height is 1 mm (3x1mm). For a 2-stack structure, (a) forms the lower layer and (b) will be the upper layer. Core 1 of lower layer will have cores 1, 2, 4 of (b) over it . Core 2 of (a) will have cores 1, 3, 4 of of (b) over it. Core 3 of (a) will have 3 and 4 of (b) over it. So the heat transfer will take place as explained below:

If core 1 of lower layer is tested, heat transfer will take place to (i) core 1, 2 4 of (b) vertically (ii) core2 and 3 of (a) laterally. The amount of heat transfer will vary and is based on equations (9) to (14).The heat flow $Q_{i,j,k+1/2}$ (W) from one cell (i,j,k) to cell above (i,j,k+1) is given by conductance between the two cells multiplied by the temperature difference between the two cells. Similarly heat flow from cell (i,j,k) to other six cells in its proximity are given by following equations [20].

$$Q_{i,j,k+\frac{1}{2}} = K_{i,j,k+\frac{1}{2}}(T_{i,j,k} - T_{i,j,k+1})(W) \quad (9)$$

$$Q_{i,j,k-\frac{1}{2}} = K_{i,j,k-\frac{1}{2}}(T_{i,j,k} - T_{i,j,k-1})(W) \quad (10)$$

$$Q_{i-\frac{1}{2},j,k} = K_{i-\frac{1}{2},j,k}(T_{i,j,k} - T_{i-1,j,k})(W) \quad (11)$$

$$Q_{i+\frac{1}{2},j,k} = K_{i+\frac{1}{2},j,k}(T_{i,j,k} - T_{i+1,j,k})(W) \quad (12)$$

$$Q_{i,j+\frac{1}{2},k} = K_{i,j+\frac{1}{2},k}(T_{i,j,k} - T_{i,j+1,k})(W) \quad (13)$$

$$Q_{i,j-\frac{1}{2},k} = K_{i,j-\frac{1}{2},k}(T_{i,j,k} - T_{i,j-1,k})(W) \quad (14)$$

$K_{i,j,k+1/2}$ is the conductance between the two cells (i,j,k) and (i,j,k+1) in W/K. The value of conductance is calculated as

$$K_{i,j,k+\frac{1}{2}} = \frac{\Delta x_i \Delta y_j}{\frac{\Delta z_k}{2\lambda_{i,j,k}} + \frac{\Delta z_{k+1}}{2\lambda_{i,j,k+1}}} \quad (15)$$

The first term in denominator is the thermal resistance in z direction for half of the cell (i,j,k) and the second term is the thermal resistance for half of the cell (i,j,k+1). $\lambda_{i,j,k}$ is the thermal conductivity in W/mK .

Similarly there are five other thermal conductances associated with each cell [20] which can be similarly computed. The conductances between two cells (i,j,k) and (i,j,k+1) is shown in Figure 3. The heat flow is calculated based on electrical equivalents of the thermal circuits and are based on [20]. The changes for the boundary cells can also be suitably done. Though the heat spread cannot be restricted to 6 neighbors alone, they will again spread to their adjacent neighbors and some cooling will also be there but this has been assumed negligible here. The total heat flow to cell (i,j,k) from six neighboring cells can be calculated. As a core is tested it generates heat. The heat flow to its neighboring core can be calculated using the equations mentioned above. The heat flow results in rise or fall of temperature. The new temperature is given by $T_{new} = T_{old} + \Delta T$. Principle of superposition has been applied for the purpose of calculating the temperatures of cores.

The testing of cores results in rise of temperature. First a core is tested and its effect on all neighboring cores in terms of temperature rise is observed. Next the coolest core is selected for testing. It is tested and again heat transfer and temperature rise is noted for each core. The new temperature will be the sum of old and the incremental temperatures. The least heated core is selected for testing. Values of temperatures are updated. Another temperature rise is observed with core testing being done sequentially i.e. according to the numbering viz. core 1 ,2 ,3 . . . n of one layer, then 1,2,3... m of the second layer and so on and temperature rise is observed with each core. Initially the process seems simple with the reasoning that cores situated away will be cooler and get selected but as the heat spreads, the temperature also rises and it is not simple to predict the next core for scheduling [22].

4.1. Algorithm

Let N be the no. of Floorplans
Let x_i (i = 1 to N) represents no. of cores in each floorplan
Total cores = Tot_cores = $x_1+x_2+x_3+.....+x_N$.
for all i such that 1<= i <= N do

Input no. of cores in each floorplan
End for

for all i such that 1<= i <= N do
    for all j such that 1<=j<= x_i do
    assign value to each core as $y_{i,j}$
    end for
end for

for all i such that 1<= i <= N do
    for all j such that 1<=j<= x_i do
    calculate and store conductance of the core,
    assign x_coordinates, y_coordinates,
    width to all cores.
    set parameter values of each cores

    # Test_flag = 0; Core_power = 0;
    Core_Temp = 318K etc#

    end for
end for

Set Core_Remaining = Tot_Cores;
Select Core $y_{1,1}$ for testing;
Set Test_flag.Core $y_{1,1}$ = 1;
Test the core for specified time;
Core_Remaining - - ;
Calculate and update the Core__Temp of adjacent cores

For all k such that 1<= k <= Core_Remaining;

#Select core with min. Temp and with its Test_flag = 0 as
Core_to_be_tested#

Core_to_be_tested = Core $y_{1,1}$;

for all i such that 1<= i <= N do
    for all j such that 1<=j<= x_i do
        If Temp.Core $y_{i,j}$ < Core_to_be_tested &
        Test_flag.Core $y_{i,j}$ = 0;
            Then Core_to_be_tested = Core $y_{i,j}$;
    end for
end for

Set Test_flag. Core_to_be_tested = 1;
Test the core for specified time;
Core_Remaining - - ;
Calculate and update the Core__Temp of adjacent cores;

End For.

4.2. Implementation

The algorithm was implemented for 2, 3, 4 layer standard benchmark circuits viz. d695, d281, f2126 and 2f2126 taken from ITC'02 benchmarks [23]. The circuits that are utilized to build the stacks are d695 having 10 cores, d281 having 8 cores, f2126 with 4 cores and 2f2126 with 8 cores. Two layered, three layered and four layered stacks have been built from these circuits. The benchmark information obtained for these comprise the number of test vectors, scan chain length from which test time can be calculated. The power profile information is obtained from newly released benchmark circuits by Millican and Saluja [13]. The floorplan of various benchmarks are given as Figure 5a and 5b below.

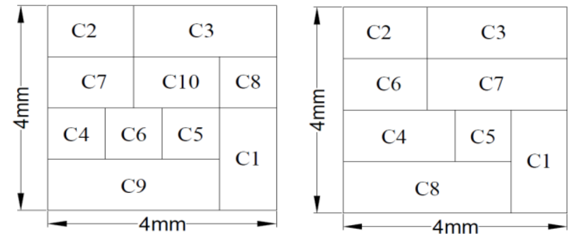

Fig 5 a: D695 and D281 benchmark circuits respectively

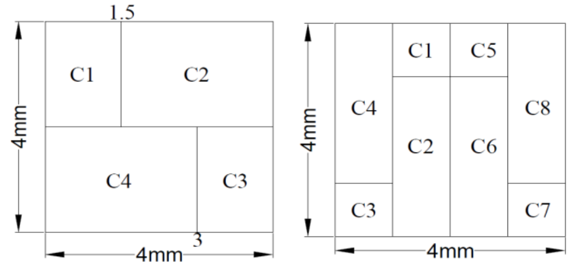

Fig 5 b: f2126 and 2f2126 benchmark circuits respectively

Testing has been scheduled sequentially also to compare temperature rise since no similar work is available for comparison.

Different combinations of the standard benchmark circuits were used to build up 2,3,4 layer stack. The input to the algorithm is the initial value of heat generated and the output is the sequence of cores for testing and the final temperature. Initial temperature is taken as 318 Kelvin. Details of each layer are read viz. x-coordinate, y- coordinate, width and height of each core in it. Conductance value is calculated as per eq. (15) for each core both in horizontal and vertical direction to account for the heat spread. One of the cores is selected for scheduling. Heat generation is calculated with initial fed power trace file which contains power for each core which in turn is based on the test length of the respective core and temperature rise is observed. This is for stacks built up using standard benchmark circuits. During testing, the heat will spread to its neighbours both horizontally and vertically. Temperature is updated for all. Next the core selected is the one with least temperature rise. It is scheduled next. Again heat spread due to this is calculated. The temperature values are updated by adding up the initial temperature and incremental temperatures. It is repeated till all cores are scheduled and thereafter tested. In this paper we will compare the results i.e. final temperature of all cores as obtained after scheduled testing as per the proposed algorithm with that of sequential testing where all cores are selected serially and tested thereafter.

5. RESULTS

Temperature rise observed when algorithm is implemented is recorded along with the sequence of testing of the core. The graphs show the final temperature of individual cores after scheduled and sequential testing of 2, 3, and 4 layered floorplan of benchmark circuits.

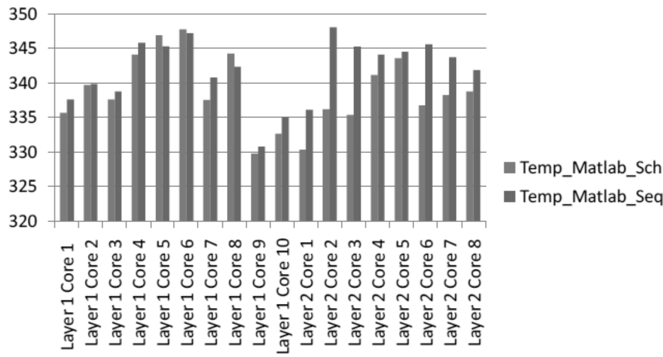

Fig 6: 2 Stack Scheduling vs sequential results

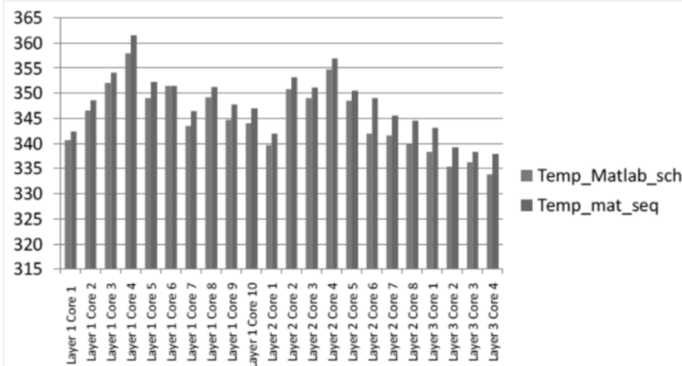

Fig 7: 3 Stack Scheduling vs Sequential results

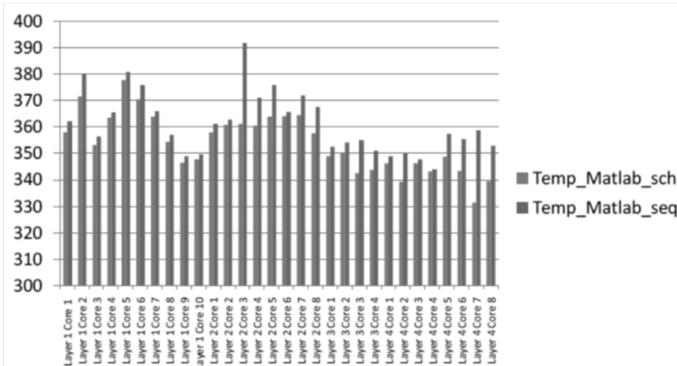

Fig 8: 4 Stack Scheduling vs Sequential results

The results after testing of cores in 2, 3,4 stacked structures are depicted in Fig 6,7,8 where their results are compared w.r.t. the temperatures after sequential testing of the cores of the same structure. In all graphs, the first histogram represents result of the core after scheduled testing and the second histogram represents temperature of the core after sequential testing on Matlab using the algorithm. Here 2 stack structure is the combination of d695 (layer 1) and d281(layer 2) benchmark circuits, 3 stack structure comprises of d695, d281 and f2126 (layer 3) circuits whereas in the 4 stacked structure, the fourth circuit is 2f2126 (layer 4) and the remaining three circuits are the same as that in 3 stacked structure. It is quite explicit that the final temperature rise obtained in case of scheduled testing is comparatively lower than that obtained in sequential testing. The graphs represent the temperature behavior of individual core. In the table 2 given below, the mean temperature after scheduled and sequential testing of each floorplan in 2,3,4 stacked structure clearly brings out the overall temperature difference of the circuit as a whole. It is quite explicit that there is difference in the range of 3-8 K in the mean temperature of 2, 3, 4 stacked circuits which is indicative of the fact that the propsed scheduling scheme of testing cores is superior to that of sequential testing of circuits.

Table 2. Mean Temp. of each stack after Scheduled and Sequential Testing

Mean Temp.	2 stack Circuit		3 Stack Circuit		4 Stack Circuit	
	Sch.	Seq.	Sch.	Seq.	Sch.	Seq.
D 695	339.6	340.3	347.9	350.3	360.6	364.2
D 281	337.5	343.6	345.8	349.1	361.2	370.8
F2126	-	-	335.9	339.6	346.2	353.2
2F2126	-	-	-	-	342.2	351.85

6. VALIDATION OF RESULTS

Validation of results needs to be done to access the suitability of the proposed method of scheduling. It was performed using the Hotspot tool [21] which is an accurate and fast model based on an equivalent circuit of thermal resistances and capacitances that correspond to micro architecture blocks and essential aspects of the thermal package. Validation of this model has been performed using finite element simulation. The chips today are typically packaged with the die placed on a spreader plate, made of aluminum, copper, or some other highly conductive material, which is in turn placed against a heat sink of aluminum or copper. This is the configuration modeled by HotSpot. We have prepared our stacks similarly, consisting of stacks with interface material in between, heat spreader and heat sink.

HotSpot dynamically generates the RC circuit when provided with an input consisting of the blocks' layout and their areas. It is also provided with a power input values (these are the values for the current sources) over any time step and the present temperature of each block. It then generates the temperatures at the center of each block [21]. We provided Hotspot with the inputs details of our stacks, viz. floorplan, power trace files, area and initial temperatures. The final temperatures obtained using this tool are shown in Fig. 9, 10 and 11 which show very little difference in temperatures (ranging in +/- 2 K) obtained with our algorithm and Hotspot. The results are in fair agreement with the results of Hotspot which explicitly indicate the high degree of accuracy of the algorithm proposed herein.

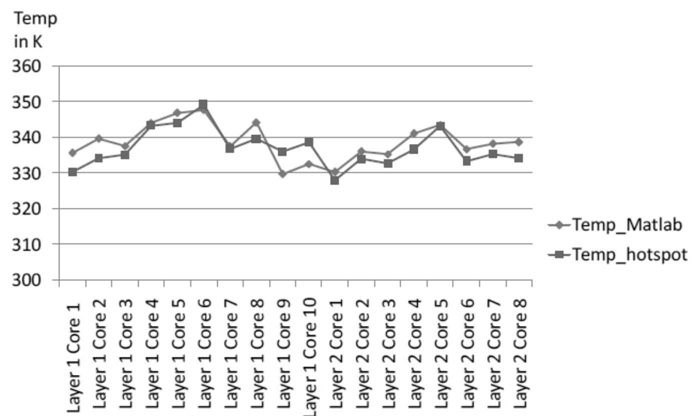

Fig 9: Validation results of 2 stacked structure

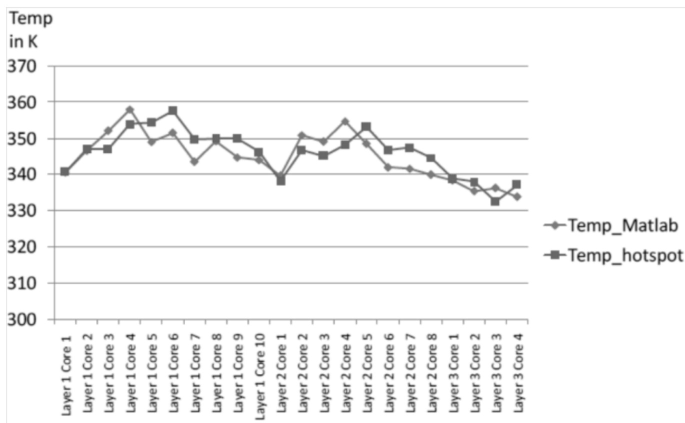

Fig 10: Validation results of 3 stacked structure

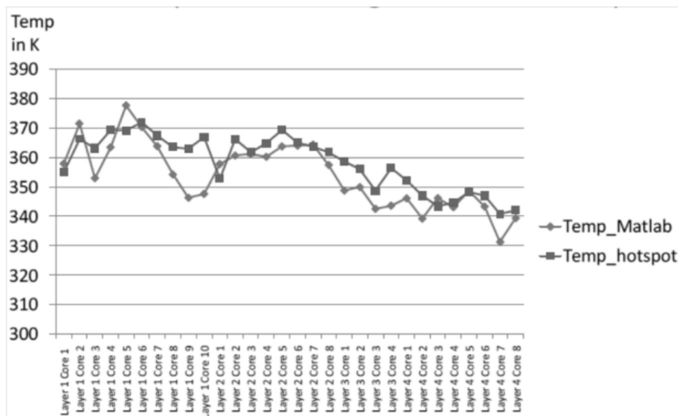

Fig 11: Validation results of 4 stacked structure

7. CONCLUSION AND FUTURE WORK

In this paper we have proposed an algorithm for scheduling of cores in multiple stacked structures which keeps the temperature rise to low levels during testing. We have compared the results which are in the form of final temperature of cores after testing with the temperature values received after sequential testing of the cores and have found the results to be convincing. We further propose to test the cores in these multiple stacked structures in parallel groups so as to minimize the number of schedules of testing, keeping into mind the temperature rise to be contained to minimum limits. It is also proposed to further refine the test scheduling by way of partitioning the test schedules so as to minimize the wait time of cores with less test length which fall for testing with cores of comparatively very high test lengths so as to limit the time taken in complete testing of the circuit. These proposed methodologies will assist in optimal test scheduling of cores in multiple stacked layers thereby eliminating delayed and lengthy test times and will obviate probability of cores getting damaged during testing on account of extremities of temperature.

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