Power and Area Efficient Design of 6T Multiplexer using Transmission Gate Logic

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ABSTRACT

The main issue in designing of VLSI circuits is power consumption and area requirement In this paper Multiplexer circuit is proposed with the help of transmission gate logic using 6 transistors. Different design methodologies are used for designing of multiplexer layout. Multiplexer is essential circuit for different field of network and communication. Multiplexer requires less number of transistors using transmission gate logic. The main concerned of this paper is to reduce area, power consumption and complexity of Multiplexer using different design methodologies.

Keywords- CMOS technology, Layout, Microwind tool, Pass Transistor, Transmission gate, Transistor

1. INTRODUCTION

Very large scale integration is the process of creating integrated circuit by combining thousands of transistors in to a single chip. Very-large-scale integration (VLSI) is the design of extremely small, complex circuit using semiconductor materials [1]. VLSI is characterized by the exponential growth of the number of transistor per chip [2]. Gordon Moore noted that the number of transistor per chip wills double every 18 to 24 month [3].VLSI circuit technology is rapid growing technology for the wide range of innovative devices and system that have changed the world today. Recently, designing of low power consumption circuit is the main concern of the research. Modern digital circuits consist of logic gates implemented in the complementary metal oxide semiconductor (CMOS) technology [4]. MOS technology is considered one of the very important and promising technologies in the VLSI design process. The circuit designs are realized based on PMOS, NMOS, CMOS and BiCMOS logic. There are various methods that are widely used for reducing the power consumption in circuits by reducing switching, supply voltage, load capacitances and the used devices. These methods are used to minimize the power consumption and also reduce the no of transistors. The alternative method for reducing power consumption is by the implementation of the pass transistor logic [1]. Low power leads to smaller power supplies and less expensive batteries [5]. Low power is not only needed for portable application but also to reduce the power of the high performance system [5].

A Multiplexer is the basic combinational circuit which has application in many field of engineering such as communication system, processor buses, network switches and digital signal processing stages incorporating resource sharing [5]. Multiplexer designed for biomedical applications are low power consumption low on resistance and faithful reproduction of input at the output [6]. Multiplexers play the important role in the functionalities of FPGAs, so to design a multiplexer with PTL will generate the concept of designing low power consumption circuits for FPGAs [1].

There are different ways to design combinational circuit with the help of. One of them is transmission gate logic .When an NMOS or PMOS is used alone as an imperfect switch, the logic is called pass transistor. By combining an NMOS and a PMOS transistor in parallel transmission logic is formed. In transmission Gate logic PMOS is used to provide strong '1' and NMOS is used to provide strong '0'.

Transmission gate logic circuit is shown in fig. 1.

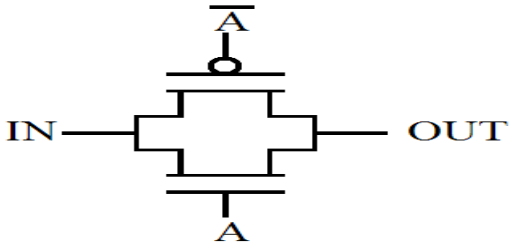

Fig. 1 Transmission Gate Logic

2. MULTIPLEXER

Multiplexer with transmission gate logic requires less number of transistor comparison to the other CMOS logic design for combinational circuit. The proposed Multiplexer requires only 6 transistors. Transmission gates produce a non restoring multiplexer [6].

The reason for adopting the apparent complexity of the transmission gate, rather than using a simple n switch or p switch in most CMOS applications, is to eliminate the undesirable threshold voltage effects which give rise to loss of logic level in pass transistors [7]. A 2 to 1 Multiplexer is designed with the help of transmission gate is shown in figure 2.

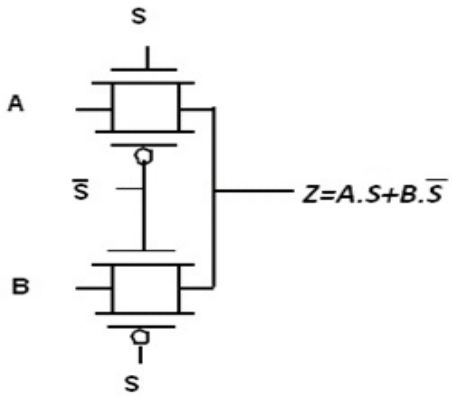

Fig .2 2 to 1 Multiplexer with Transmission Gate

The select and its complement enable exactly one of the two transmission gates at any given time.

VLSI fabrication technology is still in the process of evolution which is leading to smaller line widths and features size and to higher density of circuitry on a chip. Scaling down of the feature size generally leads to improved performance. Micro electronics technology may be characterized in terms of several figure of merit [1].

1. Minimum feature size
2. Number of Gates on one chip
3. Power dissipation
4. Maximum operating frequency
5. Die Size
6. Production Cost

Figure of merit can be improved by changing the dimension of the transistor, separation between features and by adjusting the doping level and supply voltages. The design efforts have focused on optimizing speed to realize computationally intensive real-time functions such as video compression, gaming, graphics etc. The increasing demand for low-power very large scale integration (VLSI) can be addressed at different design levels, such as the architectural, circuit, layout, and the process technology level.

At the circuit design level, considerable potential for power savings exists by means of proper choice of a logic style for implementing combinational circuits [8]. There are different types of technology advancement in the VLSI design such as 90nm, 65mn, 45 nm etc. These technologies are used to improve the performance of the circuit in terms of the power, area, delay etc. These technologies depend on the distance between source and drain.

In semiconductor design, standard cell methodology is a method of designing application specific integrated circuit (ASICs) with digital –logic features. Along with semiconductor manufacturing advances, standard cell methodology has helped designers scale ASICs from comparatively simple single-function ICs (of several thousand gates), to complex multi-million gate system-on-a-chip (SoC) devices. A Standard cell based Layout uses predesigned logic cells Known as standard cell. Gate array based design is based on predefined transistor on the silicon wafer. The designer uses predefined set of transistor from the library while designing the layout. This design is also called semicustom based design layout. Another approach of designing is the full custom based design layout. In this design, designer abandons the approach of using pretested and pre characterized cells. These designed methodologies are used in this paper for designing of the multiplexer circuit.

There are various methods that are widely used for reducing the power consumption in circuits by reducing switching, supply voltage, load capacitances and the used devices. These methods are used to minimize the power consumption and also reduce the no of transistors. With increasing demand for battery operated applications, methods for reduction of the power consumption of the memory blocks have received significant interest [9].The alternative method for reducing power consumption is by the implementation of the pass transistor logic [1].

3. MULTIPLEXER SCHEMATIC

Schematic diagram of proposed 2:1 MUX is as shown in fig.3. This circuit is designed with the help of transmission gate logic. The circuit is implemented with the help of 6 transistors, Where 3 PMOS and 3 NMOS are used. This circuit requires less number of transistor comparisons to other CMOS logic. The proposed 2 to 1 multiplexer circuit requires two transmission gates logic along with the one inverter. The gate of the one MOS in a transmission gate is connected to the selection line S and other is connected to the S'. The PMOS of inverter is connected to the 1.20 V supply and N switch is connected to the ground logic Vss. In the CMOS design inverter NMOS works as pull down network and PMOS works as pull up network.

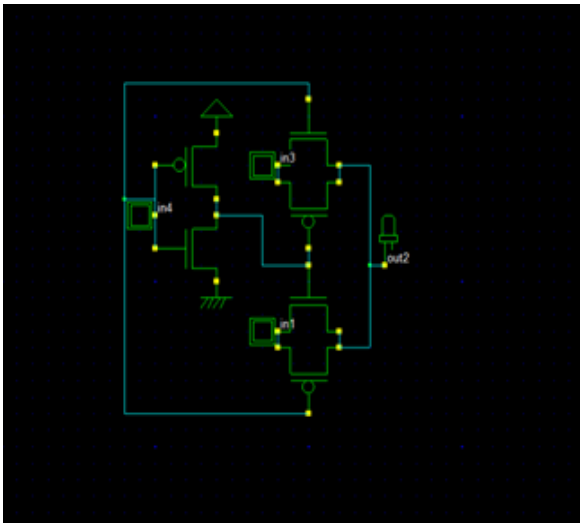

Fig.3 Schematic of 2 to 1 MUX transmission gate logic

The switch is applied at the input of the inverter. Light emitting diode is applied at the output of 2 to 1 multiplexer as shown in fig. 3. BSIM model parameters is used for analysis of layout of the 2 to 1 multiplexer.

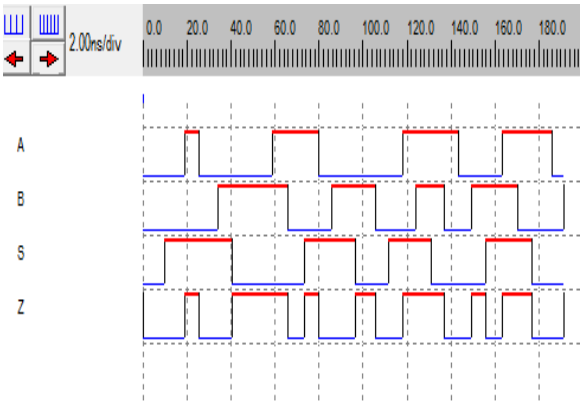

Fig 4 shows simulation result of proposed 2 to 1 MUX

Fig 4 shows the simulation result of proposed 2 to 1 multiplexer. Where S is the selection line A and B is the input of the multiplexer and Z is the output of the multiplexer. When S is logic high output follows the input A, when S is at logic low output follows the input B.

4. LAYOUT DESIGN ANALYSIS

Fig.5 shows the standard cell multiplexer layout design. Standard cell based layout is implemented using schematic of 2 to 1 multiplexer using transmission gate logic. This is the self generated layout from the microwind library. Standard cell multiplexer design is complex and consumes more power and area.

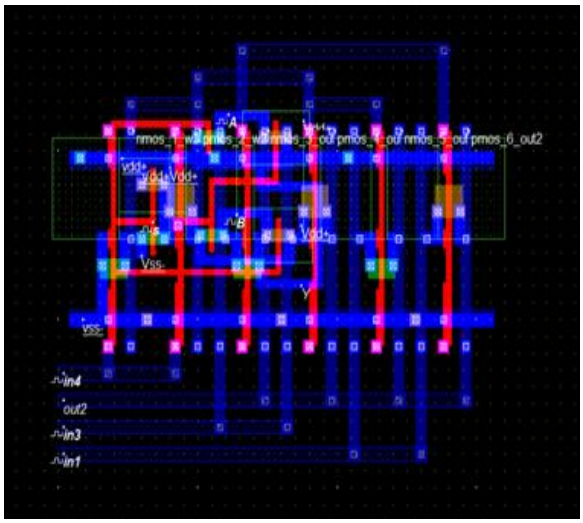

Fig. 5 Standard Cell Layout Design of 2 to 1 Multiplexer

Another layout design of the 2 to 1 multiplexer has created based on Gate array based design. It is also known as semicustom based design methodology is shown in fig. 6. This layout is based on the PMOS and NMOS selected from the library of the micro wind. The same supply of 1.2V is given to the layout but layout is less complex and consumes less power than standard cell based design requires less power consumption than standard cell based and semicustom based design layout.

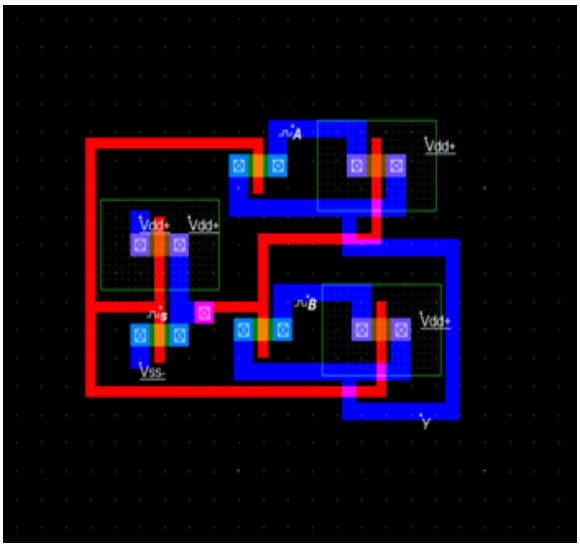

Fig. 6 Semi Custom Design of 2 to 1 Multiplexer

Fig. 7 shows the design of 2 to 1 multiplexer using full custom layout design. This circuit is designed with common well PMOS's. Full custom layout of the proposed 2 to 1 multiplexer is less complex and the main parameters of consideration are area, complexity and power of the 2 to 1 multiplexer in this paper. Table 2 shows the area and power consumption of 2 to 1 multiplexer circuit.

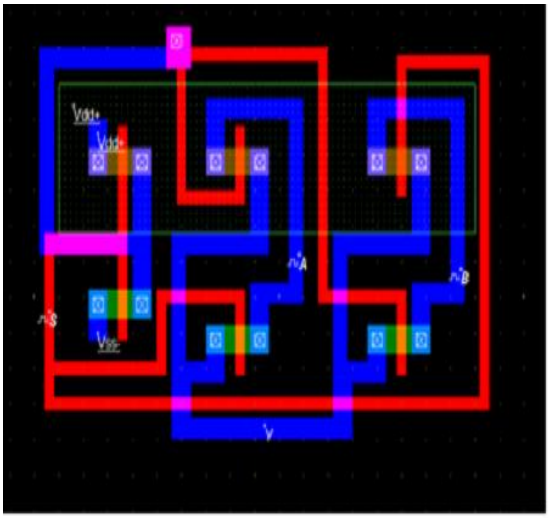

Fig. 7 Full Custom Design of 2 to 1Multiplexer

Fig.8 shows the generated simulation waveform of proposed 2 to 1 multiplexer circuit with the help of transmission gate logic. Here S is the selection line, A and IB are inputs and Z is the output. When S is low, output will follow B i.e. Z=B. When S is High, output will follow the A i.e. Z=A. In this way 2 to 1 multiplexer logic has been verified for standard based design, semi custom design and full custom design.

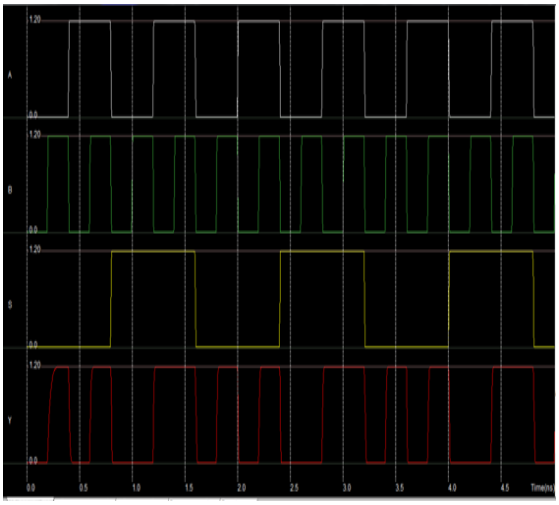

Fig. 8 Simulation Result of 2 to 1 Multiplexer

MUX Layout	Technology Used	AREA Used	POWER Consumption	Complexity
Standard Cell based Design	45nm	50.2 μm^2	0.436 µW	complex Layout
Semi-Custom Design	45nm	2.5 μm^2	0.072 µW	Lesser than standard cell based Design
Full Custom Design	45nm	14.8 μm^2	0.068 µW	Least Complex

Table 1 Area and Power consideration

Here 45nm technology is used in the designing of standard cell based layout, semi custom based layout and full custom layout of 2 to 1 multiplexer with the help of micro wind tool. The supply voltage of 1.2 V is used in the designing of standard based layout, semi custom based layout and full custom layout. Transistor width (w) = 0.200 micrometer and length L=0.100 micrometer has been used in the design.

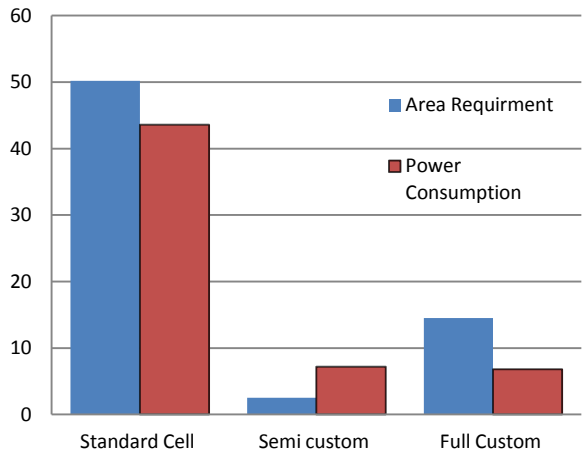

Fig.9 Area and Power consideration of different type cell

5. CONCLUSION

This analysis has proposed three different type layout design of 2 to 1 multiplexer using transmission gate. Standard cell based layout, semicustom based layout and full custom layout are developed for the 2 to 1 multiplexer. Parametric analysis of 2 to 1 multiplexer is done. Area, power and complexity of the layout are the parameters are considered for analysis methods are the parameters taken for analysis. Fig. 9shows that semi custom based layout design has 95.0% of reduction in the area compared to the standard cell based design and 83.10% of reduction in area comparison of full custom design. Full custom design has 70.5% of reduction in the area compared with the standard cell based layout .Complexity of semi custom based layout and full custom layout is lesser than standard cell based layout. The power consumption of semicustom based layout is 83.46 % lesser than standard based design and power consumption of full custom based layout is 84.40 % lesser than standard cell based layout.

6. ACKNOWLEDGEMENT

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7. REFERENCES

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