Comparative Analysis of Universal Gates using MCML and CMOS Technique

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ABSTRACT
MOS current mode logic (MCML) is an emerging logic family which is gaining attention due to its high speed of operation, robust performance and presence of mere switching noise as compared to the CMOS logic family. In this paper we have compared universal gates using MCML and conventional CMOS in terms of power and propagation delay at 16-nm Technology node. Comparative analysis shows that MCML universal gates has less power and delay as compared to conventional CMOS based universal gates at 16 nm technology. Variability analysis establishes MCML based universal gates as the most resilient and immune to various electrical parameters.

Keywords
MCML, CMOS, power and delay

1. INTRODUCTION
The on-chip integration of various analog and digital circuits requires higher speed of operation with less power consumption. The conventional CMOS technology is not capable of providing an efficient solution to these requirements. The emerging class of MOS current mode logic (MCML) is proving to be a promising technology for the current trends of technology requirements due to its higher speed of operation. MOS implementation of current mode logic (CML) is preferred over bipolar CML because of scalability of its feature size and less power consumption with

higher speed of operation [1] [2] [3]. Moreover, CMOS logic family suffers from large dynamic power dissipation at high frequencies.

Nowadays, high-speed circuits use a well-known logic style, namely the current mode logic (CML) [4]. Designing high-speed circuits puts additional constraints on the design. For instance, circuits forming the blocks of a Giga-bit communication system should be simple and consist of a minimum number of active devices. Also, PMOS devices should not be used in high-speed signal processing circuits due to the fact that PMOS devices have less charge carrier mobility which makes them have an inferior unity-gain frequency with respect to NMOS devices. At high frequencies, CML circuits operate with lower supply voltages than CMOS circuits. Thus, CML circuits are a better choice for high speed applications.

In this paper, a more general approach is taken. Two-input MOS CML elementary logic gates (AND, OR, NAND and NOR) are investigated. The 16 nm technology is used.

2. MOS CURRENT MODE LOGIC
Design and performance parameter of MCML logic are given in subsequent sections:

2.1 Power efficiency of MCML
The power consumed by an MCML gate is

$$P_{MCML} = I_{BIAS} \text{ X } V_{DD} \quad (1)$$

Where,

P_{MCML} – Power consumed by MCML gate

I_{BIAS} – Bias current

V_{DD} – Power supply

As per the above equation the power consumed by an MCML gate does not depend on the operating frequency. An MCML gate consumes constant current (and power) from the power supply network. This behavior is in contrast to the CV^2f power dissipated by conventional CMOS, where the power consumed by a static CMOS gate exhibits a linear relationship with the operating frequency. MCML is therefore more power efficient at high frequencies as compared to static CMOS. MCML based universal gates are introduced in this paper to perform power and delay analysis between MCML and CMOS.

2.2 Delay
Delay is the time required for the output to reach 50% of its final output level when the input changes to 50% of its final input level.

2.3 Low noise environment of MCML
CMOS circuits suffer from simultaneous switching noise (SSN), which accounts for a major portion of the total on-chip noise. In contrast, the constant current of MCML significantly lessens on-chip SSN.

2.4 Logic Circuits
Basic MCML gates share certain standard characteristics. Only one gate, therefore, needs to be optimized. NAND, AND, NOR and OR gates are considered in this work. These gates are based on the circuit shown in Figure 1.

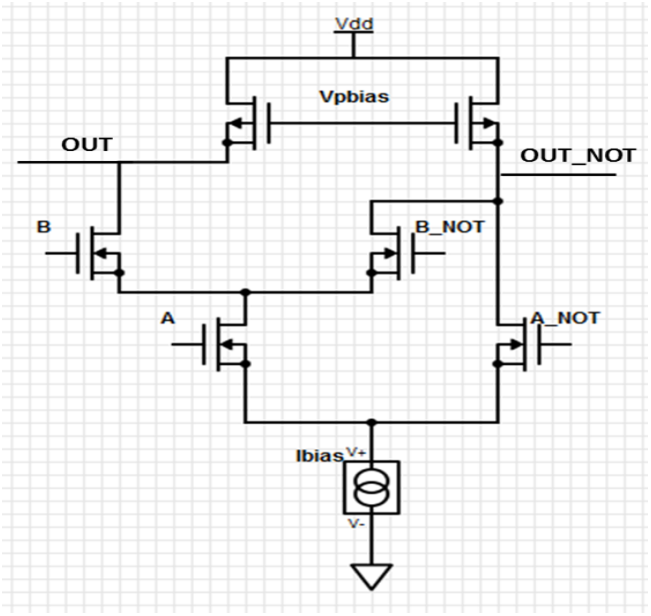

Figure 1. MCML Universal Gate[5]

3. SIMULATIONS AND RESULTS

The simulations are based on 16 nm low power technology models.

Here are the figures showing the simulation results of universal gates by both CMOS as WELL as MCML Technology.

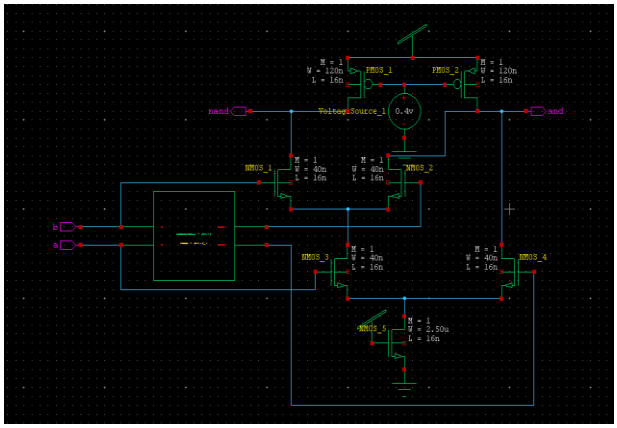

Figure 2. Schematic of AND/NAND using MCML

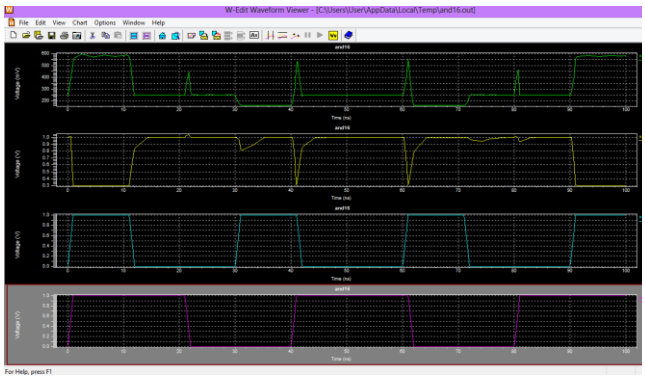

Figure 3. Waveform of AND/NAND using MCML

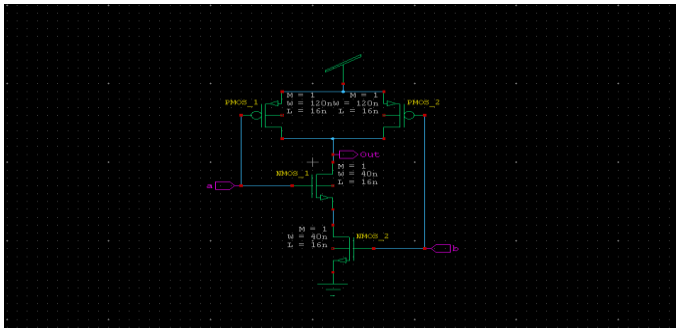

Figure 4. Schematic of NAND using CMOS

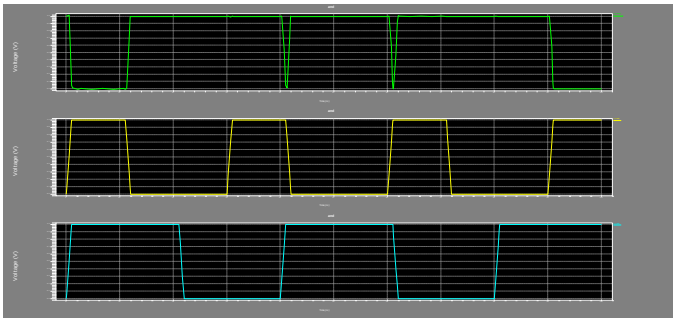

Figure 5. Waveform of NAND using CMOS

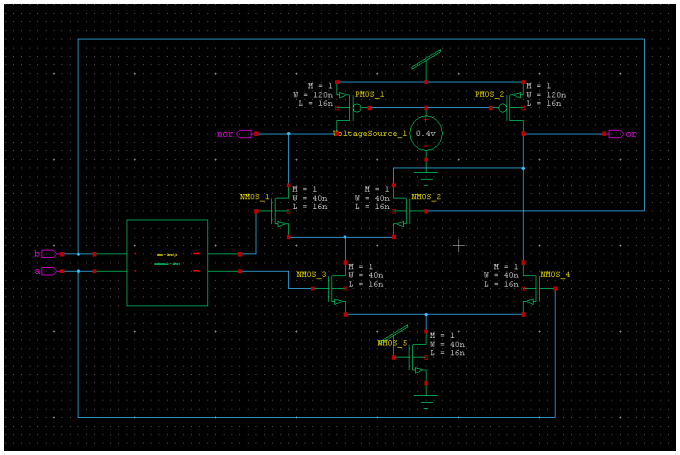

Figure 6. Schematic of OR/NOR using MCML

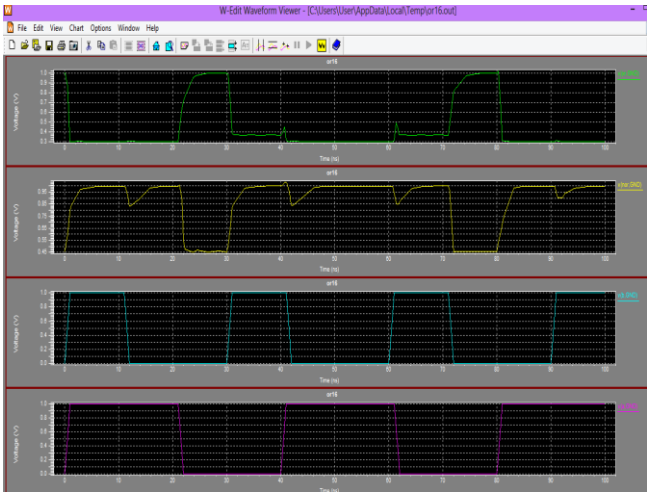

Figure 7. Waveform of OR/NOR using MCML

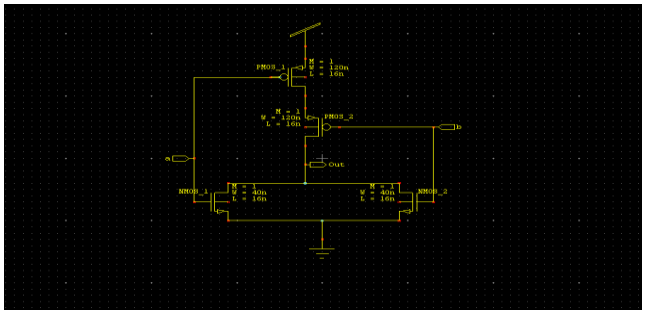

Figure 8. Schematic of NOR using CMOS

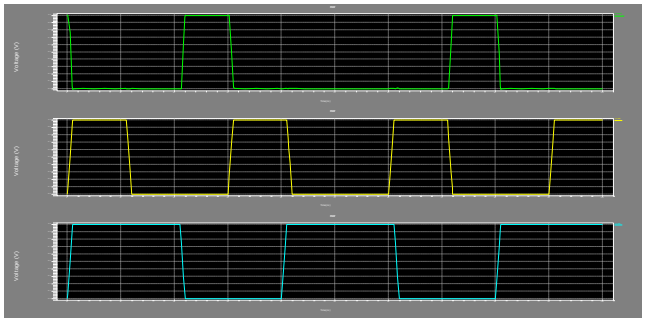

Figure 9. Waveform of NOR using CMOS

TABLE I. **Power and Delay Analysis**

Parameter	**POWER(watts)**	**DELAY(sec)**
CMOS(NAND)	1.347954e-004	-2.0582e-008
MCML(AND/NAND)	6.502383e-008	-9.9204e-009
CMOS(NOR)	1.343237e-004	1.3086e-010
MCML(OR/NOR)	4.135800e-008	-1.2330e-010

4. CONCLUSION

From the above results we conclude that unlike standard CMOS, MCML Circuits perform better in terms of power and delay and therefore used in high speed circuits. From the Table 1 it can be concluded that circuits based on MCML technology consumes less power and provides less delay as compared to conventional CMOS circuits. This paper has studied two-input universal gates implemented in the current mode technology (16nm) and concluded that MCML are faster than CMOS. Hence MCML topology shows more robustness against conventional CMOS.

5. REFERENCES

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