Implementation of Trinary/Quaternary Addition using Multivalue Logic Digital Circuit

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ABSTRACT:
Objective of multivalve logic design is to reduce number of gates needed and also to reduce interconnect path length. Interconnect path consist of the largest number of gates from input to output. The reason of these two objectives is that they will give extremely good properties when implemented in VLSI. Reducing number of gates will reduce the chip area, and minimizing interconnect path length will give opportunity to use highest clock frequency. In this paper quaternary to binary and binary to quaternary converter are designed. We can design the multivalve logic to binary converter which is use for conversion of ternary-valued input 0,1,2 and quaternary-valued input 0,1,2,3 into corresponding binary-valued output 0,1. The physical design of the circuits is simulated and tested with MICROWIND layout design tool in 50nm technology. The conversion method is simple and compatible with the present CMOS process. The circuits could be embedded in digital CMOS VLSI design architectures.

Keywords:
MVL, binary, ternary, quaternary, octal, hexadecimal.

1. INTRODUCTION:
Multivalve logic carry more information on a single line . It minimizes the number of gates needed and largest number of gates in any path from input to output. Minimizing number of gates will reduce the chip area, and minimizing depth will give opportunity to use highest clock frequency. In this paper the multivalve logic gates has been design in multivalve system and output as binary valued circuit. The proposed gates allow designing any MVL digital circuit taking advantage of the knowledge coming from the binary circuits. The multi-valued logic design consisting of two drivers and a transistor matrix is simulated using Micro wind layout design tool. Functional operation of the quaternary logic is simulated and its propagation delay, power consumption are analyze. The design is dependent on the quaternary voltages for the multi-valued logic. The logic is based on use of a CMOS and pass transistors transmission gate logic. The pass transistors transmission gate at the output has been used to pull the output node to the required voltage levels and also provide sufficient equivalent resistance for the multivalve logic implementation [1, 2, 3].

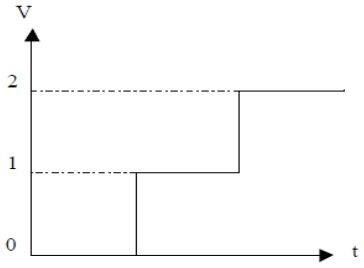

Fig 1 Ternary logic level

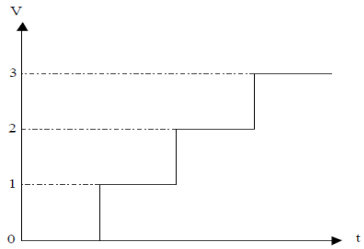

Figure 2 quaternary logic levels.

1.1 Multivalve logic system:
The binary logic have two logic levels is input and output represented by 0, 1. While the ternary and quaternary logic have three (i.e. 0, 1, 2) and four (0, 1, 2, 3) logic levels. MVL reduces the number of interconnects wires since it carries more information on a single line [1,8].

1.2 Binary Addition:
It is a key for binary subtraction, multiplication, division. There four rules of the binary addition

In fourth case, a binary addition is creating a sum of (1+1=10) i.e. 0 is write in the given column and a carry of 1 over to the next column.

A+/B	0	1
0	0	1
1	1	10

Octal Number addition:

Following are the characteristics of an octal number system.

Uses eight digits, 0,1,2,3,4,5,6,7.

Also called base 8 number system

Each position in a octal number represents a 0 power of the base (8). Example 80

Last position in a octal number represents a x power of the base (8). Example 8x where x represents the last position - 1.

Following octal addition table will help you greatly to handle octal addition.

A+/B	0	1	2	3	4	5	6	7
0	0	1	2	3	4	5	6	7
1	1	2	3	4	5	6	7	10
2	2	3	4	5	6	7	10	11
3	3	4	5	6	7	10	11	12
4	4	5	6	7	10	11	12	13
5	5	6	7	10	11	12	13	14
6	6	7	10	11	12	13	14	15
7	7	10	11	12	13	14	15	16

To use this table, simply follow the directions used in this example: Add: 68 and 58.Locate 6 in the A column then locate the 5 in the B column. The point in sum area where these two columns intersect is the sum of two numbers.

68 + 58 = 138.

1.3 Hexadecimal Number addition:

Following are the characteristics of a hexadecimal number system.

Uses 10 digits and 6 letters, 0,1,2,3,4,5,6,7,8,9,A,B,C,D,E,F.

Letters represents numbers starting from 10. A = 10. B = 11, C = 12, D = 13, E = 14, F = 15.

Also called base 16 number system

Each position in a hexadecimal number represents a 0 power of the base (16). Example 160

Last position in a hexadecimal number represents a x power of the base (16). Example 16x where x represents the last position - 1.

Following hexadecimal addition table will help you greatly to handle Hexadecimal addition.

A + B	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10
2	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11
3	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12
4	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13
5	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14
6	6	7	8	9	A	B	C	D	E	F	1	1	1	1	1	1

										0	1	2	3	4	5
7	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16
8	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17
9	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18
A	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19
B	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A
C	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B
D	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C
E	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D
F	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E

1.4 MVL Arithmetic addition:

Addition rules are the same as in the decimal system. The sum or product of two digits may only produce one or two digit numbers. In the latter case, if necessary, the first digit is carried over to the next operation (on the left.) For example, in base 7, 36 + 144 = 213. Indeed, from right to left, 6 + 4 = 13. Then 3 + 4 + 1 = 11, and finally 1 + 1 = 2.

As everyone knows, 2 + 2 = 4. This is true in all base systems. That is, except bases 2, 3, and 4. In base 4, we have 2 + 2 = 10. In base 3, 2 + 2 = 11. However, recollect that (4)10 = (10)4 = (11)3, and everything falls into its right place again. Numbers equal in one base are equal in any other base. Conversion between bases does not violate arithmetic identities. In base 2, 2 + 2 = 4 appears as 10 + 10 = 100 - looking differently but having exactly the same meaning [4,5].

The same, of course, is true of 2 × 2 = 4 which is true in all bases starting with 5. In bases 4,3, and 2 it appears as

2 × 2 = 10

2 × 2 = 11

10 × 10 = 100,

Respectively.

Ternary addition:

+ Radix Number	0	1	2
0	0	1	2
1	1	2	10
2	2	10	11

Quaternary addition:

+Radix Number	0	1	2	3

0	0	1	2	3
1	1	2	3	10
2	2	3	10	11
3	3	10	11	12

2. SIMULATION AND VERIFICATION:

We can design the multivalve logic gate truth table and then by converting binary equivalent truth table to multivalve logic truth table, we can design the CMOS layout on MICROWIND layout editor tool.

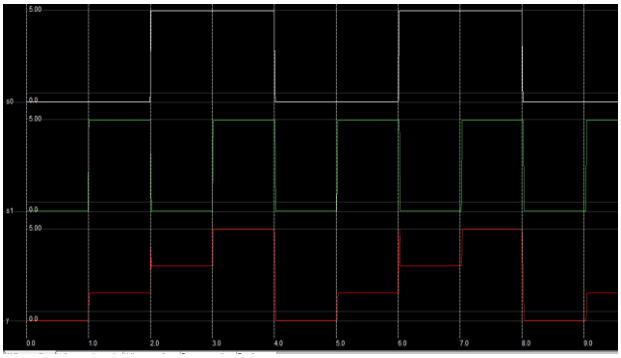

Fig 3 Timing Simulation for Quaternary Level Design

The fig 3 shows the quaternary levels of the equivalent binary signal. The level 1 is equivalent to 0V, level 2 is equivalent to 1.5V, level 3 is equivalent to 3.0V and level 4 is equivalent to 5V.

For this implementation we use transmission gate logic.

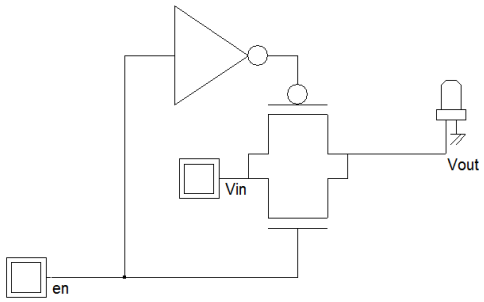

Fig Transmission Gate circuit.

The transmission gate is design by using one PMOS and one NMOS transistor. The source-source end both are connected to input. While both drain –drain end are connected to input load capacitor. One enable input is use to turn on and turn off both transistor simultaneously. The operation of transmission gate is opposite to static CMOS logic, as both transistors are turn on at the same time in transmission gate. But in CMOS only is transistor turn on at one time. In transmission gate the number of stray capacitance and interconnect length is reduce. This will reduce the power consumption and area of the design.

Truth Table of Transmission Gate.

en	Vin	Vout
0	X	No Change
1	0	0
1	1	1

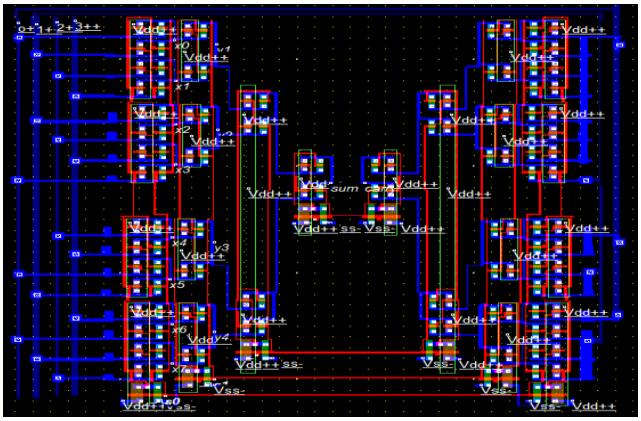

Fig Layout of quaternary two bit adder logic circuit.

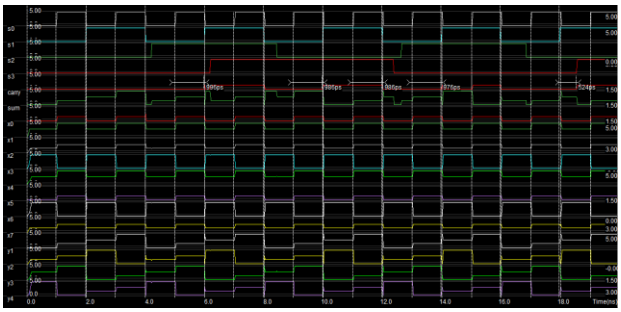

Fig Timing simulation of quaternary two bit adder logic circuit

Multiplexor type logic is design for implementation of quarterly value logic shown in fig 4and its timing simulation is shown in fig 5. It has n + l inputs, one of which is an n valued control input whose value determines which of the other n-valued inputs is selected for output. where 'xk' is a four-valued controlling or selecting input that takes on values (0,1,2,3). For input xk =0, input x, is selected; for input 'xk' =1, xp is selected, and so on. Thus, in general xo = < x l , x2, x3, x4>, using the string-sequence notation introduced in the main text [6,7] .

Design	Power dissipation	Switching delay	[1] Power Dissipation	[1] Delay
Quater-nary AND logic	500uW	10ps	641.1 to 1091.1uW	30ns to 550ns
Quater-nary OR Logic	432uW	10ps	641.1 to 1091.1uW	30ns to 550ns
Quaternary Mux 4X1	8.9uW	-	1370.0uW	48ns to 105ns

The worst case switching delay is in the range of 10 ps and power dissipation for quaternary AND logic is reduce to

500uW since the block binary to quaternary Converter consumes current as the input voltage is increased.

3. CONCLUSION

Logic having more than two levels to a single wire decreases the number of wires for the same range of data, and this reduce number of pins required for design. The reduction in logic circuit also reduces the wire interconnection length which in turn decreases resistance and capacitance of contacts and interconnections, and the interconnection delay can be greatly decreased. By using the platform of binary logic system the complexity of digital circuit is reduce in design circuit higher than binary logic system i.e. multivalve logic. CMOS technology is chosen for the circuit realization; embedding MVL circuits in binary structure will perform better than binary only. Multiple-valued logic has many theoretical advantages -its potential to increase the functional density of metal-limited digital integrated circuit layouts by reducing the number of signal interconnections.

4. REFERENCES

[1] Milton Ernesto Romero, Evandro Mazina Martins, Ricardo Ribeiro dos Santos, and Mario Enrique Duarte Gonzalez "Universal Set of CMOS Gates for the Synthesis of Multiple Valued Logic Digital Circuits" IEEE Transactions On Circuits And Systems—I: Regular Papers, Vol. 61, No. 3, March 2014 pp no 736-749..

[2] Fatma Sarica and Avni Morgu "Basic Circuits for Multi-Valued Sequential Logic" International Conference on Electrical and Electronics Engineering ELECO dec 2011 pp no. 56-58.

[3] Vasundara Patel, k s gurumurthy "Arithmatic Operation in Multivalve Logic" International journal of VLSI design and communication system (VLSICS) Vol 1 no 1 March 2010 pp no.21-32.

[4] Tanay Chattopadhyay and Tamal Sarkar "Logical Design of Quaternary Signed Digit Conversion Circuit and its Effectuation using Operational Amplifier" International Journal of Power Systems and Integrated Circuits, Vol. 2, No. 3, December 2012 pp no. 7-12.

[5] V. T. Gaikwad & P R. Deshmukh "Design Of Cmos Ternary Logic Gates" International Journal of Electrical and Electronics Engineering Research (IJEEER) Vol. 4, Issue 4, Aug 2014.

[6] Mahsa Dornajafi, Steve E. Watkins, Benjamin Cooper, and M. Ryan Bales "Performance of a Quaternary Logic Design" IEEE International Conference in year 2008.

[7] Jinghang Liang, Linbin Chen, Jie Han, and Fabrizio Lombardi "Design and Evaluation of Multiple Valued Logic Gates Using Pseudo N-Type Carbon Nanotube FETs" IEEE Transactions On Nanotechnology, Vol. 13, No. 4, July 2014 pp no. 695-708.

[8] Diogo Brito, Student Member, Taimur G. Rabuske, Jorge R. Fernandes, Paulo Flores, Senior Member, and José Monteiro "Quaternary Logic Lookup Table in Standard CMOS" IEEE Transactions On Very Large Scale Integration (Vlsi) Systems year dec 2014pp no. 1-11.

[9] Sheng Lin, Student Member, Yong-Bin Kim, Senior Member, and Fabrizio Lombardi "CNTFET-Based Design of Ternary Logic Gates and Arithmetic Circuits" IEEE Transactions On Nanotechnology, Vol. 10, No. 2, March 2011 pp no. 217-225.