Illustrative Comparison of MCML and CMOS Design Techniques using Tanner EDA

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ABSTRACT
In this paper, a comparison is done between MOS Current Mode Logic (MCML) and Complementary metal Oxide Semiconductor (CMOS) circuits operating in low power application. It is found that MCML logic circuits exhibit a decrease in delay and so decrease in overall power delay product compared with CMOS circuits. The tested inverter are optimized for low power and high-speed operation, according to the simulation of the circuits for lower voltage. This simulation is done using Tanner EDA. From the results shown it is seen that the MCML logic circuits reveal high efficiency and good performance at low power and high speeds which makes them to be more capable for application in the integrated circuits with high density.

Keywords
CMOS,mcml,tanner,eda

1. INTRODUCTION
Comparison of CMOS design techniques with the MCML technique is done in this paper. Need of this comparison is to measure the differences of both design techniques in terms of time delay , power consumption and area. For this we have compared Inverter circuit designed by both MCML technique as well as CMOS technique.

CMOS logic gates, also known as complementary MOS gates. In general, a static CMOS gate includes an nMOS pull-down network to connect the output to 0 (GND) and pMOS pull-up network to connect the output to 1(VDD).the network is arranged such that if one is ON then another will be in OFF state.

We encounter the problem while designing High-Speed ICs with classical CMOS technology that delay limits the switching speed of the gate. By correctly sizing our transistor we can improve the propagation delay times via, as large W/L ratios will result in a faster switching gate but also in a bigger power consumption.

MOS current mode logic (MCML) has various advantages over other logic styles hence it is emerged as a promising technology[4]. Power dissipation in MCML circuit is independent of its operating frequency so at high frequency power dissipation is significantly less also the switching noise is slow as current supplied during switching is constant. They offer high performance due to low voltage swing, high noise margin and high switching speed [5-8]. So, MCML style is appropriate for designing high performance digital circuits.

2. CMOS DESIGN
A CMOS transistor or device has four terminals: gate ,source, drain and body. It is a switch. To allow flow of current switch must be conducting or on to allow current to flow between the source and drain terminals.

For turning a transistor on or off we use gate terminal. There are two kinds of CMOS transistors: n -channel transistors and p -channel transistors. An n -channel transistor requires a logic '1' on the gate to turn the transistor on(to make the switch conducting). A p -channel transistor requires a logic '0' on the gate to turn the transistor on (to make the switch conducting). The p -channel transistor symbol has a bubble on its gate to remind us that the gate has to be a '0' to turn the transistor *on* .

Static power and dynamic power are two main sources of power dissipation in CMOS circuits. Static power results from resistive paths between power supply and ground. The static power dissipation of a circuit is expressed by the relation

$$\mathbf{P_{stat} = I_{stat}\, V_{DD}\text{-----(1)}}$$

Where,

I_{stat} is the current that flows between the supply railsi n the absence of switching activity.

Switching capacitive loads between different voltage levels results into Dynamic power. For a CMOS gate the dynamic power is

$$\mathbf{P_{dynamic} = \alpha C V^2_{DD} 1/\tau\text{-----(2)}}$$

where α is the activity factor of output node.

C is the total capacitance

V_{DD} is terminal voltage

τ is the transient time or time delay.

We cannot get the total power dissipation by summing up these two equations as there are other factors which also results in power dissipation these are: leakage current and short-circuit current.

Short circuit current results from both PMOS as well as NMOS being ON at the same time in a CMOS. Leakage current is defined in the different forms as main source of leakage current can be any these are:
Reverse bias leakage current (I_{REV})
Sub threshold leakage current (I_{SUB})
Thus the total current is defined in terms of these four factors

$$P_{TOTAL} = \alpha C_{load} V^2_{DD} 1/\tau + V_{DD}(I_{static} + I_{leakage} + I_{Short\ circuit})\text{-----(3)}$$

Let us consider a basic inverter circuit using CMOS design in Tanner EDA.

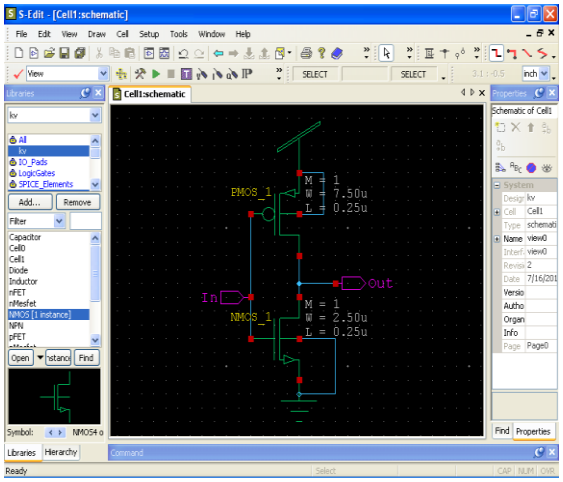

Fig 1: Basic inverter circuit using CMOS design.

3. MCML DESIGN

There are three main components of MCML circuit which includes a pull-down network (PDN), a constant current source, and a load circuit [4]. The basic MCML block is shown in Fig. 2.
Its PDN consists of source coupled NMOS transistor pairs. The constant current source generates the bias current I_{bias} while the load resistance R_L determines the output swing.

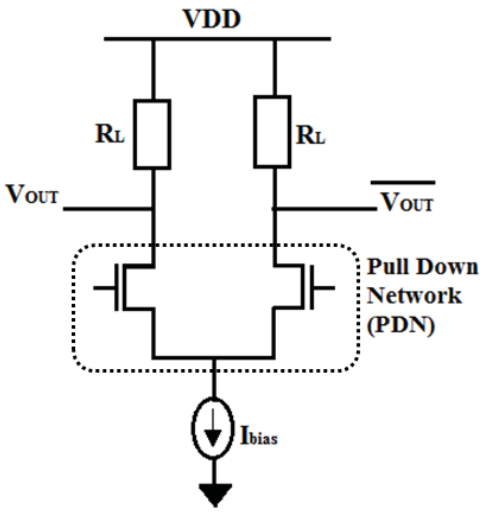

Fig 2 MCML Circuit .[4]

As the current supplied by V_{DD} during switching is almost constant thus MCML produces a small switching noise. Moreover, owing to their differential structure, MCML gates exhibit a better noise immunity with respect to complementary CMOS logic.

The optimum design of MCML gates involves minimizing a chosen quality metric such as energy-delay product or power-delay product. Since the delay of an MCML gate depends on the voltage swing ΔV and the bias current I_B.

MCML circuits consume static power because of the use of a constant current source, while dynamic power dissipation is ignorable with respect to static power. from which it is deduce that the power dissipation in MCML is constant with the frequency ,unlike conventional CMOS, thus suggesting dominant static power dissipation in MCML circuits. Therefore P_d in MCML circuits is given
by:

$$P_d = V_{DD} \text{ x } I\text{-----(3)}$$

Now , let us consider a basic inverter circuit in MCML design using Tanner EDA

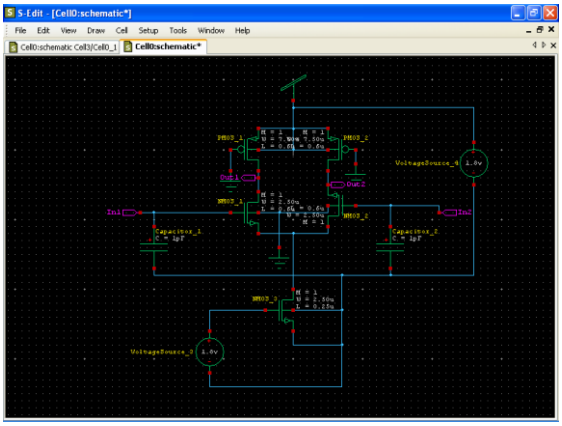

Fig 3: Basic inverter circuit using MCML design

we can see that there are two inputs and two outputs in respect to these inputs . the output is in complimentary form hence working as an inverter is fulfilled.

4. COMPARISON OF CMOS AND MCML DESIGN

When designing High-Speed ICs with classical CMOS technology we come across the problem that delay limits the switching speed of the gate. We can improve the propagation delay times by correctly sizing our transistor, as large W/L ratios will result in a faster switching gate, but also in bigger power consumption. Some techniques developed to improve the design of High-Speed circuits(as Complementary Pass-Transistor Logic(CPL) or Differential Cascode Voltage Switch Logic (DCVSL)) showed that when differential signals are used in the circuits, a compact design, a better gate design, a better noise immunity and, in a word, a better gate for this kind of High-Speed operation can be obtained.

MOS Current -Mode Logic circuits provide true differential operation , have the feature of low noise level generation, and static power dissipation: the amount of current drawn from the power supply that does not depend on the switching activity. Due to this, MCML gates have been discovered to be useful for analog and mixed-signal ICs.

The most important difference between CMOS and MCML is that MCML dissipates less power than CMOS in high frequency applications, while providing an analog friendly environment. Although the performance of CMOS technologies improves remarkably with scaling, conventional CMOS circuits cannot satisfy the speed and power requirements of these applications simultaneously. Moreover, conventional CMOS circuits generate considerable supply noise. Thus, hindering the on-chip integration of sensitive analog and digital circuits. MOS current-mode logic (MCML) has emerged as a logic style that can achieve the much needed high speeds while consuming less power than conventional CMOS circuits at these high frequencies. [1]MCML circuits enables the integration of analog and digital blocks on same chip as characterized by their low supply noise generation and high noise immunity. Static synchronous CMOS circuits have gradually more difficult challenges to overcome in terms of clock skew and switching noise in ultra-deep-submicron design.

Advantageous characteristics of MCML are lower crosstalk due to the reduced output voltage swing. This has made asynchronous circuit design an increasingly practical alternative. [1,3]

5. SIMULATION RESULTS

The low power inverter is simulated in Tanner EDA using CMOS .5um technology as well as using MCML .5um technology. the input parameters taken in the simulation

Table 1: Parameters of simulation

Technology	.5um
Supply Voltage	3.3v
Simulation time	9.98 seconds

the input data that are fed to the circuits and output for both CMOS and MCML are shown in the figures shown below

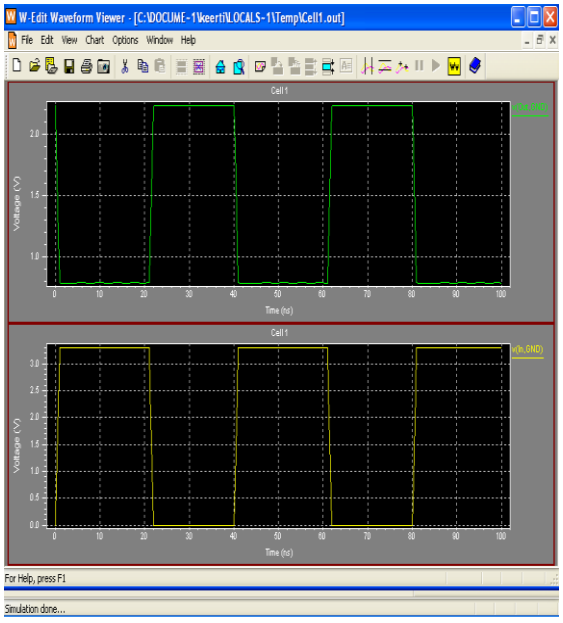

Fig 4: input and output waveforms of inverter using CMOS

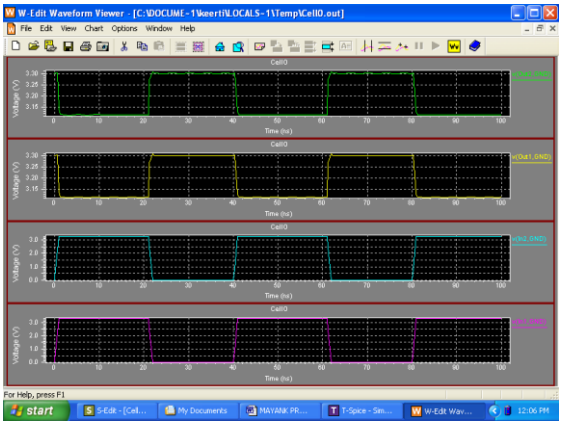

Fig 5: input and output waveforms of inverter using MCML

the performance of the MCML inverter is compared with performance of CMOS inverter to verify the reduction of power

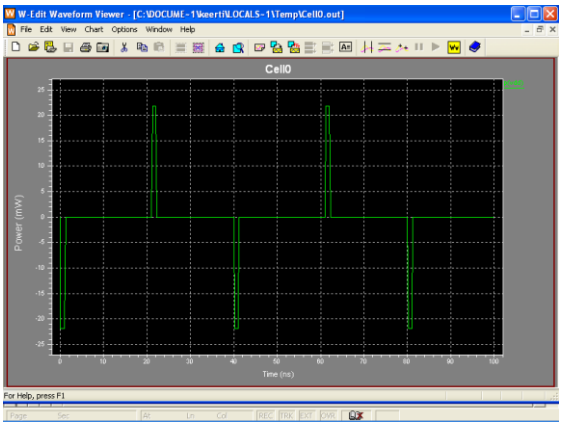

Fig 6: power dissipation by MCML inverter.

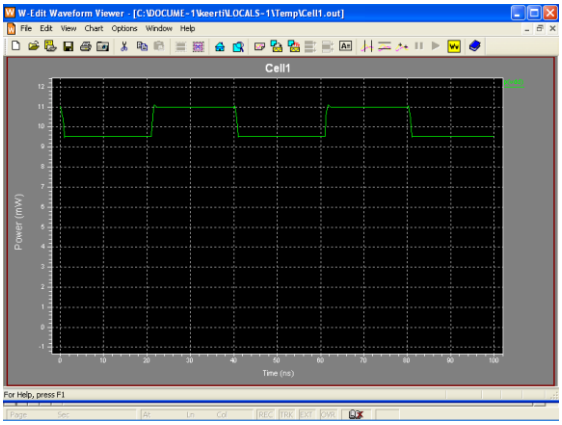

Fig 7: power dissipation by MCML inverter.

Table II: Power dissipation by MCML and CMOS inverters

Inverter	Power
MCML Inverter	Spikes of 23mW (less in comparison to CMOS)
CMOS Inverter	9.5mW to 11mW

Table III: Delay of MCML and CMOS design is compared here:

Inverter	Delay
MCML Inverter	3.0847e-010
CMOS Inverter	7.7373e-010

6. CONCLUSION

This paper presents performance comparison of static CMOS logic gates and MCML logic inverter at 0.25µm technology. All the simulations have been done on Tanner EDA software. The simulation results show that MCML logic gates are advantageous over CMOS logic gates in the applications where delay is of major concern.

The simulation results show the advantage of MCML gates over the CMOS gates for high - speed low power applications. The behaviour of MOS Current-Mode Logic inverter under conditions of reduced power supply voltage has been investigated, and it was shown that the operating voltage can be reduced by at least 54% from its nominal value without declining the gate operation. From the results shown it is seen that the MCML logic circuits disclose high efficiency and good performance at low power and high speeds which makes them to be more capable for applications in the integrated circuits with high density.

The circuits designed using CMOS technology can be designed using MCML Technology in circuits where delay is major concern.

7. REFERENCES

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