Design and Analysis of CMOS Thermometer Current Steering DAC to Remove Non-Linearity

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ABSTRACT
The Current Steering Data Converter with Thermometer technique is designed and analyzed utilizing 180nm technology in Cadence Virtuoso Simulation tool along with power supply of 1.8 V. Implementation of DAC is accomplished in such a manner that the output results subsume less non-linearities and less glitches. A novel design is proposed to ameliorate the differential non-linearities and glitches occur in the data converter to a great extent. Layout of proposed DAC is designed and realized under Cadence Assura Tool with Design Rule Check and Layout Versus Schematic. The INL is calculated with resultant values 0.256LSB.

Keywords
INL, Thermometer Current Steering DAC, Segmented DAC

1. INTRODUCTION
The data converters in digital signal processing exhibit large amount of errors in static as well as in dynamic form. The errors not only reduce the performance but also deteriorate the accuracy of conversion from digital to analog signal. Numerous Techniques are designed for the purpose of eliminating the cause of non-linearities in architectural design of current steering DAC. The non-linearities happen due to static and dynamic errors. To convert the data more accurately, current steering technique is utilized with improved linearity. The linearity of data converter is greatly affected with the factors like process variation, mismatching of current sources and parasitics associated with the capacitance.

To reduce the impact of non-linearities, the bits of thermometer coded D/A converter are increased with the assistance of higher order of binary to thermometer decoder. The main challenge is to implement the design achieving static linearity [1]. Mismatch between current sources is basic reason of non-linearity in current steering digital to analog converter which is disseminated by environmental and process variations [2]. Non-Linearities constitute INL and DNL, are the general characteristics are to be considered in implementing the architecture of D/A converter. Another cause of concern of non-linearity in current steering DAC is the output impedance of the DAC is code-dependent. The paper demonstrates the technique which primarily focuses on the criterion to deal with factors causing errors. The code-dependency in the output impedance is amended with current switching technique in which complementary current cell is attached with traditional current cell and the current cell and the current flowing through the current sources steers towards the different output nodes simultaneously and is code-independent [3]. The proposed DAC is designed considering this technique along with reducing the non-linearities by increasing the number of bits to be processed in thermometer DAC.

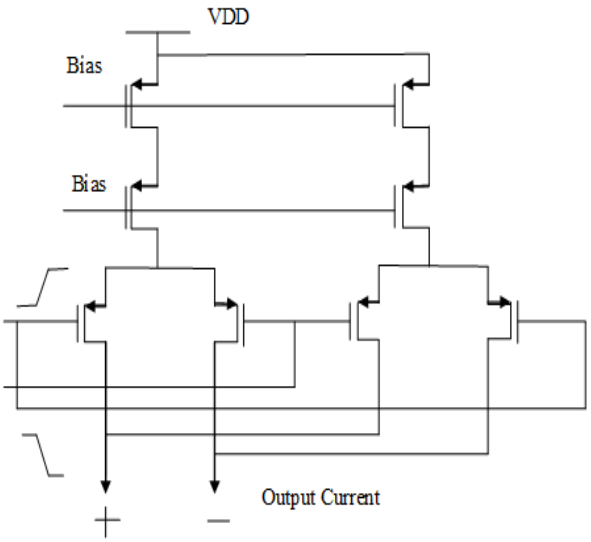

Fig. 1 Efficient Output Impedance Circuit [3]

2. PAPER ORGANISATION
The Thermometer DAC is designed and analyzed under Cadence Virtuoso Tool and layout of the architecture design is implemented further in Cadence Assura Tool with DAC and LVS verification. Section 3 deals with explication of current cell utilized in the design of data converter with schematic design. Section 4 elaborates the decoder employed for proposed design with schematic design. Section 5 describes the design of Latch to enhance timing problems. Section 6 explains the thermometer of data converter with schematic and layout design. Section 7 constitutes the Layout Simulation of proposed thermometer DAC. Section 8 contains the results and simulation design along with specifications.

3. CURRENT CELL
The operation of current steering is exercised with the utilization of a properly design current cell which comprises of matched current sources and differential switches. The principle source of non-linearities in the D/A converter is mismatching exist between current sources. To mitigate such non-linearities, proper aspect ratio of current sources is considered and current cells are attached parallel with each other in such a manner that based upon every bit input value, the current is derived to the load. The Schematic design of current cell is demonstrated in Fig. 2. The switches will operate on the appropriate binary input. For the design of an N-bit thermometer DAC, 2^N-1 current cells are required.

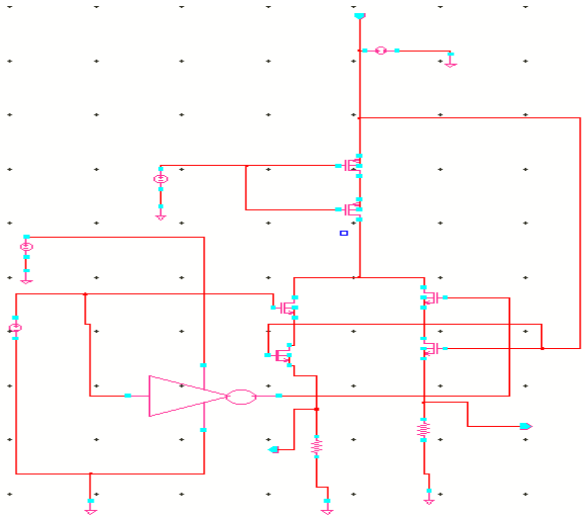

Fig. 2 Schematic Demonstration of Current Cell

4. DECODER

For the architectural design of thermometer DAC, the decoder is employed which provides the thermometer input to all the current cells for functioning. The binary to thermometer DAC is implemented with logic gates AND, OR, NAND, NOR designed with Metal Oxide Semiconductor transistors in 180nm technology. Four binary input bits in decoded to fifteen thermometer bits as demonstrated in Fig. 3.

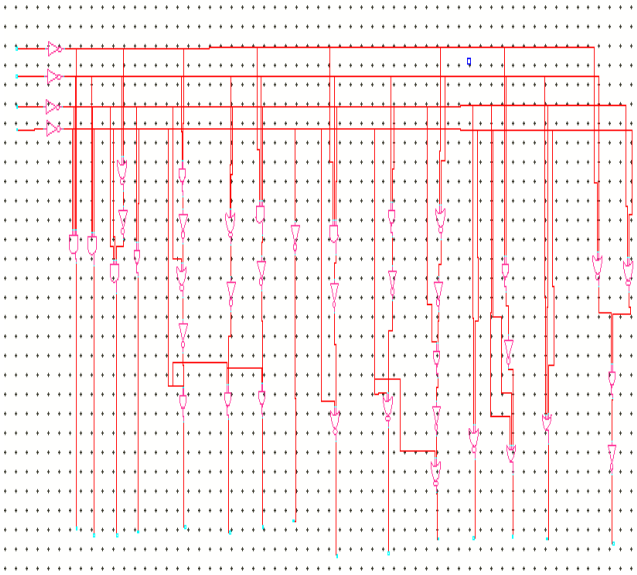

Fig. 3 Schematic Demonstration of Binary to thermometer decoder

5. LATCH

The decoder when provides input to all the current cells experiences a synchronization problem between the input and output signals which largely affects the performance and output of digital to analog converter with the presence of glitches. To enhance the performance of data converter, a Latch is introduced between decoder and current cells for effective timing accuracy. Latch is designed with MOS transistor as shown in Fig.4 under 180nm CMOS technology.

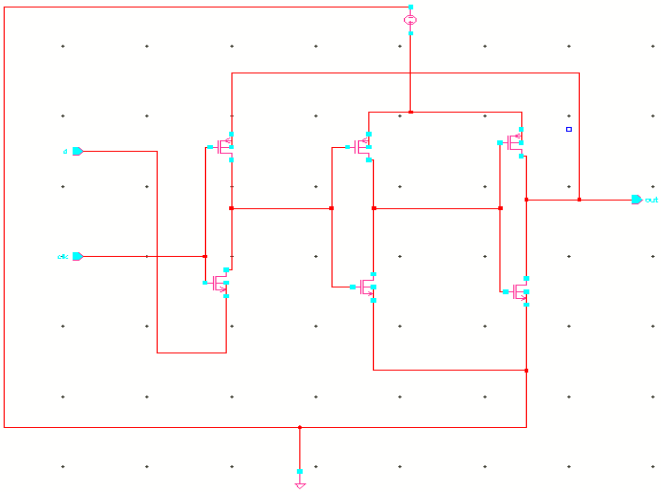

Fig. 4 Schematic Demonstration of Thermometer-decoded DAC

6. THERMOMETER-DECODED DAC

The thermometer-decoded data converters have emerged as the latest technology in the field of digital signal processing. The thermometer DAC is so named depending upon the operation of accessing bits in decoder from binary to thermometer bits. Each output of decoder senses a change of all ones to all zeros which generally refers similar to thermometer equipment. However, this technique of converting data from discrete form to continuous form emulates the current cells to activate on the occurrence of a higher order input bit. The output of decoder becomes the input of each current cell as given in the Fig. 5.

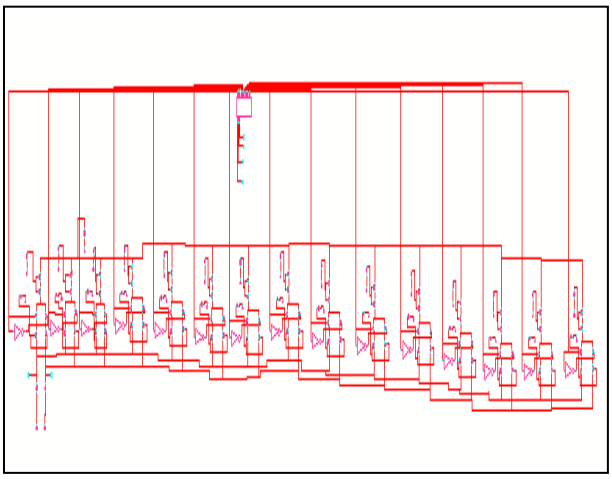

Fig. 5 Schematic Demonstration of Thermometer DAC

The thermometer DAC comprises of decoder, latch for synchronization and current cells. The current cells are connected so that the switches depending upon the input bits get activated or deactivated and current is being steered from current sources to the output end. The thermometer is favourable where very less glitches, non-linearites and large monotonicity are obligatory.

7. LAYOUT-DESIGN OF THERMOMETER DAC

The layout of thermometer DAC is implemented and simulated in Cadence Assura tool with Design Rule Check and verification is done in Layout versus schematic in CMOS 18nm technology as shown in Fig. 6.

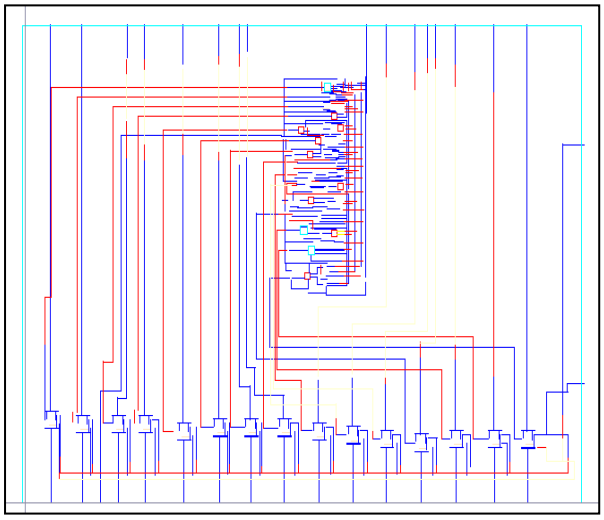

Fig. 6 Layout design of Thermometer DAC

8. RESULTS AND SIMULATIONS

The thermometer DAC is simulated and result is analyzed in its transient response with the stop time of 200ns. Fig.7 shows the simulation waveform of binary to thermometer decoder as four bit input is applied to decoder which transforms into fifteen output signals.

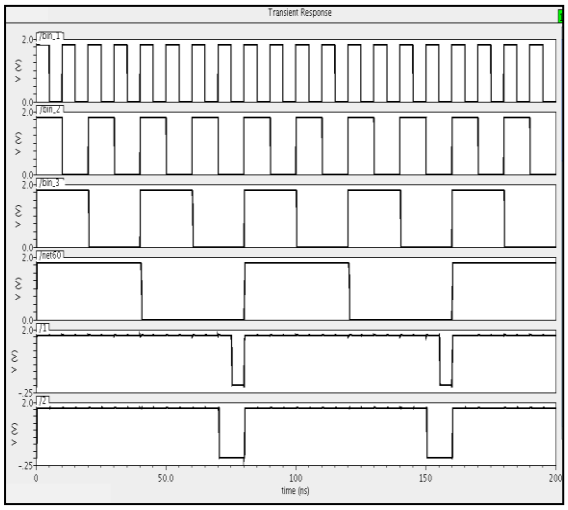

Fig. 7 Simulation Result of Binary to Thermometer Decoder

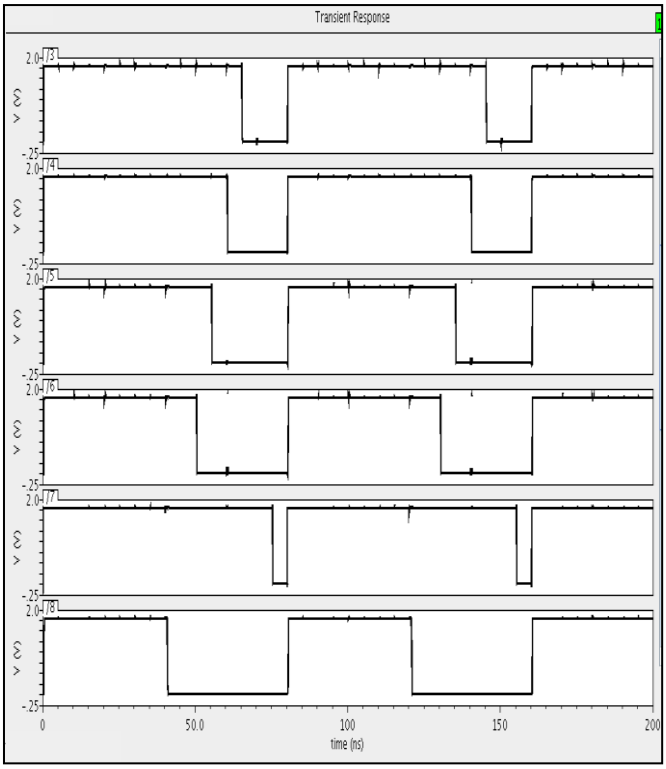

Fig. 8 Simulation Result of Binary to Thermometer Decoder

The Design Specifications of Binary to Thermometer DAC is given in the Table 1 which obtained after the realisation of decoder.

Table 1. Design Specification of Binary to Thermometer Decoder

Technology	180nm
Resolution	4 bits
Supply Voltage	1.8 V
Period	80ns
Pulse Width	40ns
Frequency	12.5 MHz

The technology under which architecture of decoder of DAC is designed is 180nm with the voltage supply of 1.8 V. The time period of simulation is 80ns with pulse width of 40ns and frequency of simulation is 12.5MHz. The decoder is to be accurate enough to transfer the precise output to each current cell with latch. The reduction of errors in output of digital to analog converter is achieved with proper sizing of MOS transistors and with matched current sources.

Table. 2 : Design Specification of Proposed Thermometer DAC

Technology	180nm
Resolution	4 bits
Supply Voltage	1.8 V
Maximum Period	80ns
Stop Time	200ns
INL	0.256LSB
Full Scale Output Voltage	1.4 V

The Design Specification of proposed thermometer DAC with more linear output response is given in the Table. 2 which describes the technology under which the architecture of data converter is implemented as well as simulated, time period upto which the output response is calculated, the value of output voltage is obtained and frequency of transient response.

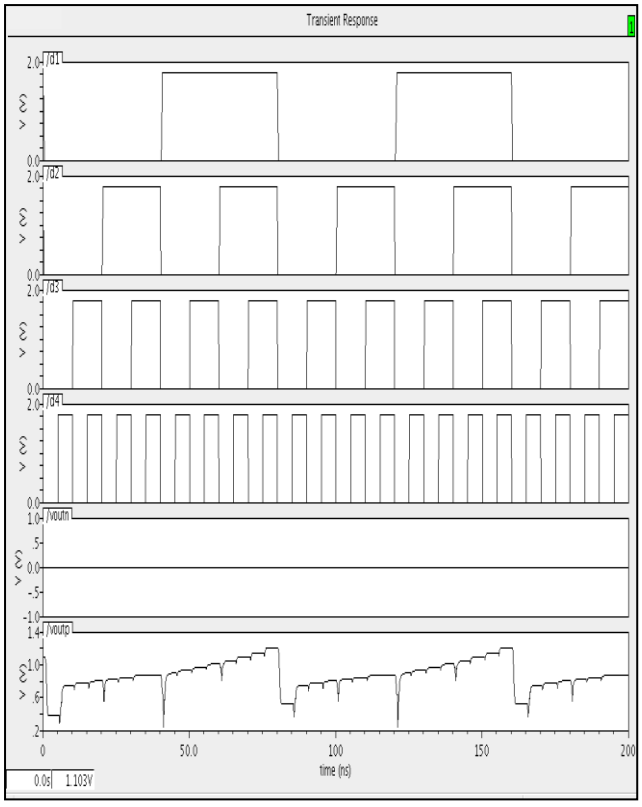

Fig. 9 Simulation Result of Thermometer DAC

The Simualtion Waveform of Thermometer DAC is achieved with the INL less than 1 LSB shown in Fig. 9. With the pattern of input bits provided to DAC, the ramp output is obtained where each step is linearly increased according to the input signal.

9. REFERENCES

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