Circumventing Short Channel Effects in FETs: Review

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ABSTRACT
The present paper aims at providing a thorough and yet a collective evaluation of some commendable research works done over the past decade with the aim for reducing short-channel effects (SCE). The necessity for development of these technologies arose as short channel effects such as – Drain-Induced Barrier Lowering (DIBL) and hot carrier effects arises manifold as the channel length is scaled further into the deep-submicron region to accommodate changes in ULSI applications. The review highlights some recent techniques to circumvent these effects in fabricated MOS devices, and in addition a short evaluation of strengths and weakness in each research works is also presented.

Keywords
Short-Channel effects (SCE), Silicon on Insulator (SOI), Drain Induced Barrier level (DIBL), deep-submicron, ULSI.

1. INTRODUCTION
The performance of modern devices may be attributed to scaling of MOS dimensions. Speed, power, functionality, packing density and reduced cost, etc. are some of the advantages achieved as a result of scaling. Controllability of the gate over the channel depletion area has been a major issue which may be attributed to increased charge sharing from drain or source. Short channel effects (SCE) may lead to several unintended reliability issues such as threshold voltage, scattering of device characteristics during fabrication process. Degradation in performance in the channel depletion layer as described by Poon and Yau's model is due to charge sharing by drain and gate electric fields. Scaling of devices has led to tremendous increase in leakage current or static power and consequently there is a need to decrease the supply V_{DD}. Decreasing V_{DD} may have multiple repercussions such as scaling the threshold voltage V_{th} which in turn increases the leakage current and static power in the sub-threshold regime. Use of Tunnel Field Effect Transistor (TFETS) is advantageous over a traditional MOSFET fabricated in a bulk silicon wafer as the subthreshold slope should not be less than 60mV per decade limit [15]-[18].

Short Channel Effects (SCE) may be attributed to the DIBL effect which reduces the threshold voltage as the channel length is scaled. Drain induced barrier Lowering (DIBL) depends on certain factors such as film thickness, film doping, BOX (buried oxide) thickness, etc.

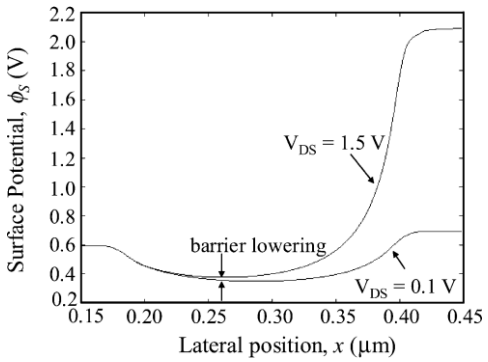


Figure 1: Surface potential variation along the position in channel for 0.1V and 1.5 V drain voltages [17].

As indicated in Figure 1, DIBL effect takes place when the potential barrier height between the source and the channel region reduces under the influence if drain electric field when a high drain voltage is applied. The drain off-current increases because the number of carriers injected into channel from source increases gradually. Hence it may be said that the drain current is controlled by both gate voltage and drain voltage.

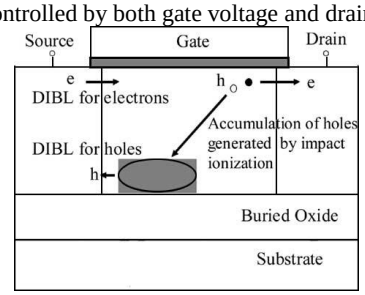


Figure 2: Mechanisms which determines Short Channel effects in SOI MOSFETs [17].

As mentioned by Anurag et al., two methods to determine SCEs in thin film SOI MOSFET devices may be, firstly with positive bias effect in the body due to holes accumulation due to impact ionization near the drain. Secondly, the DIBL effects in the potential barrier at source near the bottom of the thin film, which is illustrated in Figure 2 [17]. The rate of hole generation due to impact ionization increases as the gate length is reduced, and then positive bias the body thereby reducing threshold voltage V_{th}.

Organic electronic devices are generating momentum in recent years due to the numerous advantages associated to its name – ease to fabricate, simple device architecture, limitless material variety, and wide applications. Organic FETs (OFET) finds itself useful in photovoltaic cells, memories, sensors and LEDs. The main difficulty is in photolithographic processing because organic solvents are used for both depositing and erasing photoresist layers. However, due to low selectivity of photoresist layer that needs erasing and not the organic electronic materials. The selection of organic solvents has been done based on miscibility and orthogonality among certain materials. Miscibility is for removing unwanted

portion of the deposited photoresist layer, while orthogonality protects the underlying thin polymer films from lithographic chemicals. Among the various solvents, segregated hydrofluoroethers (HFEs) have been selected accounting to their superior properties such as zero ozone depletion, non-flammability and low toxicity [1].

2. REVIEW OF PROPOSED SOLUTIONS

Short Channel Effects due to scaling of channel lengths is mainly due to encroachment of drain electric fields in the channel depletion region as shown in Figure 3. The metal at the gate may shield the top of the device against the electric field lines, however, they penetrate the device through the buried oxide layer and silicon wafer substrate thereby causing tremendous DIBL effects. Various device structures have been proposed for reducing the degrading effects in the submicron MOSFETs which are discussed below:

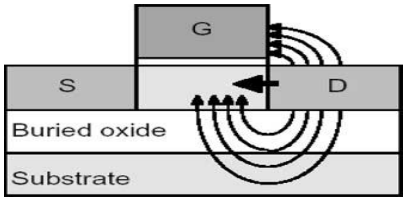


Figure 3: Drain electric field lines interfering with channel.

A. Micro-scale organic field effect transistors

Figure 4 shows the fabricated micro-scale OFET. Initially the polyethylene terephthalate (PET) substrate is cleaned by using a standard cleaning solvent using de-ionized (DI) water, 2-propyl-alcohol and acetone in an ultrasonic bath for about 5 min in each cleaning. The substrate was dried at 100°C for an hour at vacuum for evaporating the residual moisture and solvent. The gate Al electrode of thickness 30 nm is deposited by a thermal evaporator through a shadow mask at a deposition rate of 0.5 Ang/s at a pressure of 10^{-6} Torr. The mixed PVP solution is spin coated at 3000 rpm for 30s, followed by soft-baking over a hot plate for uniform deposition. The coated photoresist film is exposed under UV light through a photo mask. To fabricate the source and drain electrodes 30 nm thick gold is deposited after deposition of a 5 nm thick Titanium adhesion layer [1].

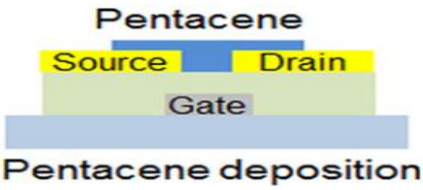


Figure 4: Device fabrication of the proposed micro-scale pentacene OFET devices [1].

The performance of the above mentioned method are summarized in Figure 5 below. Figure 5 (a) shows the drain current vs. gate voltage when drain-source voltage is fixed to -40V in the logarithmic scale. A p-type transfer characteristics is observed using the pentacene active channel. The on/off current ratio was some 10_2–10_3 due to the injection barrier and short channel. Figure 5(b) shows the output characteristics i.e. drain current vs. drain voltage for a 3 µm channel device. A non-linear curve is seen at the output characteristics which indicated the presence of an injection barrier at the metal-pentacene contacts. While Figure 5(c) shows that resistance decreases as the channel decreases. Figure 5(d) highlights the contact resistance as function of gate voltage. It may be concluded that on applying a large negative input in p-type short channel devices, the evolving high current density in the conducting channel may cause a small voltage drop over the contact region.

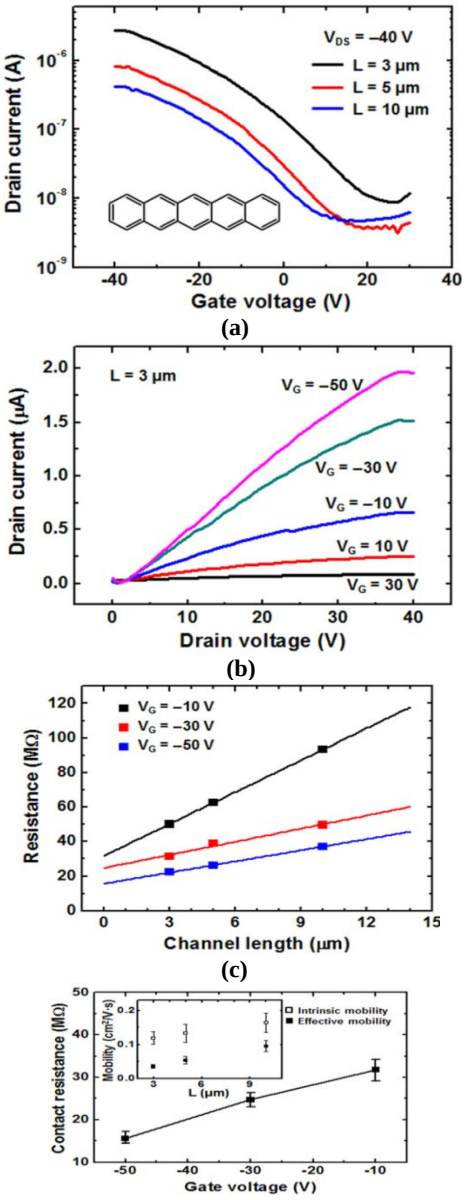


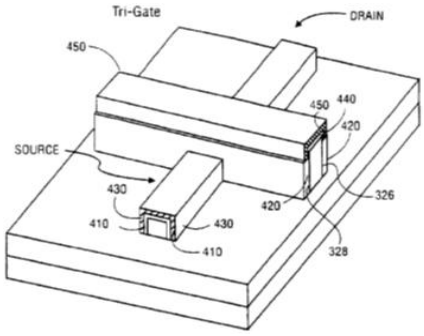
Figure 5: Various results with variation in channel lengths, 3, 5 and 10 µm (a) Transfer characteristics. (b) Output characteristics (c) Series resistance vs. channel length at -10, -30 and -50V gate voltages. (d) Contact resistance at -10, -30 and -50 V [1].

The research work by Jang et al. successfully fabricated micro-scale OFET devices on a flexible substrate by using traditional photolithography manufacturing process using a fluorinated solvent. The 3 µm fabricated channel pentacene OFET exhibited stable electrical characteristics in both bending and flat conditions [1].

B. SOI MOSFET developments from single gate, double gate, triple gate structure.

Prashant et al. [6] proposed a tri-gate type SOI MOSFET for circumventing SCEs in 60 nm gate length SOI type

MOSFETs. The structure has a gate di-electrode formed on dielectric over the semiconductor body opposite to the gate electrode. Since the gate electrode and the gate dielectric surround the device body, it has three separate channels and three gates. Figure 6 shows the tri gate structure for a fully depleted SOI device. Experimentation with a 60 nm gate length shows that tri gate structure reports superior performance for non-planar device.



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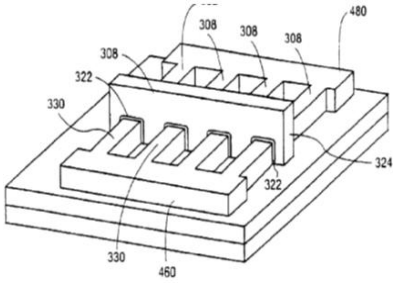


(b)

Figure 6: Complete tri gate structure [6].

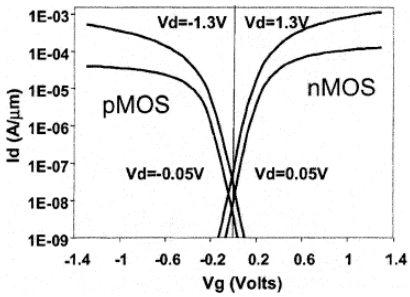


Figure 7: I-V characteristics for a 60 nm gate length NMOS and PMOS transistor. I is the normalized width [6].

C. CARBON Nanotubes (CNTs) with G-C interfacial layer for low resistance electrical contact.

In order to reduce SCEs, Chai et al. [7] used graphitic carbon (G-C) interfacial layer to carbon nanotube and also reduce the subthreshold swing of transistors by using these improved contacts. They used five different kinds of metal as electrodes (Pd, Pt, Au, Ti and W) on different Carbon nanotubes. Figure 9(a) shows the energy band diagram which reveals that the Fermi level of the metal aligns properly with the valence band of CNT. Figure 9(b) shows the I_d-V_{gs} transfer curve of the Carbon nanotube device under varying metal contacts. The ON state conductance of the CNT showed no dependence on metal work function. Pt has the highest work function i.e. 5.9 eV among the group. Although Ti showed lower work function than other metals in the group, i.e. 4.3 eV, it showed better conductance than those Pt contacted devices. From the experiment it can be concluded that the contact improvement is due to the presence of the G-C interfacial layer rather than heat induced relaxation [7].

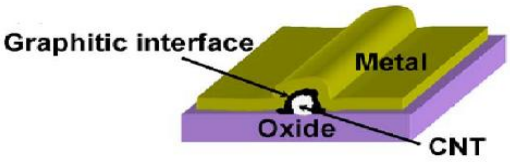
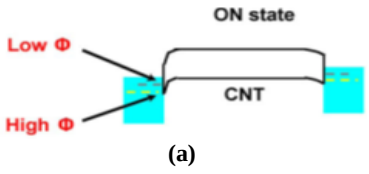


Figure 8: Schematic of CNT/metal interface with G-C interfacial layer



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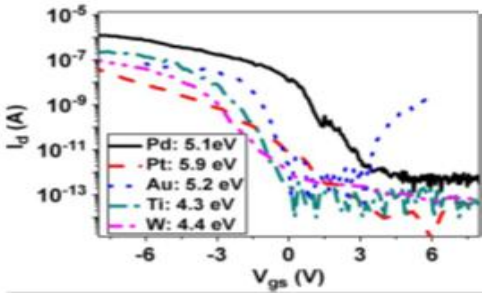


(b)

Figure 9: (a) Energy band diagram of the ON state conductance. (b) Transfer curves I_d-V_{gs} of single CNT devices with different contact metals.

D. Graded channel dual material double gate (GCDMDG) for enhanced analog/RF performance.

Sharma and Bucher [8] identified a novel architecture for reducing SCEs in DG MOSFETs. The analyses were done in the sub 20 nm regime using ATLAS device simulation. GCDMDG type MOSFET achieved superior drain current, higher cut off frequency and peak transconductance at lower drain current. The performance of the proposed method was compared with other existing advanced methods. Figure 10 shows the GCDMDG type MOSFET structure, whereas Table I shows the comparison with various DG works.

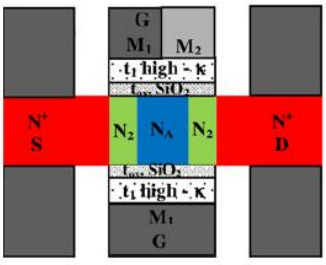


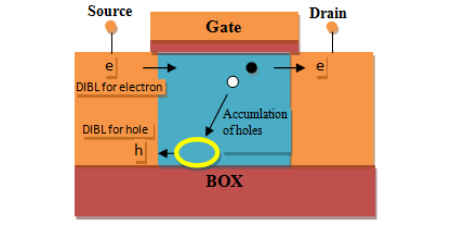
Figure 10: Schematic of GCDMDG MOSFET [8].

Table 1: Analog/RF figures of Merit for various DG MOSFETs [8].

Device parameters: L_G=15 nm. T_{si} = 6 nm, EOT = 1nm, V_{GS}=0.3V, V_{DS}=1V								
Device	g_m(mS/μm)	g_m/I_{ds} (V)	g_m/g_{ds}	V_{EA} (V)	f_T (GHz)	f_{max} (GHz)	TFP(X 10^3) (GHz/V)	TFP(X 10^5) GHz/ /)
DG	2.44	12.7	17.7	1.39	476	1140	6.05	1.07
DMDG	2.19	13.5	20.2	1.50	439	1110	5.91	1.19
GCDG	2.91	13.4	15.2	1.14	546	1170	7.31	1.11
CDMDG	2.79	14.1	17.9	1.27	534	1160	7.55	1.35

E. FD-SOI MOSFET using high k-gate spacer dielectric.

Deepesh et al. [9] in their work studied the performance of fully depleted SOI MOSFET using high k-gate spacer dielectric using sentaurus TCAD simulator. In their model, a lightly doped channel is assumed to avoid degrading the carrier mobility and threshold voltage variations. The doping concentration of source/drain region is however maintained at 1 x 10^{-19} cm^{-3} with a gate length 25 nm.6 nm, 0.6 nm and 20 nm being the thicknesses of silicon film, gate oxide and buried oxide respectively. A work function of 4.4 eV SOI MOSFET was assumed. Figure 11 illustrates the proposed model and the simulation results; the I_{ON}/I_{OFF} is significantly higher in high k-spacer thereby improving subthreshold slope by 12% and reducing DIBL by 22%.



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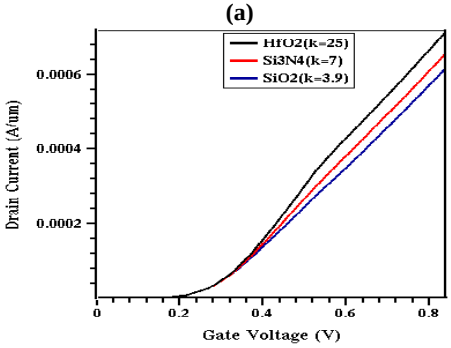

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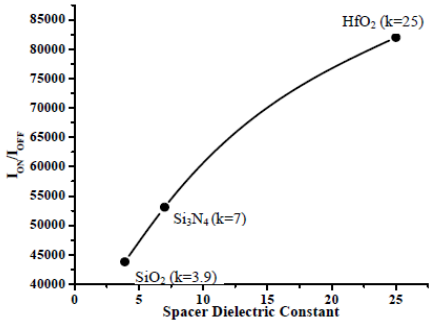

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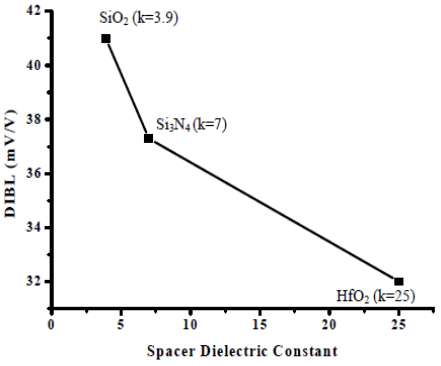


(d)

Figure 11: (a) Illustration of proposed method. (b) Ids-Vgs characteristics of three dielectric offset spacer SOI devices. (c) ON current to OFF current ratio for different spacer of different dielectric values. (d) DIBL variation of SOI device with different spacer dielectric [9].

F. Short-channel undoped symmetrical double gate metal –oxide-semiconductor FETs.

Ioannidis et al. [11] studied the effect of localized interface charge on the threshold voltage of short-channel undoped symmetrical Double gate MOSFETs. An analytical threshold voltage model of short channel undoped symmetrical double gate MOSFET which includes positive or negative interface charges near the drain is presented. The threshold voltage model was derived assuming an analytical solution for the potential distribution along the channel in the subthreshold regime. A cross section of the symmetrical DG MOSFET with localized interface charges is shown in Figure 12. While Figure 13 shows different types of threshold voltage plots.

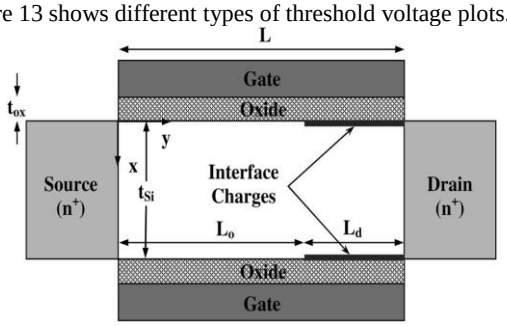
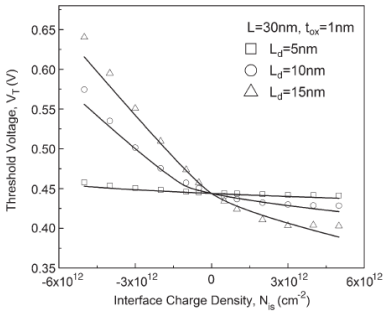


Figure 12: Schematic cross section of symmetrical DG MOSFET with localized interface charges [11].



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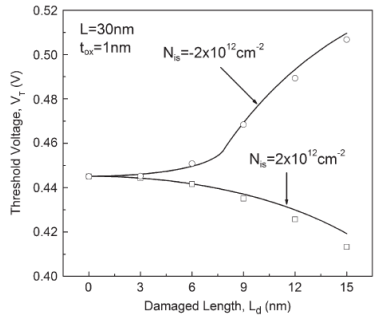

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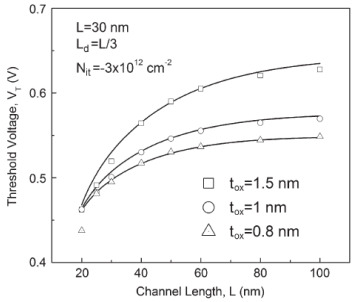


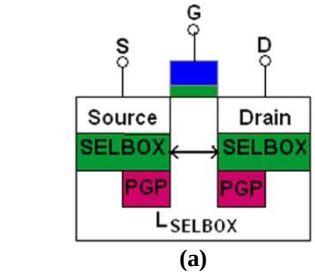
(c)

Figure 13: (a) Threshold voltage vs. interface charge density plot of DG MOSFETs (b) Threshold voltage vs. damaged region length for different voltages of interface charge densities (c) Threshold voltage vs. channel length plot for fixed values of L_d and N_{it} [11].

G. PGP-SELFBOX or Partial-ground-plane (PGP)-based MOSFET for reducing the magnitude of SCE.

Iyer et al. [12] carried out an extensive simulation study on the use of PGP-SELFBOX and SELFBOX structures for supressing self-heating effects and SCEs in the PGP-SELFBOX. SELFBOX type devices connects active region to the substrate offering a path for heat dissipation. A new SELFBOX has been proposed and simulated using Medici simulator. In this device, the BOX is covering only the source and drain regions and a window has been made under the channel region. The PGPs have been used under the SELBOX, with the edge of PGP in line with the source/drain junctions and the SELBOX edge. The ground plane (GP) technique is used to reduce SCEs. The use of heavily doped GP is an effective means to prevent the electric field lines from the drain to reach the source directly. With PGP, the electric field line coupling is minimized, resulting in the reduction of SCE-like DIBL. The use of continuous GP, however, increases the source and drain parasitic capacitances and increases the crosstalk. However, the use of PGP reduces this problem considerably. The problem of floating-body effect in SOI (partially depleted) is alleviated in the SELBOX and PGP-SELBOX devices. This is because the holes generated by impact ionization can quickly go out of the devices [12].

Figure 14 (a) shows the schematic of the model. While Figure 14 (b) shows the output characteristics of the proposed model.



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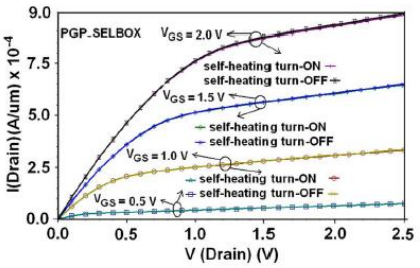

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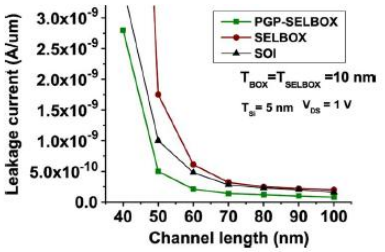


(c)

Figure 14: (a) Schematic of the PGP-SELFBOX structure (b) Output characteristics (c) Leakage current [12].

H. Single halo implantation on the Carbon nanotube field effect transistor (SH-CNFET).

Carbon nanotube FETs are ultra-thin bodies and does not suffer from severe mobility degradation as typically observed for silicon MOSFETs with nanometer dimensions. Halo implantation creates a non-uniform potential under the channel and causes to suppress channel leakage current. In order to achieve the benefits of both halo implantation and CNTFET structures, Arefinia and Oruoji [13] proposed application of single halo (SH) implantation in CNTFET structures to reduce SCEs. Therefore, for the first time we have simulated SH-CNTFET structure using two-dimensional (2-D) quantum simulation. In the SH-CNTFET, as shown in Figure 1, we consider a (13, 0) CNT with a diameter of 1 nm that is embedded in a cylindrical gate insulator of HfO_2 with thickness 2nm and dielectric constant 16. The channel length is 15nm, which consists of 10nm undoped (intrinsic) CNT and 5nm p-doped CNT as halo implantation. The length of n-doped CNT extensions is30nm at the source and drain ends. Pocket implantation on the source side of the SH- CNTFET is kept at 0.7nm and the source/drain doping is 1nm. All the device parameters of the C-CNTFET are equal to the SH-CNTFET unless its 15nm channel is intrinsic CNT [13].

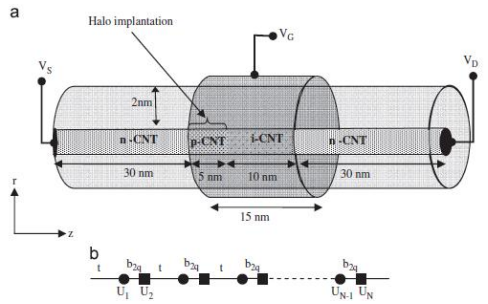
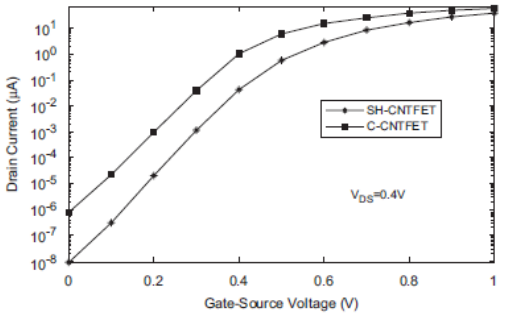


Figure 15: SH-CNFET structure with coaxial gate [13].



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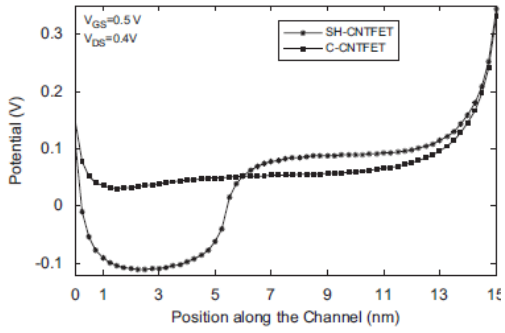


(b)

Figure 16: (a) Transconductance characteristics of C-CNTFET and SH-CNTFET structures on logarithmic scale (b) Potential profile along the channel of SH-CNTFET and C-CNTFET [13].

I. Silicon-Germanium-on Insulator (SGOI) MOSFETs.

Figure 17 shows the cross-sectional view of strained Si on SGOI MOSFET. A strained –Si MOSFETs on SGOI substrate can be fabricated by using a combination of SIMOX and ITOX. A SiGe layer is grown directly on a Si substrate using an ultrahigh-vacuum chemical-vapor-deposition process. A uniform buried oxide formation inside the SiGe layer and also the relaxation of SGOI are realized by the usual SIMOX process (oxygen ions are implanted into the Si substrate, and high-temperature annealing is carried out to grow a buried SiO2 layer). Thereafter, the increase in both the Ge content of SiGe and buried oxide thickness is simultaneously achieved by oxidizing the top SiGe layer in oxygen–argon gas mixture ambient through the Ge condensation technique (low temperature ITOX annealing). For a fully depleted structure, a strained-Si thin film is directly grown on this thin SGOI substrate. By varying the Ge mole fraction in SGOI layer the amount of strain in the thin silicon layer on top can be controlled [14]. Figure 18(a) shows the variation of the threshold voltage with the change in strain (Ge content in SiGe) for a gate length of 50 nm (effective channel length of 45 nm). We can observe that the threshold voltage decreases almost linearly with an increasing strain (even becoming negative for a Ge content of 0.3–0.4), and the decrease in *V*th is quite significant. Figure 18 (b) shows the variation of the threshold voltage with gate length for different values of Ge mole fraction in the SGOI layer for a strained-Si thickness of 5 nm and SiGe thickness of 10 nm. It is observed that *V*th falls sharply below ~75-nm gate length due to short-channel effects like drain induced barrier lowering (DIBL), the gate-S/D charge sharing, etc. The *V*th values from the analytical model are in close proximity with the simulation results. The DIBL is computed as the difference between the linear (V_{DS} = 0.05 V) and saturation (V_{DS} = 0.5 V) threshold voltages. Figure 18 (c) shows the DIBL variation with gate length for 20% Ge mole fraction. It is observed that the DIBL is significant for small channel lengths (below 60–70 nm), while it is negligible for longer channel lengths (above 100 nm) [14].

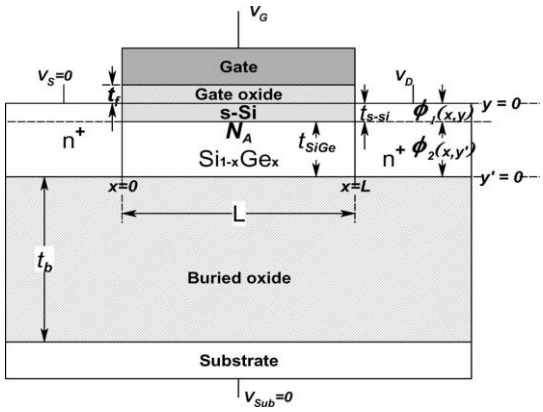
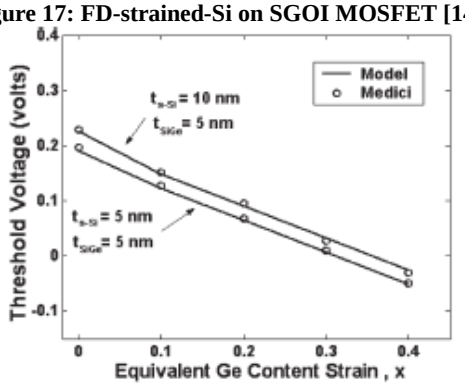
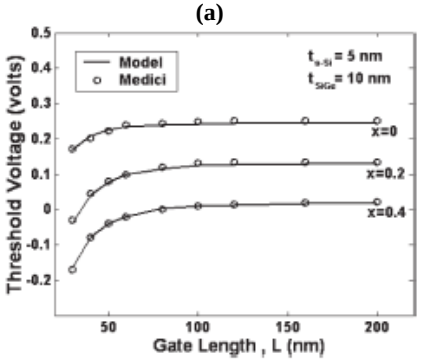


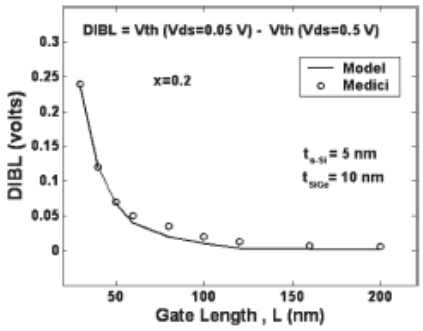
Figure 17: FD-strained-Si on SGOI MOSFET [14].



(a)



(b)



(c)

Figure 18: (a) Variation of threshold voltage with strain (b) Linear threshold voltage versus channel length (c) DIBL versus channel length [14].

3. CONCLUSION

In the section II of this paper, the physical structures responsible for controlling the SCEs in SOI devices are studied and appropriately cited. The detailed results of each research works are highlighted. Some novel device architectures and materials used for fabricating highly efficient FET with reduced SCEs as well as par performance of FET reviewed in current paper.

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