Different Techniques used for Carry Select Adder - A Review

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ABSTRACT
To design the power and area proficient fast speed data path logic systems, the field of very large scale integration (VLSI) is the generally significant area of research where minimize the area and power is the more difficult task. In digital system, mostly adders lie in the crucial paths that affect the whole performance of the system.To perform the fast arithmetic functions in many data processing processors at low cost, carry select adder is the most suitable adder among the various adders. In this paper, we describe the different techniques which are used to design the proficient CSLA.

Keywords
Carry Select Adder (CSLA), Arithmetic logic unit (ALU), RCA, BEC, CBL, D-Latch, Basic unit.

1. INTRODUCTION
The adders are most widely used in electronics applications. Adders are not only used in arithmetic logic unit but in addition to the other parts like calculate addresses, table indices and similar applications. Others uses are multiply accumulated structure (MAC) also in multipliers in high speed integrated circuit and digital signal processors. Currently, the most usable area in research of VLSI is the design of area proficient and low power fast speed data path logic systems. Others are classified as carry look ahead adder, CSLA, ripple carry adder on the basis of requirement such as delay, area and power consumption.

Carry select adder (CSLA) is generally the combination of two ripple carry adders (RCA) and multiplexer. It is depend upon the principle of to calculate sum which in turn depends on assuming input from the previous stage .One carry input is zero (0) and other carry input is one (1).The multiplexer will select the appropriate sum [2] Fig.1.

Area of the carry select adder is not proficient because it uses numerous pair of ripple carry adder to produce the partial sum and carry through supposing Cin='1' and '0' and final output is selected by multiplexer. Carry select adder is used in many processors and computational systems to remove the difficulty of propagation delay.

The RCA consists of many cascaded single bit full adders. Unlike CSLA, its figure is area efficient and simple but its speed is slow because it needs previous carry out signal till the operation starts. Before the carry in signal arrive summation is ready. Here in CSLA, only need to wait for the multiplexer delay in every single bit adder [14]. Carry propagation delay can reduce by 'N' times than RCA.

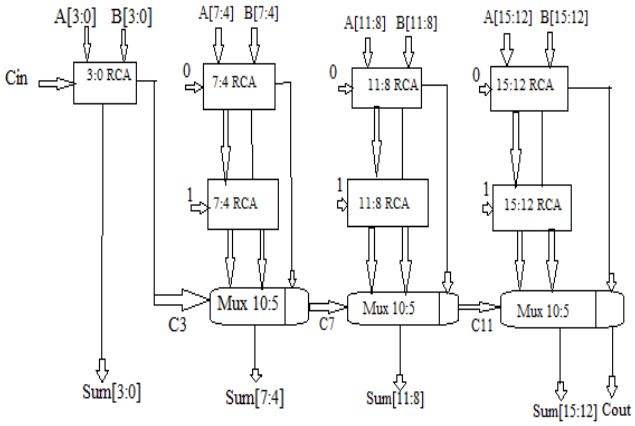

Fig 1: 16-bit CSLA using Ripple Carry Adder

2. DESIGN AN AREA-EFFICIENT CSLA BY SHARING THE CBL TERM
Here the principle used is to replace the RCA at Cin=1 with common Boolean logic (CBL). In CSLA, each part of the adder consists of two RCA with Cin=0 and Cin=1 as N-bit adder is divided into number of parts. According to logic state carry in signal, through multiplexer, it can choose accurate output result. As know that it can compute faster as it do not need to wait for previous stage and summation result is ready and hence in each single bit adder, they get exact computation by only one multiplexer delay. Carry propagation delay be able to decrease by N times in CSLA than RCA. In CSLA, duplicated adder result in larger power consumption and area.

After Boolean simplification, duplicated adder in conventional CSLA can be removed. Correspondly in every single bit adder block duplicate carry out and sum signal can be generated [14]. Here in conventional CSLA, original characteristics of parallel architecture can presented by utilize the multiplexer to choose the precise output according to its preceding carry output signal. Hence circuit area, transistor count and power delay product of the circuit can be decreased to a great extent [14]. These characteristics make it more area efficient and power proficient [3].

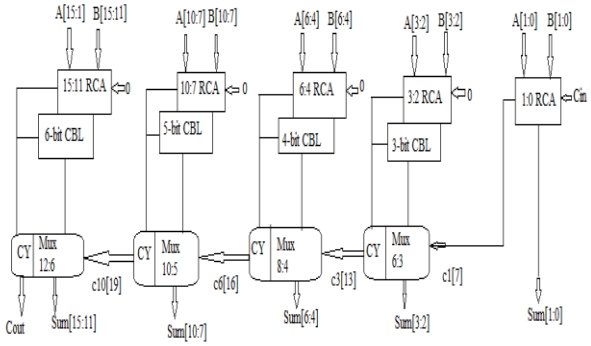

Fig 2: Carry select adder using Common Boolean Logic [3]

3. IMPLEMENTATION OF AN EFFICIENT CSLA BY USING BOOLEAN TO EXCESS-1 CONVERTOR

To eliminate the problem of carry propagation delay, in most of the computational systems, carry select adder is used. From the circuit diagram of carry select adder, it is evident that there is a possibility for reducing the power consumption and area by using a simple and gate level modification.

The principle of it to use the Boolean to excess -1 converter (BEC-1) than using the RCA with Cin=1 as shown in Fig.3 to have lower power consumption and area. The benefit of this BEC logic is the fewer number of logic gates are required than the N-bit CSLA structure and with the reduced number of gates propose the vast advantages in the reduction of power and also in the area [4].

Table 1 Truth Table of the 4-Bit Bec

B[3:0]	X[3:0]
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	1010
1010	1011
1011	1100
1100	1101
1101	1110
1110	1111
1111	0000

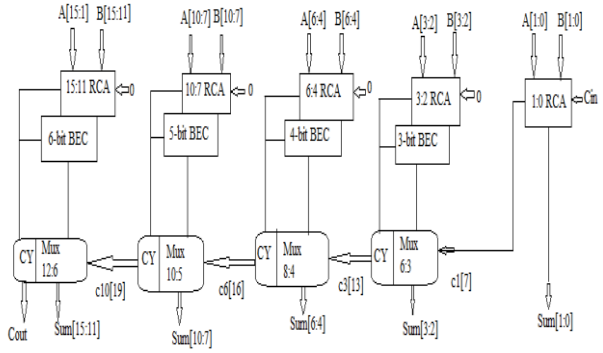

Fig 3: Carry select adder using BEC [4]

4. AREA–DELAY–POWER EFFICIENT CARRY SELECT ADDER USING LOGIC FORMULATION

An efficient logic design for CSLA is derived from the logic formulation. They have analyzed the logic operation involved in the conventional and BEC based CSLAs to study the data dependence and to recognize the redundant logic operations.

To design the new logic formulation for the CSLA, have to eliminate the redundant logic operations from the conventional design of CSLA. In this CSLA design, before the calculation of final sum, the CS operation is scheduled which is different from the conventional approach. The bit-pattern of two anticipating carry words related to Cin='0' and '1' and fixed Cin bits are used for logic optimization of carry selection and carry generation (CG) units. By using these optimized logic units, an efficient design for CSLA is derived [5].

By designing the CSLA in this technique, we get less area and delay than the previous designs. CSLA also becomes the good candidate for the Square root adder due to the small carry output delay Fig.4. This SQRT CSLA consumes 50% less energy than the existing BEC-based CSLA.

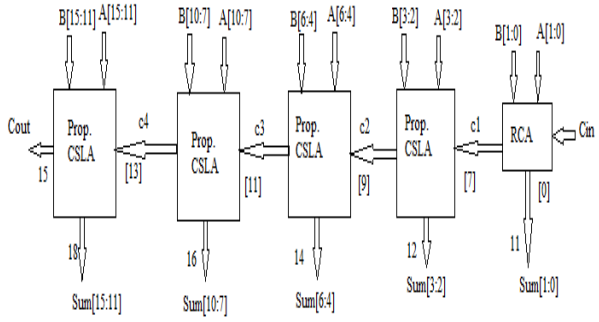

Fig 4: Square root Carry select adder with n=16 [5]

5. IMPLEMENTATION OF AN EFFICIENT CSLA BY USING D-LATCH

Carry select adder is the best and fast adder amongst the conventional adder structures. Because of the rapid rising mobile industry here is not simply the requirement of fast arithmetic logic unit but in addition the less area and low power arithmetic logic units are required .The purpose of designing the CSLA architecture using D-Latch with enable signal in place of the BEC as doing in conventional CSLA,

they achieve three advantages in form of power, area and delay [13].

The CSLA using BEC has reduced power and area with little bit increment in delay but the CSLA architecture using D-Latch reduces the area, power and delay. Latch is used to store the 1-bit information. When the enable signal is applied; the output of latch is continuously affected by their inputs. In the adder, the addition process is done by clock signal. When the clock signal becomes high means '1', addition process for carry input one is perform, whereas the clock signal becomes low means '0' then addition process for carry input zero is performed. The working of the Latch is to accumulate the sum and carry for Cin=1 Fig.4.

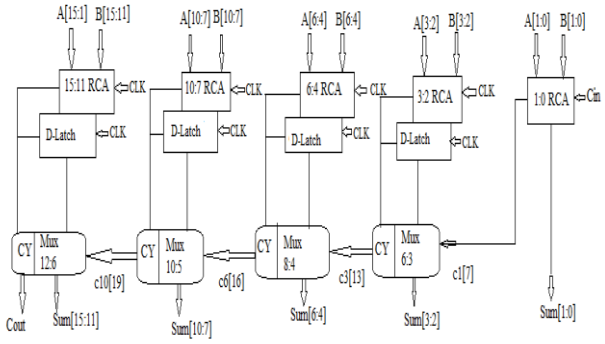

Fig 4: Carry select adder using D-Latch [13]

6. DESIGN OF AN EFFICIENT CSLA BY USING BASIC UNIT

The conventional 16-bit CSLA is made by using the two ripple carry adder cells, each for every 4-bit cells. The first four bits ripple carry adder block add the four bits assuming the carry bit as logic '0' and the other RCA block add the four bits by assuming the carry bit as logic '1'. Depending upon the carry bit from preceding state, the final sum is obtained. In this way delay in increased. So, it replaced the second ripple carry adder block with the basic unit. This basic unit comprises of the incrementer [12].

In this new 16-bit CSLA, only the least significant 4-bits are using conventional ripple carry adder, whereas the other cells are inserted in parallel with the given incrementer. Once the all intervening sums and carries are calculated, the final sums are calculated using multiplexer with minimum delay [15]. Thus the proposed architecture occupied less chip area and also found to consume less power Fig.5.

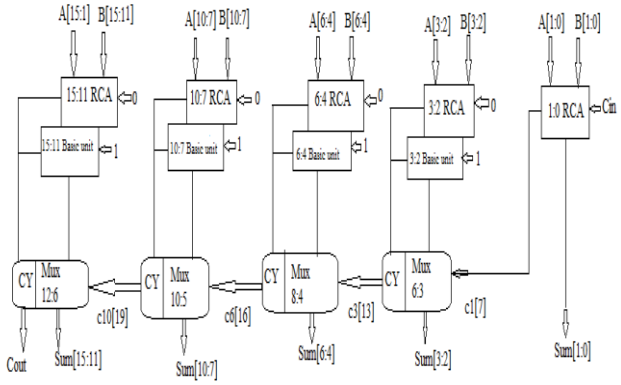

Fig 5: Carry select adder using Basic Unit [12]

7. DIFFERENT LOGIC STYLES FOR CSLA IMPLEMENTATION

A logic style of a circuit influences its speed, power dissipation, size and wiring complexity. Logic style affects the switching capacitance, transistor activity, short circuit current and delay. The circuit design is based on the number of transistors in series, transistor size and wiring capacitance.

Logic styles are of two types. Static logic style and dynamic logic style. In static logic style, each gate output is connected either to Vdd or ground through low resistance path. On the other hand dynamic logic style, each gate output relies on temporary storage of signal value on the capacitance of high impedance circuit nodes [11].

Carry select adder is the design element of any arithmetic unit aiming to achieve lower power consumption, minimum transistor count and high speed. CSLA is designed using three logic styles which as complementary metal oxide semiconductor, Transmission Gate (TG) and Pass Transistor Logic (PTL) these are the static logic styles as given below:

7.1 Complementary Metal Oxide Semiconductor (CMOS)

CMOS logic style is a combination of two networks: the Pull up Network and the Pull down Network. The Pull up Network is comprises of PMOS transistor and the Pull down Network is consists of the NMOS transistor. The function of Pull up Network is to provide the connection between the gate output and the Vdd and we get the high output at gate terminal. The function of Pull down Network is to provide the connection between the gate output and the ground and the output of the gate is low.

The advantages of the CMOS is its strength and vigorous against its voltage scaling and transistor sizing. Because of the complementary transistor pairs, the design of the complementary metal oxide semiconductor is straight-forward and proficient.

7.2 Transmission Gate (TG)

It is an electronic switch that will selectivity block or pass the signal from input to output. It comprises of p-channel PMOS transistor and n-channel NMOS transistor with separate gate connections and common source and drain connection. The control signal is fed to the n-channel transistor gate along with its complement is fed to the p-channel transistor gate but combining the characteristics of p-channel transistor as well as n-channel transistor. It is able to pass logic '1' and logic '0' efficiently without any distortion.

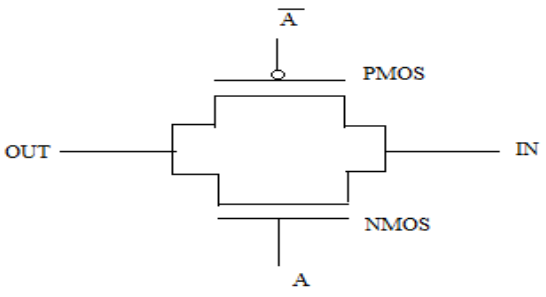

Fig 6: Transmission Gate [11]

7.3 Pass Transistor Logic (PTL)

It tries to minimize the no. of transistor used to implement the logic function. The primary inputs are used to drive the gates of transistors as well as source drain terminals of the MOSFET. The use of minimum no. of the transistor provides lower capacitance. But there is a problem of threshold voltage drop through NMOS transistor logic which necessitates the use of swing restoration logic at the gate output.

The Metal oxide semiconductor networks are linked to variable inputs rather than constant power lines, so only one signal path is active throughout the whole network. These pass transistor multiplexer structure need complementary control signal for that dual rail logic is used. As the result, two MOS networks are required which annihilates the advantage of using low transistor count. Because of their irregular structure, the design of the Pass transistor is not straight-forward and proficient as complementary metal oxide semiconductor.

8. CONCLUSION

The existing carry select adder and its designing method in the VLSI design has been explained. Though these various designing method which explained above are proved to make more proficient carry select adder having less area and lower power utilization than the other adders. Newer modification can focus on achieving more improved area-power-delay carry select adder for data processing processor in very large scale integration design.

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