Implementation of Triangular Carrier based Space Vector Modulation for 3-∅ Bridge Inverter using FPGA

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ABSTRACT
The Space Vector Pulse Width Modulation (SVPWM) is used for three phase bridge Inverter to produce AC output voltage of desired magnitude and frequency. The purpose of controller is to produce regulated output voltage with low distortion under varying load conditions. A triangular carrier based space vector pulse width modulation is developed in MATLAB using Xilinx block set and executed in Field Programmable Gate Array (FPGA). The gate switching pulses required for 3-∅ bridge inverter are generated through FPGA controller which are further amplified to turn on IGBT switches by the use of driver circuit.

Keywords
Field programmable gate arrays (FPGA), triangular carrier based space vector pulse width modulation, current controlled voltage source inverter (CC-VSI)

1. INTRODUCTION
The renewable energy sources used voltage source inverter (VSI) for grid interfacing.The voltage source inverter (VSI) can be controlled either through voltage or current feedback. Current controlledvoltage source inverter (CC-VSI) is preferred due to its intrinsic over current protection characteristics and exceptional dynamic performance.

Conventionally pulse width modulation (PWM) method is used to produce gate pulses for inverter switches to get inverter output voltage. Various PWM techniques have been implemented during the past few decades and details of them can be found in [1]. However, the space vector modulation (SVM) has come into practice with the development of microprocessor technology. The outstanding features of space vector modulation are: can be implemented digitally and a wide linear modulation range for the line-to-line output voltages. SVM has several benefits such as optimum switching pattern, fixed switching frequency, reduced output harmonic spectrum and excellent DC-link voltage utilization [2-5].

The FPGA is mostly used in power electronics applications where input/output is required with fast speed.Control method for generating gate pulses for inverter based on SVPWM is implemented in FPGA in [6-9]. Control methods for multilevel inverter based on FPGA have been implemented by authors in [9, 10]. Various reviewpapers based on control system implementation in FPGA are available [11-13].

This paper is organized as follows. Section 2 briefly introduces the triangular carrier based space vector pulse width modulation method. A detailed description of FPGA is presented in section 3. In section 4, implementation of 3-∅ SVPWM in FPGA is presented and a step by step procedure of executing a bit file in FPGA is discussed. Hardware setup for control strategy implementation is given in section 5 which is an interface between the FPGA and current controlled voltage source inverter. Hardware results are given in Section 6. Section 7concludes the work.

2. TRINGULAR CARRIER BASED SPACE VECTORPULSE WIDTHMODULATION
Instead of using conventional SVM, triangular carrier based SVM is implemented to avoid computational burden. Triangular carrier based pulse width modulation permit efficient and quick implementation of SVPWM in which sector determination is not required. The method is based on the duty ratio cycles that SVPWM displays. The pulses can be generated by comparing the duty ratio profile with a triangular carrier of higher frequency as the case of sinusoidal PWM [14].

In space vector PWM, 3-ph sinusoidal modulating signal get transformed into a revolving voltage vector with a constant magnitude and angular frequency, Here the constant voltage magnitude is magnitude of desire voltage to be produce and angular frequency is the sampling frequency. In space vector based PWM, instead of three modulating signal for 3-phase, a revolving voltage vector is used as a voltage reference. This voltage reference vector is sampled once in every sub-cycle T_s and sampled voltage vector gives the voltage command for the given sub-cycle.

A proper combination of active and zero state vectors are required to estimate a given voltage reference in SVPWM. The equivalence in conventional space vector and triangular comparison based PWM (which is equivalent to space vector PWM) is derived. The value of space vector $\mathbf{U}_{\text{ref}}$ at any time is calculated by time averaging zero vectors and the adjacent two active space vectors. Equivalence in SVM and triangular comparison approach can be derived as explain below from Fig. 1 .The average pole voltages V_{AO}, V_{BO} and V_{CO} can by mathematically expressed by Eq.(1), Eq. (2) and Eq. (3)-

$$V_{AO} = \frac{V_{DC}}{2}\frac{T_1+T_2+T_7}{T_s} - \frac{V_{DC}}{2}\frac{T_0}{T_s} = \frac{V_{DC}}{2V_P}m_A^* \quad (1)$$

$$V_{BO} = \frac{V_{DC}}{2}\frac{T_2+T_7}{T_s} - \frac{V_{DC}}{2}\frac{T_0+T_1}{T_s} = \frac{V_{DC}}{2V_P}m_B^* \quad (2)$$

$$V_{CO} = \frac{V_{DC}}{2}\frac{T_7}{T_s} - \frac{V_{DC}}{2}\frac{T_0+T_1+T_2}{T_s} = -\frac{V_{DC}}{2V_P}m_C^* \quad (3)$$

Here m_A^*, m_B^* and $m_C^*$are equivalent modulating signals of three phases and $\frac{V_{DC}}{2V_P}$ is inverter gain. m_A^*, m_B^* and m_C^* are not sinusoidal but some common mode voltage is added to them. It can be observed that m_A^* is the scaled version of V_{AO} and modulating signal m_B^* and $m_C^*$are phase shifted version of

m_A^*. On comparing m_A^* with falling ramp, the two will intersects at switching instant and again intersection occurs with rising ramp. These intersection points are switching instants which can be used to produce same switching states and same waveform similar to conventional SVM.In the above equations null vector T_0 and T_7 are equal and can be cancelled. The vector sum of voltage vectors are not equal to zero which is given by Eq. (4)-

$$V_{AO} + V_{BO} + V_{CO} \neq 0 \qquad (4)$$

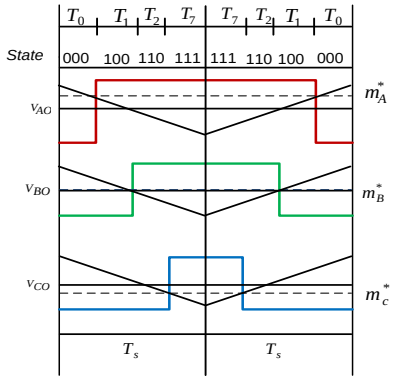

Fig. 1 Triangular approach based space vector modulation

Hence, sum of modulating signal is also not equal is zero as given by Eq. (5).In each phase modulating signal, some common mode voltage is added.

$$m_A^* + m_B^* + m_C^* \neq 0 = 3m_{CM} \qquad (5)$$

This common mode voltage must be calculated to apply triangular carrier based space vector PWM instead of conventional space vector PWM. In triangular carrier, actually null voltage vector states are not equal. To make them equal, further sequence is used to calculate value of m_{CM} from Eq. (6) – Eq. (10)-

$$m_{MAX}^* = m_{MAX} + m_{CM} \qquad (6)$$
$$m_{MID}^* = m_{MID} + m_{CM} \qquad (7)$$
$$m_{MIN}^* = m_{MIN} + m_{CM} \qquad (8)$$

For equal division of null voltage vector time-

$$m_{MAX}^* + m_{MIN}^* = 0 \qquad (9)$$
$$m_{MAX} + m_{MIN} + 2m_{CM} = 0 \qquad (10)$$

Which implies that m_{CM} can be using Eq. (11)

$$m_{CM} = 0.5(\, m_{MAX} + m_{MIN}) \qquad (11)$$

Simulation block, for calculating the value on common mode voltage and further to generate control commands for inverter is shown in Fig.2 –

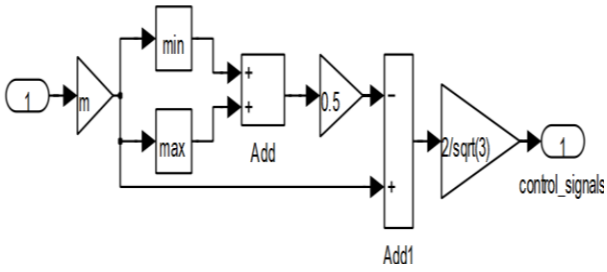

Fig. 2 Control block for calculating common mode voltage

3. DESCRIPTION OF FIELD PROGRAMMABLE GATE ARRAYS (FPGA)

FPGAs have been revolutionized digital signal processing in comparison to ancient processors. FPGAs has many features such as easily upgraded, reusability of codes, compact is size and less consumption of power[15, 16].

FPGAs are consists of three main types of blocks. FPGA board has an array of logic blocks, programmable input output blocks, switches and wires for interconnection. The logic blocks may include lookup tables,tri-state buffers, multiplexers, registers, dual port memories, multipliers, digital clock managers. They are organized in two dimensional arrays with dedicated horizontal and vertical routing channels to interconnect them.These logic blocks are configured to perform various mathematics and logical operations in wide range. The channels which are used for routing are basically wires and programmable switches. They are used to connect logic blocks and I/O devices in number of ways to form systems as per the control of the device configuration bitstream [17-19].

The performance of FPGAcan be derived from the parallel architectures used inside it for processing of data in contrast toDSP or microprocessorwhere the performance depends on the clock rate of the processor. All FPGAs required to be programmed in order to synthesize for a particular digital system.

Fig.3 shows the hardware arrangements of FPGA controller. It components of FPGA controller are CPU, LCD display, the various input output ports to connect the external devices.

Fig. 3 Hardware arrangement of FPGA

4. IMPLEMENTATION OF SVPWM CONTROL STRETEGY USING FPGA

The Xilinx system generator provides the software development platform for implementing triangular carrier based SVM. It has a library called the Xilinx Blockset in MATLAB/Simulink software. Further, software is used to translate model into a hardware realization.

The System Generator maps system parameters (mask variables) declared and defined in Simulink, into objects and architectures, signals and ports, and attributes in a hardware realization. Apart from this, command files are created by System Generator for FPGA synthesis, hardware description language simulation as well as implementation tools. Therefore, user can work exclusively in graphical user interface in process of system specification to hardware

realization [20]. The Xilinx Blockset basic elements library has a block called system generator which controls the generation process. The System Generator parameterization graphical user interface permits the user to select the target FPGA device, clock period of target system, and other implementation choices.

The 3-ØSVPWM method has been used togenerate gate pulse for inverter control. Its performance is tested using FPGA with Altium NB 3000, Xilinx Spartan 3AN processor. Step by step procedure for generating inverter gate pulse is shown in Fig. 4. .XILINX ISE design suite 14.5 is used for model based design for PWM pulse generation for three phase bridge inverter and Altium designer software is used for FPGA project design. Number of steps has been performed for bit file generation using Altium design software. It generates the programming file that is required for downloading the design to the physical device. For detailed study of FPGA project design [1] can be referred.

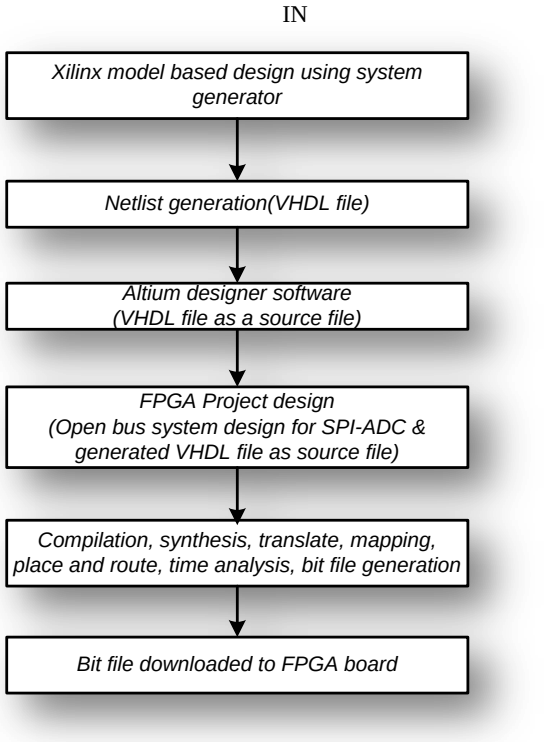

Fig.4 Step by step procedure for hardware realizationusing FPGA

5. SCHEMATIC DIAGRAM FOR HARDWARE SETUP

The implementation of the SVPWM in FPGA requires the translation of the major components which were modeled using MATLAB/Simulink blocks, into hardware mapblocks. Later, these blocks can be simulated on a bit and cycle true basis and then complied into a HDL script. Xilinx System Generator library contains number of such blocks, and these blocks are used to update the architecture of the carrier based SVPWM into the FPGA based model.

Schematic diagram to test SVPWM control method for generating gate pulses using FPGA is shown in Fig.5 is implemented and the real-time results are obtained.

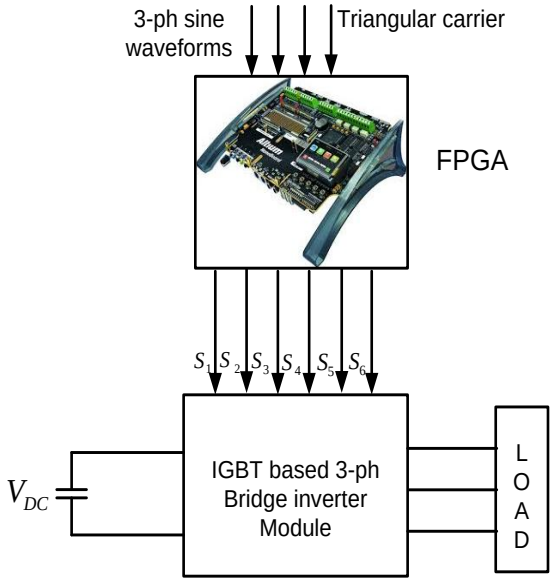

Fig. 5 Schematic diagram for hardware setup

6. RESULTS AND DISCUSSIONS

This section presents the results of experimental work Drawn by XILINX SPARTAN-3AN NB3000 FPGA system for **3-Ø** two level IGBT based bridge inverter. FPGA usually consists of two-dimensional arrays of logic blocks and flip-flops with an electrically programmable interconnection. They can be used to integrate large amounts of configurable logic blocks in a single Integrated Circuit (IC), which is entirely reprogrammable. Here the real time implementation of triangular carrier based SVMcontrol method for 3-Ø bridge inverter using FPGA is carried out. SVPWM control strategy for the inverter is implemented using Xilinx system generator and Altium generator software.From Xilinx integrated library with MATLAB different logic block like MCode, CMult, Relational, AddSub, Gateway In and Gateway are selected and configured to design the control model and HDL netlist is generated from system generator token to implement FPGA project in Altium designer.Fig.6 showing the Xilinx based model of control strategy.Device Utilization Summary for Altium FPGA board is given in Table 1.

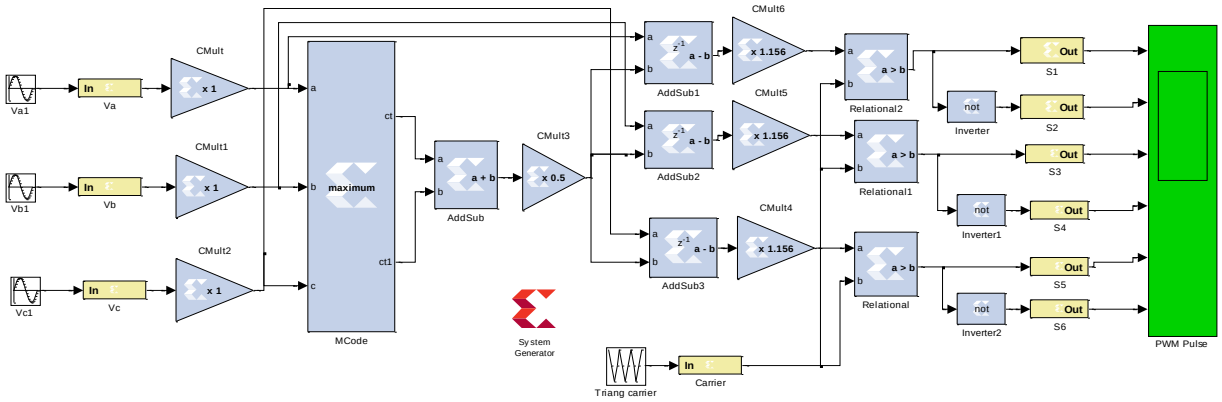

Fig. 6 Xilinx model for implementation of SVPWM

Table.1 Device Utilization Summary for Altium FPGA board

Logic Utilization	Used	Available
Number of Slices	92	11264
Number of Slice Flip Flop	1	22528
Number of 4 input LUTs	177	22528
Number of bonded IOBs	0	502

The gate signal generator model developed using system generator is compiled and converted into bits and is downloaded into FPGA for execution in real time. The generated switching pulses are fed to pulse Amplifiers through the Driver circuit of IGBT Power Module before being applied to the gates of IGBTs of theinverter. Sinusoidal signal and triangular carrier signal of frequency 500 Hz are given as input by ADC-SPI port and inverter gate pulses are obtained by user I/O port which is shown in Fig. 7. It shows gate pulses S1 to S6 from top to bottomrespectively for PWM inverter.

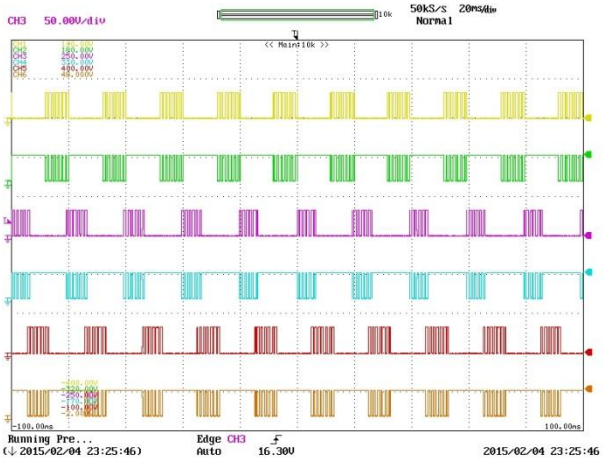

Fig.7 Generation of gate pulses for 3-Ø bridge inverter using FPGA

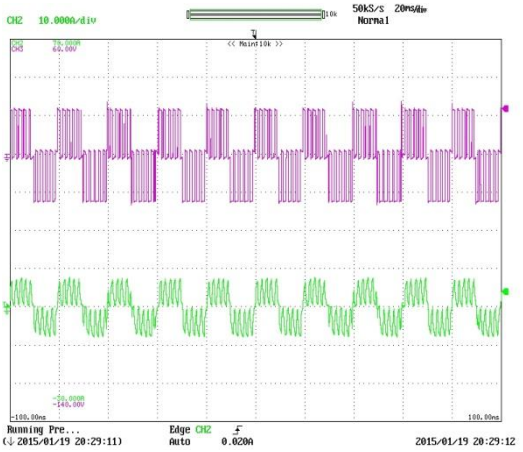

Fig. 8 Load voltage and load current through RL load of phase R

7. CONCLUSIONS

The implementation of triangular carrier based SVM control strategy for three phase PWM inverter has been implemented and the results are shown for linear inductive loads. From results shown above, it is observed that control strategy performs better in view of harmonic content of the steady-state output voltage with linear loads whereas better output voltage is observed under loads with less non-linearity. The reconfiguration logic block is used to design the control model gives the flexibility to improve the performance of inverter driven by the control PWM signal which is executed out from Altium FPGA. The future scope of work is to design the PWM based power controller of inverter where carrier based SVPWM can be used most economical and effectively.

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