Performance Analysis of Magnitude Comparator using Different Design Techniques

Meena Aggarwal
M.E. Student, Department of ECE
NITTTR Chandigarh, India

Rajesh Mehra
Associate Professor,Department of ECE
NITTTR Chandigarh,India

ABSTRACT
Comparators are a basic design module and element in modern digital VLSI design, digital signal processors and data processing application-specific integrated circuits. This paper comprises of design of three different comparators for 2, 4 and 8 bit magnitude comparison. The above said designs are prepared using two different design approaches: Weighted Logic and PTL .The above two design approaches are designed in a way to endow with good quality performance.. The performance of these three different comparators in the two design styles has been compared in terms of area and power consumption which are the important parameters that are considered while designing any digital circuit. The schematic are designed and simulated for its behavior using DSCH-3.1.The layout of simulated circuits are created using Verilog based netlist file which is then simulated in Microwind 3.1 to analyze the performance of comparators for the two design styles at 45nm and 32 nm CMOS technology.

Keywords
ALU, Comparators, CMOS style, Digital Arithmetic, Full Adder module, PTL logic, GDI technique.

1. INTRODUCTION
Comparator is eminent to be a extremely basic and useful component of arithmetic units of the digital systems. In such systems, comparison of any two numbers is said to be a essential arithmetic operation that determine whether a number is greater than, equal to, or less than the other number [1]. Subsequently, comparator is utilized for such operations. Magnitude comparator forms a combinational circuit to compare two numbers, let A and B, and lastly determine their comparative magnitudes and by this means relation between the two(equal to, less than, greater than). Fig.1 depicts the fundamental block of N bit magnitude comparator. The result of comparison is represented by 3 binary variables that indicate whether A>B, A=B, or A<B.

If two n-Bit numbers are to be compared then the circuit will have 2n inputs & 22n entries in the truth table. For 2-Bit numbers there shall be 4-inputs & 16-rows in the truth table, similarly, for 3-Bit numbers the truth table would comprise of 6-inputs & 64-rows [2].Figure 1 shows the block diagram of n-bit magnitude comparator.

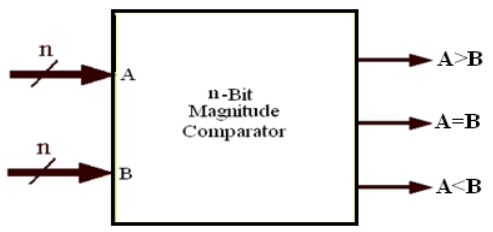

Figure 1: Block Diagram of n-Bit Magnitude Comparator

2. TWO- BIT COMPARATOR
2-Bit Magnitude Comparator is intended to compare two numbers each having two bits (let A1, A0 & B1,B0). Therefore, for such an arrangement, truth table [3] shall have 4 inputs & 16 entries as in Table 1.

Table 1: Truth Table of 2-Bit Magnitude Comparator

INPUT				OUTPUT		
A1	**A0**	**B1**	**B0**	**A>B**	**A=B**	**A<B**
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

3. DESIGN APPROACHES
There are numerous approaches which will be useful in designing CMOS comparators. Each scheme will put forward different operating speed, power consumption, and circuit complexity.

The size of the circuit depends on the number and size of the transistors and also on the wiring density. The wiring complexity is a function of number of connections and their

lengths. All the said parameters may vary noticeably from one logic style to another and for that reason proper choice of logic style is very important for desirable circuit performance . The main principle of all the design styles and modifications is to bring down the number of transistors to be used to perform the desired logic, lessen the power consumption and attain an increased speed. One of the major return of using lesser number of transistors is to put more devices on a single silicon chip which further brings drop in total area.

4. COMPARATOR LOGIC STYLES

The work presented herein is focused on basic two styles of design which are as under :

a. Weighted Logic b. PTL Logic

4.1 Weighted Logic

The approach of weighted bit logic is mostly employed to proficiently execute arithmetic blocks eliminating the overhead delay caused by designing on the gate level. This is achieved by integration of many stages onto one stage and all these were individually meant to differentiate between bit orders . The structural design of the new logic is shown in Fig. 1 depicting a two bit comparator. It is formed of a pre-calculation stage which is followed by a combining stage. Pre-calculation blocks are designed in such a way that they depict the type of functionality a designer seek to implement while combining blocks account for the order of the bits.

Pre-calculation stage: The logic execution is constituted in a way to guarantee that the outputs of the upper pre-calculation block (O/P1, O/P2) estimate to (1, 01). An output (0,1) will not be evaluated. This can be achieved by checking the truth table of pre- calculation stage 1 shown below in Table 1. Comparable observations relate pre-calculation block 2. The underlying principle behind (0, 1) from the output of the pre-calculation block is that this combination is fed to the combining block and it results in a short circuit thereby connecting the Vdd to the ground which further produces power loss. When the input is (1, 1) , a degraded voltage O/P1 and the same happens for O/P2 when the input is (0,0). The voltages are restored using a level restorer circuit [4].

Combining stage: In order to explain the functionality of this block, we look at 3 different cases (A>B, A<B and A=B). When the case is of unequal inputs, then the inequality output evaluates '1' and '0' in the cases of A<B and A>B, respectively, for correct functionality while the equality output is high. On the other hand, in case of equality A=B the equality output is low irrespective of the inequality output.

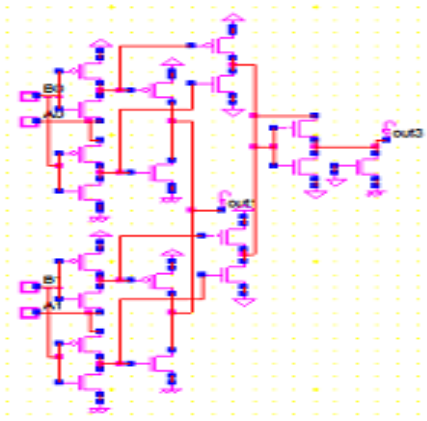

Figure 2: 2-Bit comparator using Weighted Logic

The circuit diagram of a 2-bit comparator which has been designed using weighted logic is shown in figure 2. Similarly, 4-bit and 8-bit comparators have also been designed using the same design approach.

Table 2: Truth Table of Pre-calculation Stage[5]

A0	B0	O/P1	O/P2
0	0	1	0
0	1	0	0
1	0	1	1
1	1	1	0

4.2 PTL logic

Chief edge of Pass Transistor Logic is to use purely NMOS Pass Transistors network for any logic operation. The fundamental variation of pass-transistor logic style and the CMOS logic style is that the source of the logic transistor networks is connected to some input signals instead of the power lines as shown in Figure 3. In this design approach, transistor acts as a switch and thereby passes logic levels from input to the output [2].Such a design approach requires lesser number of transistors because one pass-transistor network (either NMOS or PMOS) is sufficient to perform any logic operation. Lesser number of transistors result in increased speed .

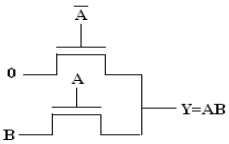

Figure 3: Symbol for AND Gate using PTL

The circuit diagram of 2-bit magnitude comparator using PTL logic is shown in below Figure 4.

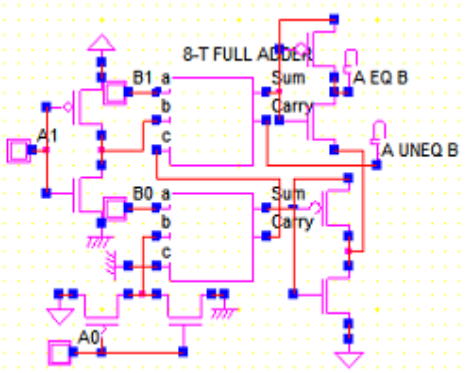

Figure 4: 2-Bit comparator using PTL

5. RESULTS AND ANALYSIS

The performance of above mentioned diverse logic styles based 2, 4 and 8 bit magnitude comparator has been evaluated in terms of area and power on 45nm and 90nm CMOS technology by using BSIM Level -4 model for different supply voltages. Simulation of various schematics drawn in DSCH-3.1 has been done in Microwind3.1. The results of simulation are shown in Table-3 and Table-4.

Table 3: Simulation results for 45nm Technology

Parameters	PTL			Weighted Logic		
Comparator	**2 bit**	**4bit**	**8 bit**	**2 bit**	**4 bit**	**8 bit**
Transistor Count	24	58	126	19	35	89
Widhth(µm)	20.3	48.3	50.8	16.1	29.3	50.8
Height(µm)	6.0	7.9	23.0	5.4	6.8	17.8
Surface(µm)	120.5	380.4	1167.8	87.1	198.7	902.5
Power(µW)	2.423	3.003	25.748	5.822	7.119	46.748

The results shown in above table which is obtained by simulating the 2,4 and 8-bit comparator in Microwind 3.1 at 45nm technology that weighted logic uses less number of transistors as compare to pass transistor logic (PTL) whereas power dissipation of weighted logic is approximately twice to that of PTL.

Table 4: Simulation results for 32nm Technology

Parameters	PTL			Weighted Logic		
Comparator	**2 bit**	**4bit**	**8 bit**	**2 bit**	**4 bit**	**8 bit**
Transistor Count	24	58	126	19	35	89
Widhth (µm)	16.2	38.6	40.6	14.9	26.1	40.6
Height(µm)	4.8	6.3	18.4	4.3	5.4	14.2
Surface(μm^2)	77.1	243.4	747.4	64.3	141.5	577.6
Power(µW)	4.417	4.180	26.381	7.551	8.508	62.909

This table shows the comparison of two logic styles in terms of area at fixed input supply voltage operating at same temperature of 27^0C in tabular form.It is analyzed that the result will be different for different technology i.e. the area consumption will vary by changing the technology of same circuit and also vary by using different logic style.It is observed from the above table that weighted logic based comparator has less area consumption as compared to PTL style for both 45nm and 32nm technology. Finally the analog simulation of various layout at different technologies has been done in Microwind 3.1. to obtain the power consumption at different supply voltage which is also shown in above Tables.

From these table, it is observed that power dissipation is less in case of PTL logic as compare to weighted logic. But when the comparison is done between two different technologies i.e, 32nm and 45nm then it is found that 32nm will show better results in terms of area for both style whereas PTL is better in terms of power consumption .It can also be seen that weighted logic style comparator uses less number of transistors

6. CONCLUSION

The final results in terms of transistor count and power consumption have been obtained by simulating both logic styles at 45nm and 32nm technology. It is observed that for the implementation of Pass Transistor Logic, the total number of 24 transistor have been utilized while weighted logic uses 19 transistor. Thereby, it is observed that weighted logic offers area and power efficient approach for the design of comparator. The simulation results have been obtained on BSIM LEVEL-4 model.

7. REFRENCES

[1] Morgenshtein, A., Fish A., Wagner, I.A., "Gate-diffusion input (GDI): A Power Efficient Method for Digital Combinational circuits," IEEE Transaction on Very Large Scale Integration (VLSI) Systems, Vol. 10 , No. 5 , pp. 566 - 581 , 2002.

[2] Anjuli and Satyajit Anand," 2- Bit Magnitude Comparator design using different logic styles," International Journal of Engineering Science Invention , Vol. 2 ,No. 1, pp.13-24, 2013.

[3] Vandana Choudhary, Rajesh Mehra, " 2-bit CMOS compartor by Hybridizing PTL and Pseudo logic," International Journal of Recent Technology and Engineering, Vol.2, No. 2, pp. 29-31,2013.

[4] Ahmed Magdy and Mohab Anis, " High Performance Energy-Efficient Arithmetic Circuits using Weighted Logic," 8th IEEE International New Circuits and Systems conference, pp. 57-60, 2010.

[5] N.Weste and D.Harris, CMOS VLSI Design: A Circuits and System Perspective, 3rd ed. Reading, MA, USA: Addison-Wesley , May 2004.

[6] H.-.M.Lam and C.-Y. Tsui, "A MUX-based high-performance single-cycle CMOS comparator," IEEE Transaction on Circuits System II, Vol.54, No.7, pp.591-595, 2007.

[7] Chiou-Kou Tung; Yu-Cherng Hung; Shao-Hui Shieh; Guo-Shing Huang, " A Low -Power High-speed Hybrid CMOS Full Adder For Embedded System," IEEE Transaction on Design and Diagnostics of Electronic Circuits and Systems, Vol.13, No.6, pp.1- 4, 2007.

[8] Geetanjali Sharma, Uma Nirmal, Yogesh Mishra, "A Low Power 8-bit Magnitude Comparator With Small Transistor Count using Hybrid PTL/CMOS Logic," International Journal of Computational Engineering & Management, Vol. 2, No. 2, pp.110-115, 2011.

[9] Manoj Kumar, Sandeep K. Arya1, and Sujata Pandey, " Single bit full adder design using 8 transistors with novel 3 transistors XNOR gate," International Journal of VLSI design & Communication Systems, Vol. 2, No. 4, pp. 47-59, 2011.

[10] Anjali Sharma, Richa Singh, Rajesh Mehra, Member, IEEE, "Low Power TG Full Adder Design Using CMOS Nano Technology," IEEE International Conference on Parallel, Distributed and Grid Computing, pp. 210-213, 2012.

[11] Subodh Wairya, Rajendra Kumar Nagaria ,Sudarshan Tiwari, "Comparative Performance Analysis of XOR/XNOR Function Based High-Speed CMOS Full Adder Circuits For Low Voltage VLSI Design," International Journal Of VLSI Design & Communication System,Vol.3, No.2, pp. 221-242, 2012.

[12] Vandana Dubey, O.P.Singh, G.R.Mishra, " Design and Implementation of a Two-Bit Binary Comparator Using

Reversible Logic," International Journal of Scientific and Research Publications, Vol. 2, No. 7, pp. 1-4, 2012.

[13] Laxmi Kumre, Ajay Somkuwar, Ganga Agnihotri, "Design of Low Power 8 bit GDI Magnitude Comparator," International Journal of Emerging Technologies in Computational and Applied Sciences (IJETCAS),Vol.4, pp.102-108, 2013.

[14] Anjali Sharma, Richa Singh, Pankaj Kajla , " Area Efficient 1-bit comparator Design by using Hybridized Full Adder Module based on PTL and GDI logic," International Journal of Computer Applications, Vol.82, No.10, pp. 5-13, 2013.

[15] Anjali Sharma, Rajesh Mehra, "Area and Power Efficient CMOS Adder Design by Hybridizing PTL and GDI Technique," International Journal of Computer Applications, Vol.66, No. 4, pp. 15-22, 2013.

[16] Arkadiy Morgenshtein ,Viacheslav Yuzhaninov, Alexey Kovshilovsky, Alexander Fish, "Full-swing Gate Diffusion input logic," Integration, the VLSI Journal, Vol.47, pp. 62-70, 2014.

[17] Pooja Singh , Rajesh Mehra, "Design Analysis of XOR Gates Using CMOS & Pass Transistor Logic," National Student Conference on Advances in Electrical & Information Communication Technology, AEICT-2014, pp.264-267, 2014.

[18] K.Rajasekhar, P.Sowjanya, V.Umakiranmai, R.Harish, M.Krishna , "Design and Analysis of comparator using different logic style of full adder," International journal of Engineering Research and Applications,Vol.4, No.4, pp .389-393, 2014.

[19] Sharma.A, Sharma.P, "Area and power efficient 4-bit comparator design by using 1-bit full adder module," IEEE conference on Parallel, Distributed and Grid Computing, pp. 1-6, 2014.

[20] Microwind and DSCH version 3.1, User's Manual, Copyright 1997-2007, Microwind INSA France.