Design and Verification of Reversible Logic Gates using Quantum Dot Cellular Automata

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ABSTRACT
This paper portrays the designing of Reversible Logic gates through the use of Quantum Dot Cellular Automata (QCA) which is a nanotechnology concept and also a striking substitute for transistor based technologies. This technology helps us to rise above the confines of CMOS technology. It also gives better results in terms of digital and analog waveform, Quantum cost, garbage output. The fundamental logic in QCA is the logic state that does not compute with voltage level; rather it measures the polarity of electrons in a quantum cell. Basically Reversible logic gates are an essential building block of various computing system. Comparing with standard gates, the reversible logic gate lower the information bits use loss by reusing the logic information bits logically and realizes the goal of lowering power consumption of logic circuits. A QCAdesigner tool is used for simulation of different kinds of Reversible logic gates such as Toffoli gate, Fredkin gate and some others.

Keywords
QCA, Reversible gates, Majority gate, clock, NANO-Technology

1. INTRODUCTION
As it seems to be a major concern of energy dissipation with the increment in the circuit complexity. Some portion of energy is from real time switching elements while some are from every irreversible bit operation which is depicted as KTln2, which was negligible for multi-billion incoming electrons passing through various gates [1]. This trouncing of energy can be diminished through the application of reversibility principle on digital circuits and it enables the circuit functioning with a minute fraction of energy [5]. Therefore, this reversible computing concept act as energy solution to many budding fields of nanotechnology in relation to quantum computing [1]. The gates which agree to regeneration of inputs from the detected outputs are the reversible logic gates. It has same number of input and output lines whereas the output line which was not utilize in any circuit was considered to be a garbage signal and the fan-out of each output line is one [2].

The aim behind reversible computing is the storage cells having electric charge with the transistor in it and not allows emerging out when the switching operation actively performed in transistor. Then it will be capable of use again through reversible computing, which ultimately lowered down the energy utilization with not any loss of digital data bits and such systems are known as reversible systems [3]. As logic is designed to be reversible but the cause of this act that information must not be wipe out. This concludes that general gates like "AND" and "OR" cannot be implemented through reversibility as multiple inputs bring down to a single output which was not in accordance to a reversibility concept as there is loss of information. The circuits with extremely less power consumption and doesn't need any sort of regular interconnections are an advantage [7].

This paper focuses upon the various architectures of reversible gates designed in QCADesigner tool with their graphical output waveforms while logic verification through the traditional truth table based methods.

2. REVERSIBLE LOGIC GATES
A circuit is said to be reversible if the input vector can be uniquely recovered from the output vector and there is a one to one correspondence between its input and output vectors, i.e. not only the outputs can be uniquely determined from the inputs and vice versa[8]. Thus the number of inputs and outputs in reversible gates are equal. Any arithmetic logic unit [6] must be able to produce a variety of logic outputs based on inputs determined by the programmer for implementation in an instruction set architecture. Therefore, reversible logic devices used in an environment must have both fixed select input lines that receive op-code signals manipulated by the programmer and permanent output lines where the result of the logical output is produced [3].

For an n input/output logic gate, if there is a one-to-one correspondence between its inputs and outputs, then this logic gate is reversible. The subsequent expressions are [8]:

$$I_v = I_{(n-1)!} \quad (1)$$

$$O_v = O_{(n-1)!} \quad (2)$$

Where the I_v is input vector and O_v is the output vector. That is to say, a reversible gate has the same number of inputs and outputs. Commonly used reversible gates are NOT gate, CNOT gate, CCNOT gate (Toffoli gate), Peres gate, Fredkin gate, Feynman gate [9].

2.1 Feynman gate
It is a 2*2 reversible gate with I_v= (A, B) and O_v= (P, Q) where I_v and O_v are the input and output vectors respectively. Quantum cost of Feynman gate is 1.

Fig. 1. Block diagram of feynman gate [3]

2.2 Toffoli Gate
It is a 3*3 gate with inputs (A, B, C) and outputs (P, Q, R) where P=A, Q=B and R=AB XOR C. It has quantum cost 4.

Fig. 2. Block diagram of Toffoli gate [3]

2.3 Fredkin Gate

It is a 3*3 gate with inputs (A, B, C) and outputs (P, Q, R) where P=A, Q=A'B+AC, R=AB+A'C having quantum cost 4.

Fig. 3. Block diagram of Fredkin gate [3]

2.4 Peres Gate

It is a 3*3 gate having inputs (A, B, C) and outputs (P, Q, R) where P= A; Q = A XOR B; R = AB XOR C. It has Quantum cost four.

Fig. 4. Block diagram of Peres gate [3]

3. QCA DESIGN OF REVERSIBLE GATES

3.1 Feynman Gate

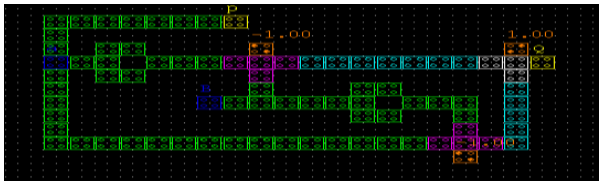

Fig. 5. QCA based Feynman gate

This gate is designed with two inverters, two AND gate and one OR gate.

3.2 Toffoli Gate

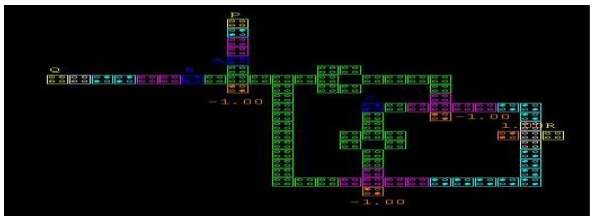

Fig. 6. QCA based Toffoli gate

This gate is designed with two inverters, two AND gates and one OR gate.

3.3 Fredkin Gate

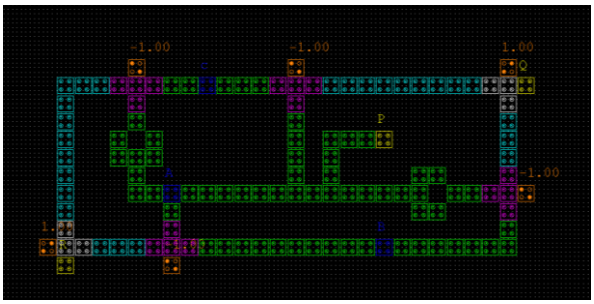

Fig. 7. QCA based Fredkin gate

This gate is designed with two inverters, four AND gates and two OR gates.

3.4 Peres gate

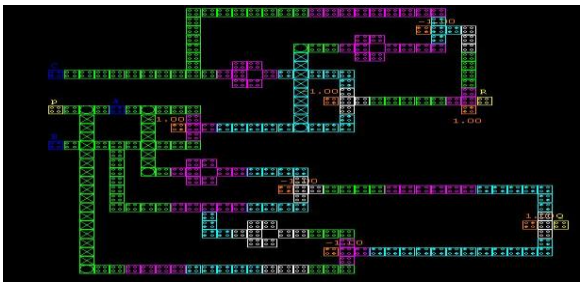

Fig. 8. QCA based Peres gate

This gate is designed with four inverters, five AND gates and two OR gates

4. RESULT VERIFICATION

The result has been verified by comparing the graphical result obtained from QCADesigner tool with the truth table of these Reversible logic gates.

4.1 Feynman Gate

Table 1. Truth Table for Feynman gate

Input		Output	
A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

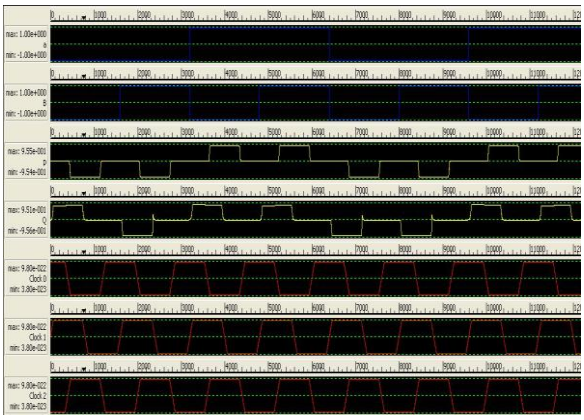

Fig 9. QCA output of Feynman gate

4.2 Toffoli Gate

Table 2. Truth table for Toffoli gate

Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0

1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

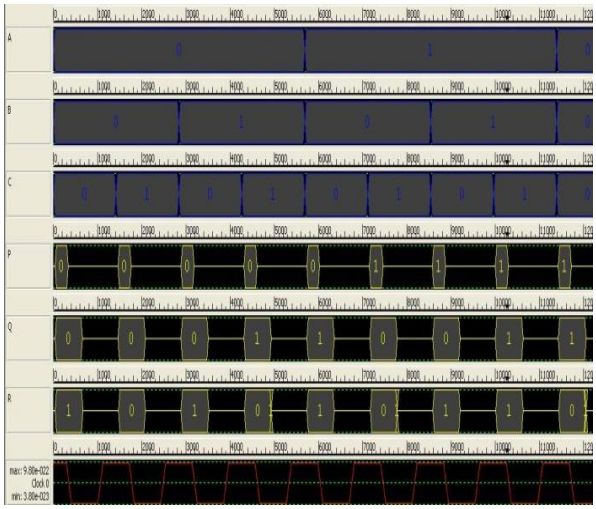

Fig. 10. QCA output of Toffoli gate

4.3 Fredkin Gate

Table 3. Truth Table for Fredkin Gate

Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

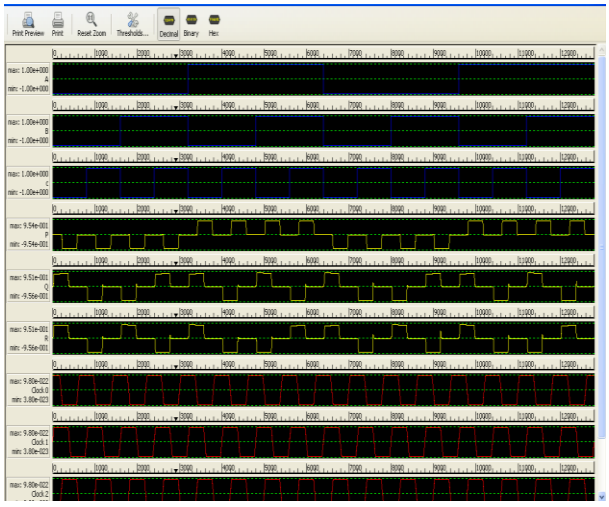

Fig. 11. QCA output of Fredkin gate

4.4 Peres Gate

Table 4. Truth Table for Peres Gate

Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

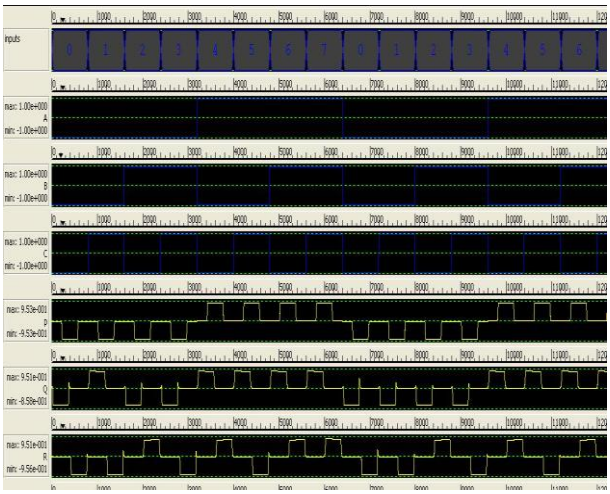

Fig. 12. QCA output of Peres gate

5. HALF ADDER

A Half adder has been designed using reversible logic gates namely Feynman and Fredkin gate.

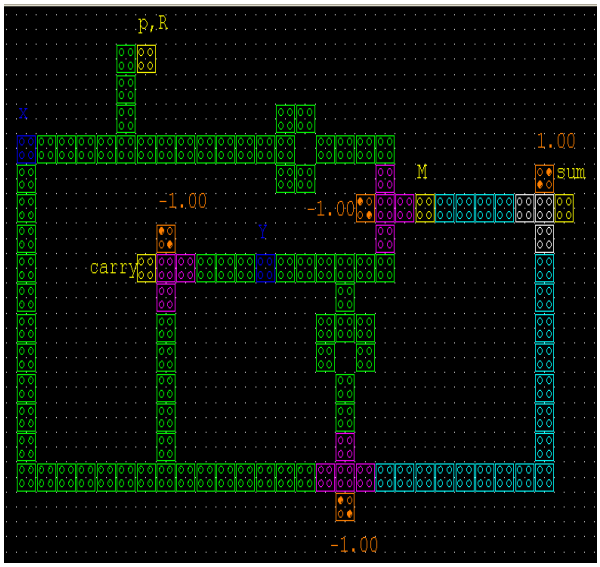

Fig. 13. QCA layout of Half-Adder

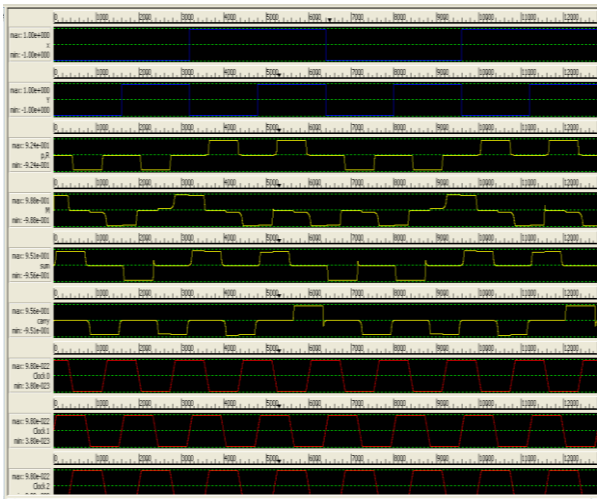

Fig. 14. QCA output of Half-Adder

6. CONCLUSION

The reversible circuits form the basic building block of quantum computers. Here, the primitive reversible gates which are gathered from literature and it helps researches/designers in designing circuits using reversible gates. Although reversible logic gates needs more cell count as compared to regular gates designed in QCA. The fundamental reversible logic gates has been tested and verified on the QCA Designer tool with minimum delay latency. Also it has wide scope in the fields of DNA computing, Digital signal processor and nano based bio-information services.

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8. REFERENCES

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