High Performance Design Techniques of Transimpedance Amplifier

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ABSTRACT
This paper hearsay on various design approach of transimpedance amplifier (TIA) that improves the performance along various parameters such as gain, noise, speed and bandwidth. Transimpedance amplifier design overcomes the drawbacks of high impedance amplifier design. Gain boost up can be done by using PMOS current source at the input stage. Capacitive coupling and cross coupled current conveyor stage trim down input noise and get better the speed of transimpedance amplifier.

Keywords
Transimpedance amplifier, noise, gain, bandwidth enhancement, cross coupled current conveyor, voltage headroom.

1. INTRODUCTION
The light travelling through a fiber experiences loss before reaching a photodiode at the far end. The photodiode then transforms the light intensity to a proportional current which is subsequently simplified and converted to a voltage by transimpedance amplifier [5]. TIA is extensively exploited as the front end of the optical communication receiver. Traditionally, such front end circuits and devices are heavily dependent on III/V technologies due to their speed and noise advantages. However the demand for high volume and wide development of optical components in recent years makes silicon based integrated circuits most economical solution [1]. CMOS process technology gives low power, low cost and high yield which offers the most economical solution in the consumer application market [3]. Transimpedance amplifier typically determines the overall optical link performance, as their speed and sensitivity set the maximum data rate and tolerable channel loss [2]. The design of wide band TIA is the challenging mainly because it is driven by a photo detector with high capacitance usually ranging from 0.2 to 0.5 pF [4]. The specification requirements of a typical TIA are large bandwidth, high transimpedance gain, low noise, low power consumption, and small group delay variation [6]. Among these designing parameters, large bandwidth is critical to achieve broadband data transmission link. Hence, methods for bandwidth enhancement are reported constantly [3]. The major bandwidth restriction of a conventional TIA is usually at the input node due to the large capacitive load introduced by preceding photodiode. To capture sufficient optical power, large area

photodiode is evitable, bringing large junction capacitance. Various CMOS TIA architectures have been reported that essentially explore different input stages for isolating the large input capacitance of the photodiode from bandwidth determination, such as common gate (CG) input stage [2], regular cascade (RGC) stage [2], [9], or CG feed forward topology containing negative feedback [2]. Other bandwidth enhancement techniques, such as inductive peaking [3] and capacitive degeneration [9], are also implemented. However, the bandwidth of all reported TIAs reduces with increasing photodiode's capacitance.

2. PERFORMANCE TECHNIQUES
2.1 Gain Boosting
The transimpedance gain of TIA must be large enough to overcome the noise of the subsequent stage. The traditional common gate stage or feedback TIA having low supply voltages impose a small dc voltage drop across the load resister in the input stage their by limiting the gain and yielding a high input referred noise. In CMOS technology it is possible to add a PMOS current source in parallel with drain resister. Thus providing port of the bias current for common gate or feedback TIA [5].

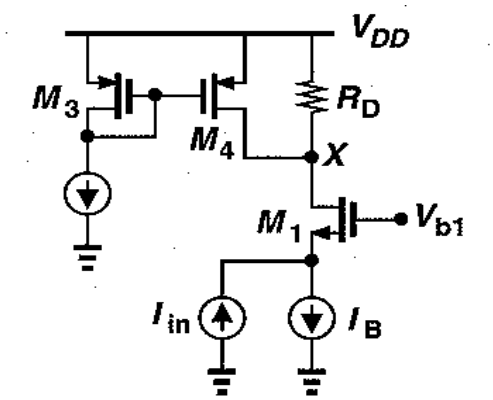

Fig 1: PMOS current source to CG stage

2.2 Capacitive Coupling
The source follower in capacitive TIA constrains the voltage headroom considerably. A possible remedy is to employ capacitive coupling there by isolating the dc levels. Input stage is coupled to source follower through coupling capacitor and the bias voltage of M2 at VDD through RB . RD can sustain a greater voltage drop to sustain noise [5].

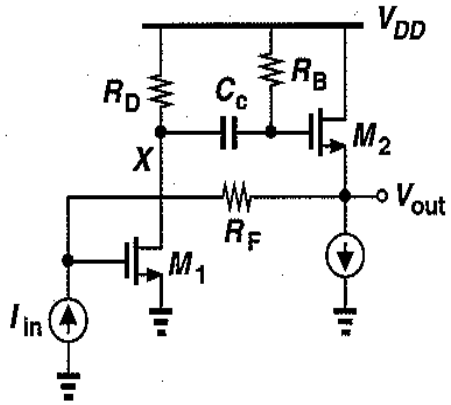

Fig 2: Capacitive coupling in feedback TIA

2.3 Regulated Cascade Stage

The RGC input stage is well suited for broad-band TIA design by its very low input impedance [3],

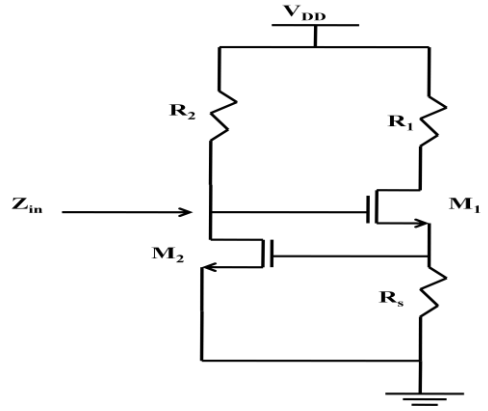

Fig 3: RCG stage

This very small input impedance in large part isolates the photodiode capacitance from bandwidth determination and therefore, unlike common gate or common source TIAs, the dominant pole of an RGC TIA is usually located within the amplifier rather than at the input node [3].

2.4 Capacitive Degeneration

Besides pushing the dominant pole to higher frequencies to increase the bandwidth, it is also possible to compensate the dominant pole with a zero, which could be accomplished by capacitive degeneration. The zero could be used to compensate the dominant pole of the circuit. The 3-dB cutoff frequency is therefore determined by the second lowest pole of the circuit.[3] The zero introduced by the capacitive degeneration stage is then to satisfy the following equation:

$$z = \frac{1}{2\pi R_S C_S} = \mathrm{f}$$

Besides the zero, this capacitive degeneration stage also brings an additional pole at

$$\mathrm{f_s} = \frac{1 + \mathrm{g_m R_S}}{2\pi R_S C_s}$$

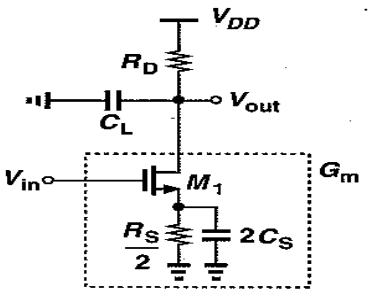

Fig 4: Capacitive Degeneration stage

2.5 Inductive Peaking

Inductive peaking is to allow the capacitance that limits the bandwidth to resonate with an inductor thereby improving the speed. With an input signal inductor initially serve as an open circuit allows all of the current to flow through the capacitor rather than the resister, results that output voltage changes faster [5].

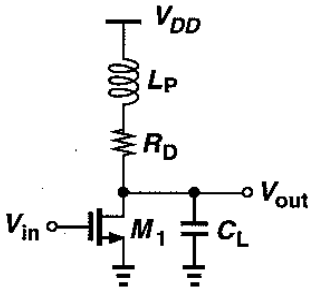

Fig 5: CS stage with inductive peaking

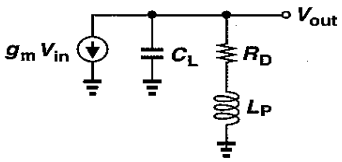

Fig 6: Small signal model

If the inductor value is excessively large then Vout experiences overshoot before settling. Therefore determine the amount of overshoot [5].

$$-\mathrm{g_m V_{in}} = \mathrm{V_{out}}\ \mathrm{C_L S} + \frac{\mathrm{V_{out}}}{\mathrm{L_P S + R_D}}$$

$$\frac{V_{out}}{V_{in}} = -\mathrm{g_m}\ \frac{\mathrm{L_P\, S + R_D}}{\mathrm{L_P C_L S^2 + R_D\, C_L\, S + 1}}\ \frac{\omega_\mathrm{n}}{2\zeta}$$

$$= -\mathrm{g_m\, R_D}\ \frac{\mathrm{S} + 2\zeta\omega_\mathrm{n}}{\mathrm{S^2} + 2\zeta\omega_\mathrm{n}\,\mathrm{S} + \omega^2{}_\mathrm{n}}$$

Where, $\zeta = (\mathrm{R_D}/2)\sqrt{\mathrm{C_L}/\mathrm{L_P}}$ and $\omega^2{}_n = (\mathrm{L_P C_L})^{-1}$

Series inductive peaking is another technique for extending TIA band width. An inductor can be interposed between a photodiode and the input of a transimpedance amplifier so as to increase the bandwidth [2].

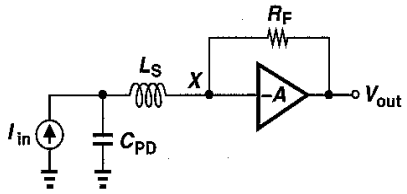

Fig 7: Series inductive peaking

$$\left[\frac{-V_{out}}{A} - \left(V_{out} + \frac{V_{out}}{A}\right)\frac{L_S\,S}{R_F}\right] C_{PD}\,S$$

$$= I_{in} + \left(V_{out} + \frac{V_{out}}{A}\right)\frac{1}{R_F}$$

$$\frac{V_{out}}{I_{in}} = \frac{-1}{S^2 + \frac{R_F}{(A+1)L_S}S + \frac{1}{C_{PD}\,L_S}} \frac{AR_F}{(A+1)C_{PD}\,L_S}$$

$$\omega^2{}_{-3db} \approx \frac{\sqrt{2}\,A}{R_F\,C_{PD}}$$

Thereby increasing the bandwidth by approximately 41% with and overshoot of 4.3% [5].

2.6 Cross Coupled Current Conveyor Stage

A new technique to offset the large junction capacitance brought by photodiode. It is achieved by "creating""zero differential impedance" at the input node of a TIA. This input stage is based on a cross-coupled current conveyor structure [6]. It provides a stable performance over a wide range capacitive load. Cross coupled structure also brings a huge improvement in noise performance [3].

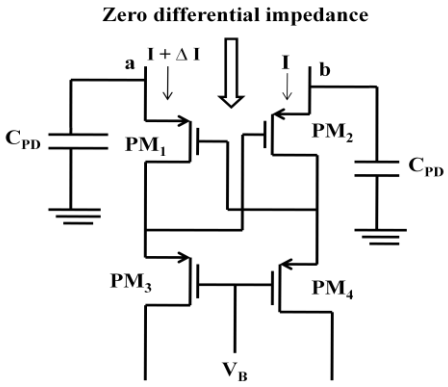

Fig 8: Current Conveyor Stage

When the four PMOS PM1, PM2, PM3, and PM4 are in saturation region, ideally

$$V_{sg}\,1 = V_{sg}\,3 = V1 \text{ and } V_{sg}\,2 = V_{sg}\,4 = V2$$

Suppose the bias voltage VB is 0-V first, the voltage at node a, Va and the voltage at node b, Vb are

$$Va = V_{sg}\,1 + V_{sg}\,4 = V1 + V2$$

$$Vb = V_{sg}\,2 + V_{sg}\,3 = V2 + V1$$

Thus

$$Va = Vb$$

Thus, no matter how large the current difference between node a and b is, ΔZ will be zero, which is independent of Δi and the parasitic capacitance of the four transistors. If the same capacitors with capacitance CPD are added to nodes a, b, respectively, ΔZ will still be zero since Va = Vb. This unique property of cross-coupled PMOS current conveyor is referred as "zero differential impedance."[3]

2.7 Automatic Gain Control

Optical receivers may experience vastly different input current because the transmitted laser power, the length and hence loss of the fiber, and the effiency of the photodiode may vary from one link to another. Thus transimpedance amplifier may accommodate relatively wide dynamic range, typically from a few microamperes to few milliamperes.

Overloading problems appears for large input currents and high speed operation. To overcome the problem of overloading automatic gain control stage is used. AGC can simply utilize the dc content of the output as amesure of input swing. [5]

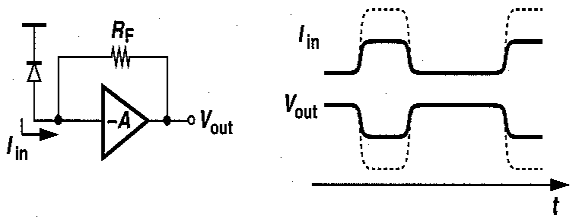

Fig 9: Conceptual illustration of AGC

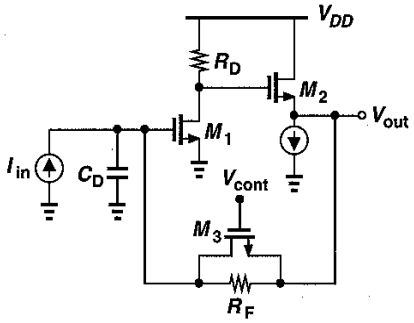

Fig 10: AGC in feedback TIA

In feedback TIAs the transimpedance gain is nearly equal to the feedback resistor. NMOS device is placed in parallel with RF lower the gain as Vcont becomes more positive. This is the most common approach to gain control. [5]

Table 1. Literature Survey

Title	Broad- band design techniques for transimpedan ce	Extension in shunt feedback transimpedanc e amplifier using negative miller	CMOS wideband amplifiers using multiple inductive-series peaking	Bandwidth enhancement with low group delay variation for a 40-Gb/s transimpedance	Cross coupled current Conveyor based CMOS transimpedance amplifier for broad band data

	amplifiers.	capacitance	technique	amplifier	transmission
Publication	IEEE Trans. Circuit Syst. I, Reg. Papers, vol. 54, no. 3, pp. 59 600, Mar	Proc. IEEE Int. Symp. Circuit Syst	IEEE J. Solid-State Circuits, vol. 40, no. 2, pp. 548–552	IEEE Trans.Circuits Syst. I, Reg. Papers, vol. 57, no. 8, pp. 1964–1972	IEEE transaction on very large scale integration (VLSI) systems, vol 21, No.8
Year	Mar. 2007	Jun. 2008	Feb, 2005	Aug. 2010	Aug. 2013
Author	Z. Lu, K. S. Yeo, J. Ma, M. A. Do, W. M. Lim, and X. Chen	S.Goswami, T.Copani, B.Vermeire, and H. Barnaby	C.-H. Wu, C.-H. Lee, and S.-I. Liu	J. Kim and J. F. Buckwalter	Dandan Chen, Kiat Seng Yeo, Xiaomeng Shi, Manh Anh Do, Chirn Chye Boon and Wei Meng Lim
Technology	0.18-μm CMOS	0.18-μm SiGe BiCMOS	0.18-μm CMOS	0.13-μm CMOS	0.18-μm CMOS
***C*PD (pF)**	0.25	0.15	0.25	N.A.	0.25
Gain (dBΩ*)*	53 single structure	53.9 single structure	61 single structure	50	46 single structure
Power consumption (mW)	with buffer 13.5	without buffer 19.6	with buffer 70.2	45.7	without buffer 10.7 with buffer 31.5
Bandwidth (GHz)	8	7.7	7.2	29	4
Input-referred noise (pA/√Hz*)*	18	5.2	8.2	51.8	10
Group delay variation (ps)	80 ±20	N.A.	275 ±25	16	125 ±25

3. CONCLUSION

Starting with Gain Boosting technique traditional common gate topology of TIA suffers from large input noise and reduces gain which is improved by adding PMOS current source to common gate stage or by using current conveyor II stage. By adding capacitive coupling in feedback TIA provide high gain and low input noise by isolating the dc levels. Adding inductive peaking stages, shunt and series inductive peaking which improve the bandwidth of TIA. Adding automatic gain control stage, reduction of overloading problem. Capacitive degeneration stage reduces the effect of load resistance and increasing the bandwidth. Adding cross coupled current conveyor stage at the input stage of TIA improves speed and reduces noise by lowering the effect of photodiode capacitance. Using regulated cascade stage enhances bandwidth by lowering the input impedance. For improvement of bandwidth, noise and speed of transimpedance amplifier for over new technologies by using cross coupled current conveyor stage with input have series inductive peaking and output provided with capacitive degeneration stage; this procedure provides larger improvements over traditional designs of transimpedance amplifier.

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