

New Protocol of Aggressive Packet Combining Scheme: An Extension to Throughput Comparison

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ABSTRACT

Aggressive Packet Combining (APC) scheme is well established for receiving correct packet in high error prone wireless link. In APC three copies of a packet are transmitted and receiver does bit wise majority decision to get the correct copy. The main research challenge in APC is that if two or more copies of the packet become erroneous at the particular bit location then majority logic fails to correct the error and also as three copies of packet are sent at a time, throughput degradation takes place at higher error rate channel. In this paper we propose a new method of correction in APC which will address the limitation which occurs in conventional APC.

General Terms

Throughput comparison

Keywords

Packet combining Scheme, Conventional Aggressive Packet Combining (CAPC) scheme, Majority Packet combining scheme, Throughput

1. INTRODUCTION

In order to combat errors in computer/ data communication networks, ARQ (Automatic Repeat Request) techniques [1-5] with various modifications as applicable to in various communications environments are used. Leung [7] proposed an idea of Aggressive Packet Combining scheme (APC) for error control in wireless networks with the basic objective of fast error control in relatively higher noisy wireless networks. APC is well established and studied elsewhere [3-10]. Several modifications of APC are also reported elsewhere [2-8]. The modifications are due to increasing throughput, tackling various error syndromes and enhancing fast correction. In APC and/ or modified APCs, two or more copies of the packets are transmitted. Copies received by the receiver either error free or erroneous are used in receiver to correct errors by applying Packet Combining schemes differently in different situations. However in original APC, if an error occurs at same locations of erroneous packets, the application of the majority logic as in original APC fails to correct the error and also throughput degradation take place due to high error rate of the channel. To address the stated problem of APC we propose a new protocol of APC. Analytical results establish that the proposed new scheme provide better correction capability.

2. REVIEW OF PACKET COMBINING SCHEME (PC)

Chakraborty [11] suggested a simple technique where the receiver will correct limited error, one or two bit error, from the received erroneous copies. The technique proposed by Chakraborty is illustrated below:

We assume the original transmitted packet as "01010101."

The packet erroneously received by the receiver as "11010101." The receiver requests for retransmission of the received erroneous packet but keeps in store the received erroneous packet. The transmitter retransmits the packet, but again the packet is received by the receiver erroneously as "00010101." Chakraborty proposed that the receiver can correct the error by using two erroneous copies for a bit wise

XOR operation between erroneous copies may be performed to locate the error position, in the present example being as follows:

First erroneous copy 11010101

Second erroneous copy 00010101

XOR 11000000

The error locations are identified as first and/or second bit from the left. Chakraborty suggested that the receiver can apply brute method to correct error by changing received "1" to "0" or vice versa on the received copies followed the application of error decoding method in use. In the example the average number of brute application will be 0.5, and in general 2^{n-1} if n bits are found in error. Several modifications of PC have been studied elsewhere [12-13] by Bhunia's.

3. REVIEW OF CONVENTIONAL APC

APC is a modified PC having application in wireless networks. In APC, three copies of a packet are transmitted. Receiver applies bitwise majority logic operation on received three copies to correct the error.

APC is best illustrated as below:

i. Original packet=11111, and it sent from the sender. Sender sends three copies of the packet.

ii. All the packets reached the receiver with errors as: FIRST COPY: 11011, SECOND COPY: 11110 and THIRD COPY: 11011.

iii. Receiver applies majority logic bit by bit on the received three erroneous copies:

11011

11110

11011, and thus gets a generated copy as 11011.

iv. Receiver applies error detection scheme to find whether generated copy is correct or not.

As it is not correct in this case, the receiver chooses least reliable bit from majority logic.

Using XOR operation, error locations are identified. In this case these are the third and fifth bit from the left side.

4. NEW APPROACH OF APC

In this new technique, instead of sending three packets of the original packets as in conventional APC, two packets are sent. If the received two packets are erroneous then XORing of both the erroneous packets are done to locate the error positions. Now receiver sends negative acknowledgement with erroneous bit positions information to the sender and also keeping the copies that has been received erroneously. And instead of retransmitting the whole packets sender sends only the erroneous bit positions by repeating each bit three times so even if the third received packets are erroneous the receiver by using majority logic with three successive bits get the original bits that have been transmitted and erroneous locations are corrected by comparing the bits obtained after majority logic with the erroneous bit locations in the first two received packets and as in conventional APC if the packets get failed then three copies of the packet is again retransmitted which leads to throughput degradation but in this new approach instead of three two packets are send as in PC scheme and if error occurs in the received packet then the erroneous bit position is sent by successively repeating it three times that means average number of bits get reduced as compared to conventional APC scheme as a result probability of bits in error reduces at the receiver. This idea will become clearer by the following examples.

Examples:

I. Original packet-11001100

1 st erroneous packet-	11011100
2 nd erroneous packet-	10101100

XOR	01110000

The error locations are identified as 5th, 6th and 7th bit locations from the right. Now sender sends only the erroneous bits by repeating each bit three times.

The third packet sent is 111 000 000 and again if it is received erroneously like 101 001 000 but by majority logic we can get the original string that has been sent like 101-1 (7th), 001-0 (6th), 000-0 (5th). Comparing third packet with the first erroneous packet, the 5th bit in the first erroneous packet is **1** but the actual bit is **0** so the first corrected packet is 11001100. Now comparing the second erroneous copy with the third packet, the 6th and 7th bits from right of the second packet shown in bold in 1 and 0 respectively but the actual bits are 0 and 1 respectively so the 6th and 7th positions are corrected as 0 and 1 from the right. So the corrected packet is 11001100.

II. Original packet-10110100

1 st erroneous packet-	00110100
2 nd erroneous packet-	10010100

XOR	10100000

The error locations are identified as the 6th and the 8th locations from the right. After getting negative acknowledgement sender sends the 3rd packet as 111 111 and if it is received without error then by majority logic the 6th and 8th bits are 111-1, 111-1 respectively. Comparing third packet with the first erroneous packet, the 8th bit from the right in the

first erroneous packet is **0** but the actual bit is **1** so the first corrected packet is 10110100.

Now comparing the second erroneous copy with the third packet, the 6th bit from right of the second packet shown in bold is 0 but the actual bit is 1 so the corrected packet is 10110100.

III. Original packet-01101001

1 st erroneous packet-	01 001101
2 nd erroneous packet-	01100101

XOR	00101000

The error locations are identified as the 4th and the 6th locations from the right. After getting negative acknowledgement sender sends the 3rd packet as 111 111 and if it is received with an error then by majority logic the 4th and the 6th bits are 101-1 011-1 respectively. Comparing third packet with the first erroneous packet, the 6th bit from the right in the first erroneous packet is **0** but the actual bit is **1** so the first corrected packet is 01101001.

Now comparing the second erroneous copy with the third packet, the 4th bit from right of the second packet shown in bold is 0 but the actual bit is 1 so the corrected packet is 01101001.

IV. Original packet-11110000

1 st erroneous packet-	10110000
2 nd erroneous packet-	01110010

XOR	11000010

The error locations are identified as the 2nd, 7th and the 8th locations from the right. After getting negative acknowledgement sender sends the 3rd packet as 111111000 and if it is received with an error as 111 101 001 then by majority logic the 2nd, 7th and the 8th bits are 111-1 101-1 001-0 respectively. Comparing third packet with the first erroneous packet, the 7th bit from the right in the first erroneous packet is **0** but the actual bit is **1** so the first corrected packet is 11110000.

Now comparing the second erroneous copy with the third packet, the 2nd and the 8th bits from right of the second packet shown in bold are 1 and 0 respectively but the actual bits are 0 and 1 so the corrected packet is 11110000.

5. MATHEMATICAL COMPARISON OF CONVENTIONAL APC AND THE PROPOSED SCHEME

In APC scheme three packets are sent at a time so N=3 so the probability that a packet is in error is given by:

$$P_{e_{APC}} = [1-(1-\alpha)^n] * [1-(1-\alpha)^n] * [1-(1-\alpha)^n]$$

$$P_{e_{APC}} = [1-(1-\alpha)^n]^3 \text{ -----(1)}$$

In the proposed scheme the probability that a packet is in error (P_{eN}) is given by

$$P_{eN} = [1-(1-\alpha)^n]^2 * [1-(1-\alpha^3)^n] \text{ -----(2)}$$

Where α is bit error rate (BER)

N is the no. of packets being transmitted and

n is the number of bits in a packet.

By using this new technique correction capability of APC increases more than that of the conventional APC.

(ii) Throughput [15]:

In conventional APC original packets are sent three times at a time so in APC N=3 and the throughput is calculated by the following formula:

$$V_{APC} = [(1 - P_{eAPC}^3) / (3 + P_{eAPC}^3)] \text{ ----- (3)}$$

In the proposed scheme, as two copies of packet are sent as in PC and if error is located in the received packet then three successive bits of the erroneous position is sent therefore the throughput is calculated by the following formula:

$$V_{New} = [(1 - P_{eN}^{(2+1/3)}) / ((2+1/3) + P_{eN}^{(2+1/3)})] \text{ ----- (4)}$$

By using this new technique correction capability and the throughput of APC increases more than that of the conventional APC.

6. SIMULATION RESULTS

Curves (Fig. 1 to 2) have been plotted by taking values of bit error rate (α) from 10^{-3} to 10^{-2} for probability of packets in error for various values of n for APC (P_{eC}) and the proposed scheme (P_{eN}). Also we have assumed that the feedback path is error free. We measured the performance in terms of error correction capability and the throughput in %.

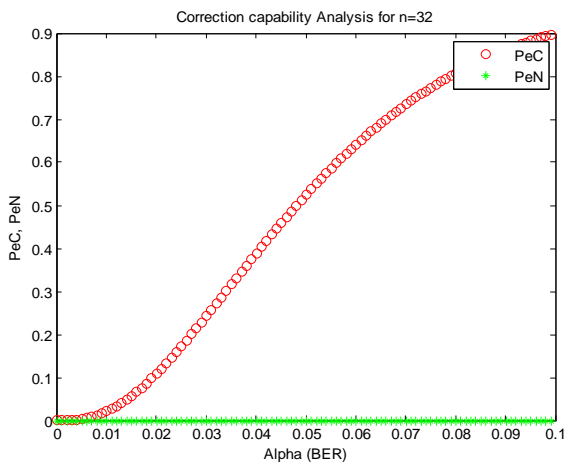


Fig. 1 Correction capability for n=32

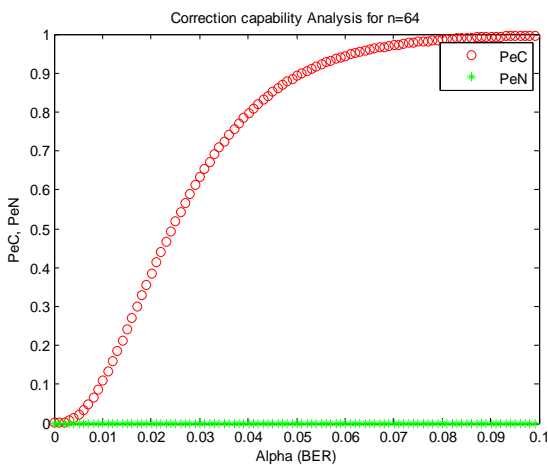


Fig.2 Correction capability for n=64

And fig. 3 and fig. 4 show the throughput of APC scheme and our proposed scheme. Simulation result shows that conventional APC gives maximum throughput of 33.5% for BER from 10^{-3} to 10^{-2} and our proposed scheme gives constant maximum throughput of 43% at any error rate.

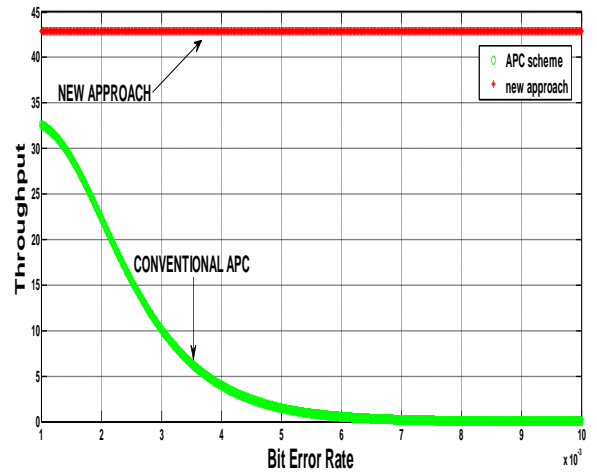


Fig.3 Throughput plot for n=1000

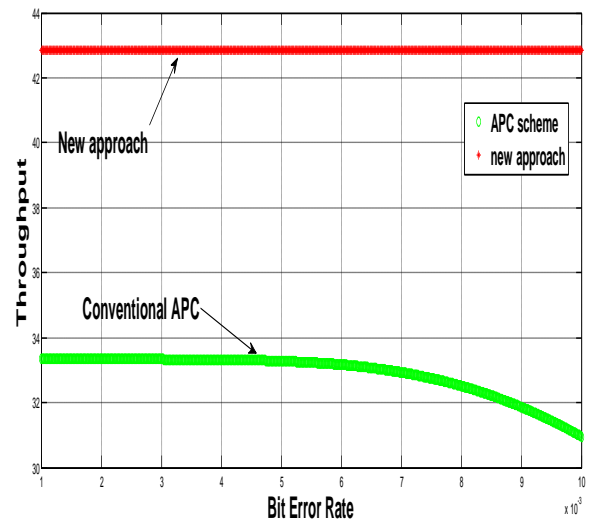


Fig. 4 Throughput plot for n=128

As observed in fig. 4 the throughput of conventional APC is maximum of about 33% at initial stage that is at low bit error rate but as the bit error rate increases throughput of the conventional APC reduces to almost zero as shown in figure.

However our proposed scheme maintains its constant throughput of about 44% for any error condition. Results show that with increase in packet size from 128 to 1000 bits, throughput increases form 43% to 44% which shows that with increase in packet size our proposed scheme will give an increased throughput for any error condition.

Curves (Fig. 1 to 4) have been plotted for probability of packets in error for various values of n for conventional APC (P_{eC}) and new proposed scheme (P_{eN}) and various values of bit error rate (α) from 10^{-4} to 10^{-1} . We measure the performance in terms of error correction capability.

7. CONCLUSIONS

In this paper, a new scheme of APC is proposed and studied. The new proposed scheme provides better correction capability and higher throughput than the conventional APC as observed from the results. Correction capability of this proposed scheme increases: (a) with increase in n (number of bits in packet), (b) with increase in bit error rate (α). Also maintains constant throughput for all error condition.

Thus the performance of this scheme is superior to the conventional APC.

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